Low-Power Low-Phase Noise LC Oscillators in Silicon-on-Sapphire CMOS Technology

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Abstract

Recent research to accommodate increasing customers' demand is focusing on low power wireless applications with a small form factor in such areas as WLAN transceivers, GPS transceivers and digital mobile phones. In particular, such a trend leads to operating frequencies over 2 GHz in the WLAN products to provide a high speed-transferring data. Recently, much effort on improving the performance of radio-frequency (RF) front-ends has been conducted in CMOS device technology for low power and low cost. However, RF components such as voltage-controlled oscillators (VCOs), power amplifiers, low noise amplifiers and mixers suffer from the drawbacks of the CMOS technology in terms of noise and poor quality (Q) factor of passive devices. In addition, low phase noise performance of the VCOs is highly desired to effectually exploit limited frequency resources.

In this thesis, a research on VCOs of low power and low phase noise is conducted in silicon-on-sapphire CMOS process. A single and a quadrature 5.8 GHz VCO are designed for targeting the intellectual property core of a WLAN front-end radio-on-chip operating in direct conversion mode. Each VCO consists of a negative G_m oscillator with an N/PMOS cross-coupled pair and an optimised LC tank. Symmetric inductors are modelled and designed in 2.5D electromagnetic field environment to obtain an optimum Q factor. Inversion-mode PMOS varactors are co-simulated to estimate LC tank tuning frequency and Q factor with S-parameter simulation results of the symmetric inductors. The bias current source in the oscillator is replaced by a noise filtering inductor and MiM capacitor to prevent the upconversion of its flicker noise and filter second-order harmonics. The single VCO exhibits a phase noise of -119.35 dBc/Hz at 3 MHz offset frequency from 0.8 V power supply voltage. It draws 0.52 mA

over a tuning frequency of 736 MHz (12.7%). A low power consumption of around 0.42 mW is achieved and a figure of merit of -189 dB is recorded; This figure of merit is the second highest among the published literatures related to RF VCOs. The quadrature VCO, consisted of two identical single LC VCOs, consumes 1.86 mW from 0.9 V supply voltage with a phase noise of -115.7 dBc/Hz at 3 MHz offset. Its tuning range reaches up to 301 MHz (5.2 %). Practical issues for the design and electromagnetic simulation of the LC VCOs are discussed and several recommendations for improving the performance of quadrature VCOs are presented.

Statement of Originality

I hereby declare that this thesis contains no material which has been accepted for the award of any other degree or diploma in any University and that, to the best of my knowledge and belief, this thesis contains no material previously published or written by another person, except where due reference is made in the text of this thesis. I also consent to this thesis being made available for photocopying and loan.

Wan-Chul Kong
5th April 2004

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Publications

1. Wan-Chul Kong, Said F. Al-Sarawi, Cheng-Chew Lim and Louis Wong, "Quasi-3D Modeling, Design and Analysis of Symmetric On-Chip Inductors in Silicon-on-Sapphire Technology", *Proc. of Conference on Microelectronics: Design, Technology, and Packaging,* part of *SPIE's International Symposium on Microelectronics, MEMS, and Nanotechnology.* In press. Perth, December 2003.

2. Wan-Chul Kong, Said F. Al-Sarawi, Cheng-Chew Lim and Louis Wong, "Ultra Low-Power Low-Noise 5.8 GHz SOS CMOS LC Oscillator", submitted, *IEE Electronics Letters,* January 2004.

List of Principal Symbols

A	sinusoidal output amplitude
A_{tank}	voltage amplitude of LC tank
$A(t)$	time-dependant amplitude
C_{avg}	average capacitance
C_{ch}	Debye capacitance
C_f	an interconnecting capacitance to a switched capacitor
C_{gdo}	gate-overlap bulk capacitance
C_{jsw}	zero-bias perimeter capacitance
C_{j0}	zero-bias junction capacitance
C_{max}	maximum capacitance
C_{min}	minimum capacitance
C_{ox}	unit capacitance of silicon dioxide
C_{par}	parasitic capacitance
C_{sub}	substrate capacitance
C_{tank}	LC tank capacitance
C_v	diode varactor capacitance
C_{var}	varactor capacitance
$C_{\text{var},\square}$	unit capacitance of tank varactor
$C(v)$	voltage-dependant capacitance
F	device excess noise number
F_{srf}	self resonant frequency
F_{tune}	tuning frequency range
f_0	oscillation frequency

G_M	total transconductance of N/PMOS pair FETs
$G_{M,\text{nmos}}$	transconductance of NMOS pair FETs
$G_{M,\text{pmos}}$	transconductance of PMOS pair FETs
$-G_m$	negative transconductance
$H(s)$	loop gain
I_{bias}	bias current
I_n	initial noise current
I_{peak}	peak current in LC tank
K_{VCO}	VCO frequency gain
L	channel length of active MOSFETs
L_D	Debye length
L_d	inductance of a differential inductor
L_{eff}	effective inductance
L_p	length of rectangle poly-silicon
L_{tank}	LC tank inductance
$L\{\Delta f\}$	phase noise at Δf offset frequency
P_{Ctank}	energy stored in a tank capacitor
P_{DC}	direct current power consumption
P_{Ltank}	energy stored in a tank inductor
P_{loss}	power loss in LC tank
P_{ref}	reference power consumption (1 mW)
P_s	charge density
Q_L	Q factor of an inductor
Q_d	Q factor of a differential inductor
Q_{dual}	Q factor of a multi-metal inductor
Q_e	effective Q factor of LC tank
Q_{ext}	Q factor of N/PMOS cross-coupled pair FETs
Q_{sw}	Q factor of a switched capacitor
Q_{tank}	Q factor of LC tank
Q_{total}	total Q factor of LC tank
Q_{var}	Q factor of a varactor

R_{ch}	MOSFET channel resistance
R_d	resistance of a differential inductor
R_{es}	effective series resistance
R_p	negative resistance
R_{poly}	poly-silicon resistance
$R_{\text{poly},\square}$	poly sheet resistance
R_s	varactor series resistance
R_{sub}	substrate resistance
R_{sw}	resistance of a switched capacitor in turn on mode
R_{tank}	LC tank resistance
S_d	differential S-parameter
$S(f)$	signal power
T	metal thickness
T_a	absolute temperature
V_B	output voltage bias of a cross-coupled LC VCO
V_{GS}	gate-source voltage
V_{TH}	threshold voltage of active MOSFETs
V_j	built-in potential
V_{max}	maximum voltage in a capacitive node
V_{peak}	peak voltage in LC tank
$V_{th,\text{pmos}}$	PMOS threshold voltage
V_0	sinusoidal output amplitude
W	channel width of active MOSFETs
W_p	width of rectangle poly-silicon
X_L	reactance by series inductance
$Y_{\text{sin\_end}}$	admittance of a single-ended inductor
Y_{sym}	admittance of a symmetric inductor
$Y_{\text{s\_sin\_end}}$	series admittance of a single-ended inductor
$Y_{\text{s\_sym}}$	series admittance of a symmetric inductor
$Y_{\text{sub\_sin\_end}}$	substrate admittance of a single-ended inductor
$Y_{\text{sub\_sym}}$	substrate admittance of a symmetric inductor
Z_d	differential Z-parameter

Z_0	impedance characteristic
a_1	Fourier series coefficient
c_i	initial bias-capacitance
c_l	increased bias-capacitance
c_n	coefficient at the nth harmonic
f_L	inductor frequency of operation
f_c	center frequency
$f_{\max}$	maximum frequency
$f_{\min}$	minimum frequency
f_0	oscillation frequency
$g_{m,\text{bias}}$	transconductance of current source FET
$h_\phi(t,\tau)$	impulse response at $t = \tau$
k	Boltzmann's constant
P_{sb}	single sideband power
P_{sig}	average power in LC tank
$q_{\max}$	maximum charge in a capacitive node
t_{ox}	silicon dioxide thickness
$u(t)$	unit step function
v_i	initial bias-voltage
v_l	increased bias-capacitance
$1/f$	flicker noise
ΔV	voltage difference by phase shift
$\Delta \mathbf{V}_{\text{bias}}$	bias voltage range for the tank circuit
Δf	offset frequency
Δq	charge difference by phase shift
$\Delta\omega$	offset angular frequency
$\Delta\omega_{1/f^3}$	angular frequency of the corner between $1/f^3$ and $1/f^2$
$\Delta\phi$	phase shift
$\Gamma(t)$	impulse sensitivity function
δ	loss tangent
$\delta(t)$	impulse function
ϵ_{ox}	silicon dioxide permittivity

ϵ_r	relative permittivity
ϵ_{si}	silicon permittivity
η	skin depth
γ	channel noise coefficient of active FETs
λ	fabrication-process parameter
μ_L	relative magnetic permeability of inductor metal line
μ_p	hole mobility
ω	radian frequency
ω_L	inductor radian frequency of operation
ω_0	fundamental angular frequency
σ	conductivity of inductor metal strips
θ	initial phase reference
θ_n	phase of the nth harmonic
$\theta(t)$	time-dependant phase
$\vec{E}$	induced electric field
$\frac{\partial \vec{B}}{\partial \vec{t}}$	derivative of magnetic flux density with regard to time

List of Abbreviations

ASITIC	analysis and simulation of inductors and transformers in integrated circuits
AM	amplitude modulation
AGC	automatic gain control
BiCMOS	bipolar complementary metal oxide semiconductor
BJT	bipolar junction transistor
BOX	buried oxide
CAD	computer-aided design
CMOS	complementary metal oxide semiconductor
D	dimension
DC	direct current
DECT	digital enhanced cordless telecommunication
DRAM	dynamic random access memory
DVCO	distributed voltage-controlled oscillator
EM	electro-magnetic
FD	fully-depleted
FET	field effect transistor
FM	frequency modulation
FOM	figure of merit
GaAs	gallium arsenide
GPS	global positioning system
HF	higher frequency

IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IP	intellectual property
ISF	impulse sensitivity function
ISM	industrial, scientific and medical
LC	inductance-capacitance
LDD	lightly doped drain
LO	local oscillator
LTI	linear time invariant
LTV	linear time variant
MEMS	micro-electro mechanical system
MESFET	metal extrinsic semiconductor field effect transistor
MiM	metal-insulator-metal
MMIC	microwave monolithic integrated circuit
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
NMF	noise modulating function
NMOS	n-channel metal oxide semiconductor
PD	partially-depleted
PHEMT	pseudomorphic high-electron-mobility transistor
PLL	phase-locked loop
PMOS	p-channel metal oxide semiconductor
PS	poly-silicon
PSD	power spectral density
PGS	patterned ground shield
Q	quality factor
RC	resistance-capacitance
RC-CR	resistance capacitance - capacitance resistance
ROC	radio-on-chip
RF	radio frequency
SEM	scanning electron microscopy
SiGe	silicon germanium

SNR	signal-to-noise ratio
SOC	system-on-chip
SOI	silicon-on-insulator
SOS	silicon-on-sapphire
SPICE	simulation program with integrated circuit emphasis
UTSi	ultra-thin silicon
VCO	voltage-controlled oscillator
WLAN	wireless local area network

Chapter 1

Research Background

A voltage-controlled oscillator (VCO) is a critical component of a radio-on-chip (ROC). Research studies on low power and low phase noise of the component are being actively conducted in the CMOS process. However, the conventional CMOS process has numerous drawbacks for designing RF ICs, which require a superior device technology or noise-dealing technique to offset the disadvantages. This chapter provides a review on silicon-on-insulator (SOI) CMOS, especially silicon-on-sapphire (SOS) CMOS device technology, and surveys the topologies of various VCOs. In addition, it presents the motivation for the current research on a low power low noise inductance-capacitance (LC) oscillator.

1.1 Introduction

The rapid growth of portable communication systems is creating a continuous demand for the mobile products of higher performance. Market research by Cahners In-Stat [5] reports that the wireless local area network (WLAN) chipset market grows to over $ 1 billion by 2004 from $ 319 million in 2001. In addition, much research for next generation wireless systems and global positioning systems (GPS) is performed to support interactive multimedia services, and global mobility and service portability [6][7][8]. Since mobile applications require a long-lasting operation and a small form factor, system-on-chip (SOC) technology emerges as the best solution to reduce power con-

sumption and complexity of integrated systems. In addition, a strict requirement for accurate frequency operation under signal interference must be met as the complexity of wireless systems is increased. Meanwhile, a great number of technical issues such as thermal interaction and crosstalk between mixed analog and digital cores remain to be solved to integrate a system in a small chip area[1]. Consequently, active research centering around device technologies is conducted to attenuate unacceptable effects caused by a conductive substrate or external radiation.

In the telecommunication environment, undesired signals such as device noise or signal interference generally coexist with a required signal. Any signals that interfere with the required signal can be regarded as noise signals and an accurate extraction of the required signal from the received signals for wireless systems becomes a specific issue. Such a matter is commonly correlated with noise performance of wireless transceivers, particularly selectivity and sensitivity are utilised as a method to measure the overall performance. According to Martin *et al.* [9], the selectivity is determined by phase noise of a local oscillator (LO) and in particular, VCO noise characteristic. In consequence, phase noise characteristic of the VCO operates as a key factor to decide the maximum number of subscribers in a telecommunication service and the available number of frequency channels.

Phase noise of the VCO is influenced by diverse noise sources. These sources are mainly comprised of the inherent noise characteristic of the VCO, the supply variation and the substrate noise [9]. In addition, the division ratio of a frequency divider in a phase-locked loop (PLL) and the bandwidth of the PLL itself are often regarded as critical factors for noise performance of the LO. Above all, phase noise among the noise sources is the dominant factor in determining the VCO performance. Figure 1.1 shows the effect of phase noise in frequency translation of an RF receiver.

The received signal spectrum commonly consists of a weak desired signal and many strong adjacent channels. If the LO signal is a pure tone, the desired signal is down-converted without error. However, if the desired signal is mixed with the LO signal

[1]For example, ground noise becomes a problem for analog circuitry since digital switching may cause variations in signal ground. It is because of current variations during the switching cycle. Analog blocks are more sensitive to this problem than the digital counterpart.

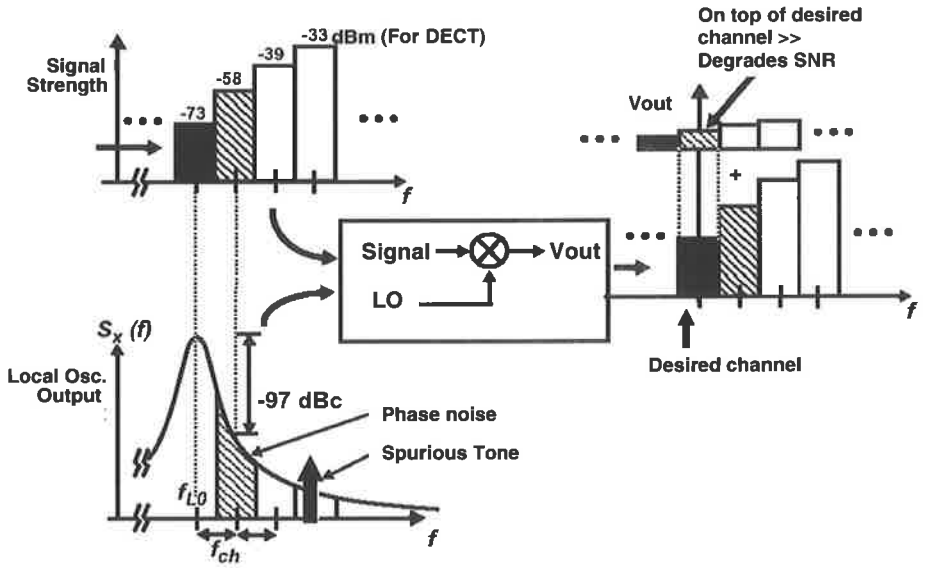


Figure 1.1: Non-ideal frequency translation [1].

constituting of phase noise and a spurious tone, the desired signal with the adjacent signals are down-converted and can fall in the same frequency band. Consequently, partial adjacent signals are added to the desired signal and the translated signals degrade the signal-to-noise ratio (SNR) of the receiver. On this account, it becomes an essential issue to reduce phase noise in VCOs.

1.2 Advanced Device Technology: Silicon-on-Sapphire CMOS

Considerable efforts to improve the noise performance of the LOs has been made through vigorous studies around phase noise of PLLs in Lim *et al.* [10], Chien and Gray [11] and Lin *et al.* [12]. First of all, diverse approaches on low phase noise of VCOs based on CMOS technology have formed the main stream [13][14][15][16]. Since a Si-based field effect transistor (FET) functioning was presented for the first time by Khang and Atala in 1960 [17], the CMOS device technology has been recognized as a promising substitute for contemporary device technologies such as bipoloar junc-

tion transistor (BJT) and gallium arsenide (GaAs) with advantages of low cost, low power consumption and high integration in microelectronic industry. However, the typical bulk CMOS structure causes nonlinearity, coupling effect and high loss, and its poor passive components seriously contribute deepening noise and malfunctions to RF wireless or space-qualified applications. To overcome such shortcomings of CMOS technology, alternative approaches have been under consideration with existing device technologies such as SOS and SOI that have been disregarded due to high manufacturing cost and low yield compared to bulk CMOS technologies.

As a variation of SOI CMOS technology, SOS CMOS technology developed by Rockwell emerges as a good solution for reducing cross-talk, substrate effect, nonlinearity and low Q factor in mixed signal processing or RF circuits [18]. In particular in monolithic implementation of a VCO, a high Q factor of passive devices is essential for low phase noise. Although SOI technology was originally devised for radiation-hardened space and military applications, the application scope is being widened owing to its superior device characteristics.

SOI CMOS technology is typically classified into partially-depleted (PD) and fully-depleted (FD) SOI processes. The silicon active regions which are electrically isolated as shown in Figure 1.2 eliminate the latch-up problem and increase the packing density by adopting buried oxide (BOX) film.

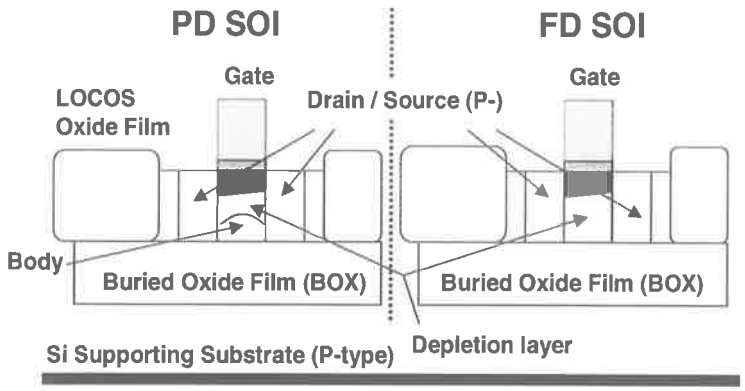


Figure 1.2: PD/FD SOI p-channel MOSFETs.

Due to the lower parasitic capacitance associated with smaller junction areas compared

with bulk CMOS, SOI CMOS technology provides high speed switching and lower leakage current between adjoining transistors. Specifically, FD SOI offers more merits than PD SOI because FD SOI reduces the charge sharing in the channel region and the depletion capacitance. As a result, it improves tolerance for short channel effect and realizes a better subthreshold slope.

In contrast, SOS CMOS technology, as illustrated in Figure 1.3 (ultra-thin silicon (UTSi) process technology of Peregrine Semiconductor Corp. [19]), provides an enhanced device characteristic through replacing Si substrate with sapphire compared to SOI CMOS technology.

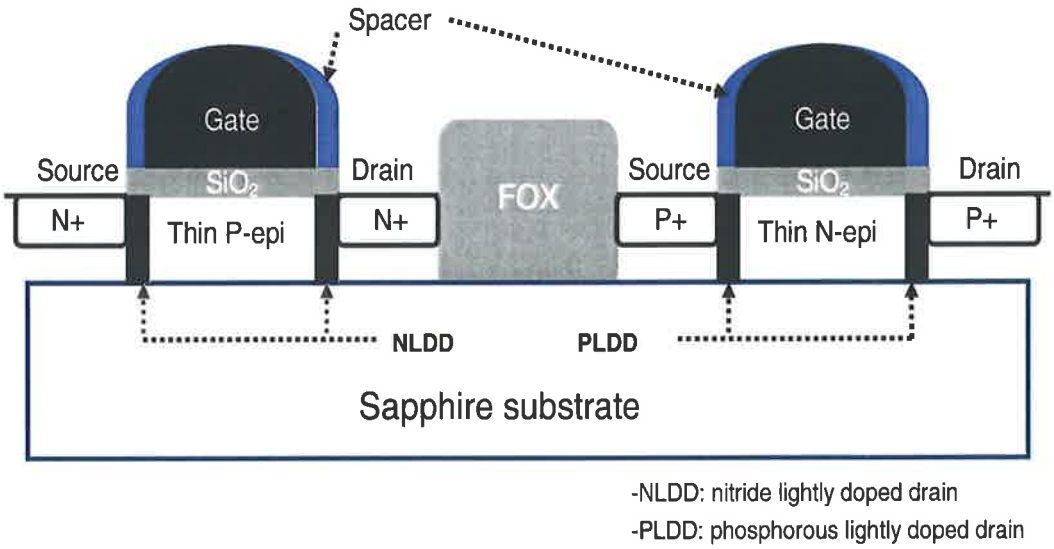
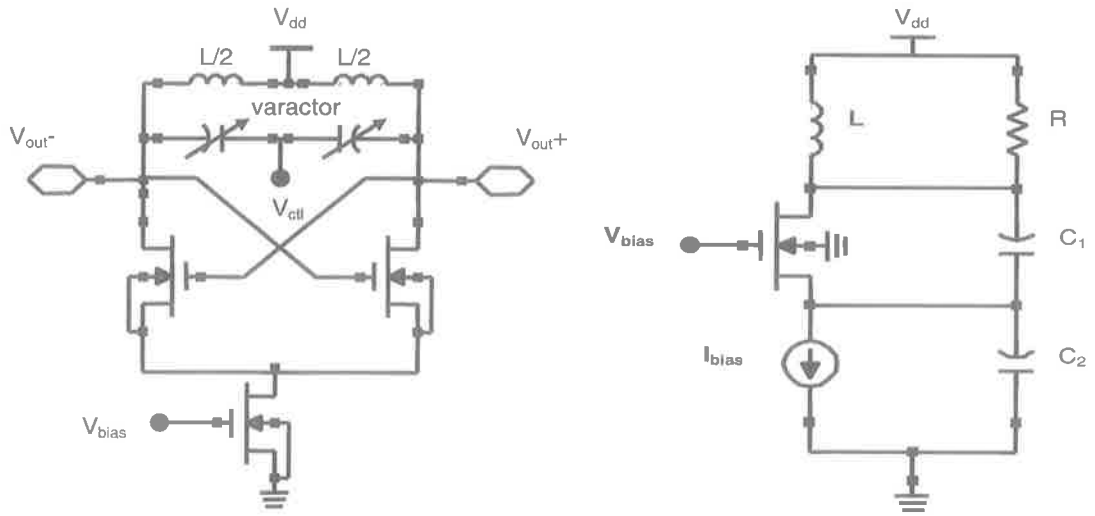


Figure 1.3: CMOS architecture in UTSi SOS process.

Besides, a reduced lifetime of minority carrier (electron for p-channel metal oxide semiconductor (PMOS) or hole for n-channel MOS (NMOS)) as well as improved electrical characteristics in PMOS makes SOS CMOS technology more beneficial compared with existing SOI CMOS [20]. The reduced lifetime of minority carrier indicates SOS CMOS technology can suppress body effect resulting in weaker kink effect and consequently improve immunity for noise sensitivity [21][22]. The higher thermal conductivity of sapphire substrate can lessen self-heating effect in comparison with SOI CMOS. Due to a thick insulating layer of sapphire, induced current by EM field is rarely formed in the



(a) NMOS cross-coupled oscillator.

(b) Colpitts oscillator.

Figure 1.4: Basic LC VCOs.

variable capacitors (varactors) attenuates the oscillating signals[4], active transistors in the LC VCOs work as an energy loss compensator to the LC tank. In consequence, Q factor of the passive devices including the varactors becomes a critical factor for lowering phase noise.

According to Leeson's model [40], phase noise of the VCO is generally mitigated as the core power of LC VCOs increases and can be directly controlled by direct current (DC) bias current. However, a better phase noise performance is actually obtainable in a limited range of the bias current (current-limited regime) and tends to be deteriorative over a certain value. In addition, it is advisable to set the DC current at a proper level since it is related with an issue of power consumption. Phase noise characteristics of VCOs will be discussed further in Chapter 2.

[4]Without supplying energy to the LC tank, the amplitude of output signals comes to be gradually smaller and finally the oscillation stops.

1.4 Research Motivation for Low Power Low Noise LC VCOs

Phase noise and power consumption are critical factors for mobile products. In wireless applications, the required power consumption and phase noise for LOs are a trade-off depending on telecommunication standards. However, the issues of power consumption and phase noise have a close relation to mobile communication, particularly the VCOs as an integrated component of the LOs. For this purpose, much endeavor related to the noise performance of VCOs with low power issue is still being conducted on the basis of an inexpensive CMOS process. As shown in Table 1.1, most experiments have been mainly performed in typical CMOS processes. Furthermore a variety of inductors such as a hollow circular inductor [41], a patterned-ground shield inductor [42], a multi layer inductor [43] and a differential inductor [44] have been investigated for the purpose of enhancing LC-tank Q on silicon substrate since Q factor improvement of passive devices is determinative for the phase noise performance [45].

However, the conductive layer causes a large amount of signal loss by inevitable EM field or external radiation compared to SOS CMOS process as mentioned in Section 1.2[5]. Moreover, approaches to design low power low noise oscillators in SOS CMOS process can be advantageous by low loss substrate and linear high transconductance transistors. In view of the manufacturing cost, the SOS CMOS is comparable to the bulk CMOS per square millimeter and costs much less compared to silicon germanium (SiGe) and GaAs processes by around 40 to 70 percentage [46].

Hajimiri [47] suggests that design complexity and power consumption of LC-tank VCOs generally increase over 10 GHz frequency to obtain spectral purity, wider tuning range and high gain of transistors. However, some recent papers [26][48][49] related to LC VCOs are showing good research results arguing the hypothesis even if power consumption is gradually increasing at higher frequency. This indicates LC VCOs can be exploited for high frequency (HF) applications.

Meanwhile, flicker noise ($1/f$) of SOS metal oxide semiconductor field effect transis-

[5]To alleviate the substrate loss, high resistive or suspended (i.e. empty) substrate can be provided for RF devices implementation.

tors (MOSFETs) becomes a critical issue due to severe lattice mismatch in comparison with bulk CMOS [50] and the noise up-conversion to phase noise may require an approachable minimization technique. In order to accommodate these issues, additional research on approaches to low phase noise LC VCOs in the prominent device process of SOS CMOS technology is necessarily accompanied with added low power advantage. The LC VCO design in this research is targeted for implementation in a 0.5 μm SOS CMOS process for direct conversion WLAN (IEEE 802.11 a) transceiver operating at 5.8 GHz ISM band (5.725 - 5.850 GHz). A single and a quadrature LC VCO are designed toward a phase noise better than -115 dBc/Hz (c of dBc: carrier) at an offset frequency of 3 MHz in below 1 V power supply. Table 1.1 will be used as a benchmark in evaluating the performance of the LC VCOs designed in terms of low power dissipation and phase noise. The utilised design procedure in this research follows a typical RF integrated circuit (IC) design flow as shown in Figure 1.5 and can be changed depending on available IC computer-aided design (CAD) tools. The conducted research covers post-layout simulation just before fabrication step (which is not shown in the flow of Figure 1.5) and the resistance-capacitance (RC) extraction step is replaced with EM field simulation.

1.5 Contributions of the Thesis

The major contributions made in this thesis are:

1. to provide a low power LC oscillator as an IP core.
   Power dissipation in wireless applications is specially critical for portable devices. In addition, it is advisable to design a low power VCO in a small chip area. To reduce a power consumption of the oscillator core, peripheral circuits inclusive of a current source will be excluded. This also makes the LC VCO compact. High Q symmetric inductor is designed for lowering energy loss which is directly associated with negative resistance, thus decreasing MOSFET finger number. The LC VCO designed in this thesis consumes the lowest power at 5.8 GHz compared to what presented in the accessible literature.

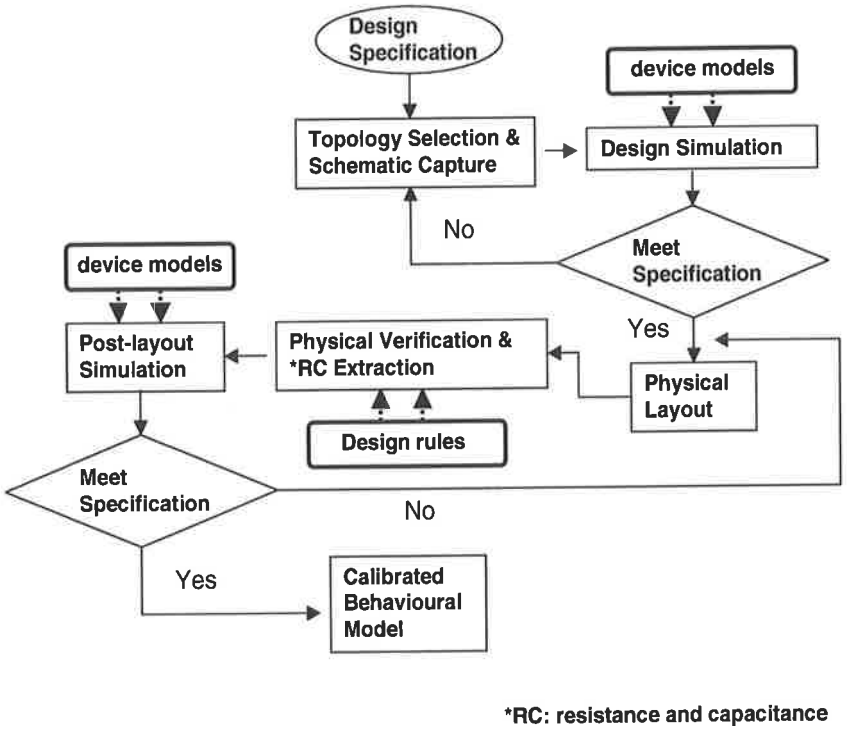


Figure 1.5: Full custom RF IC design flow.

2. to improve a phase noise performance of LC VCOs at a given low power supply voltage.

   As the power supply voltage is reduced, available tank voltage amplitude decreases. Therefore, VCO phase noise performance must not be degraded because the low power output spectrum becomes sensitive to noise. At a low supply voltage below 1 V, a filtering technique using a planar inductor and a metal-insulator-metal (MiM) capacitor can be beneficial to suppress flicker-induced upconversion to phase noise and applied to filter out problematic second-order harmonics. A monolithic inductor and a MOS varactor of LC tank are optimised to achieve high Q tank.

3. to provide a design methodology for high Q integrated inductor in SOS CMOS process.

Quality of passive devices such as an integrated inductor is one of quite important factors to determine phase noise performance of LC VCOs. In this thesis, a procedure for optimizing a symmetric inductor on sapphire substrate is investigated. This optimisation was conducted using quasi-3D modelling method.

1.6 Thesis Organization

This thesis consists of six chapters:
Chapter 1 introduces the motive of the research on a low-power low-phase noise LC VCO in SOS CMOS device technology.

Chapter 2 presents a complete analysis of LC VCO in terms of its oscillation mechanism and noise characteristics.

Chapter 3 presents a variety of on-chip inductors and their characteristics. Modelling, design and analysis of symmetric inductors on sapphire substrate are conducted on 2.5 dimension (D) EM simulation environment.

Chapter 4 surveys a variety of tank varactors in CMOS fabrication process together with UTSi SOS process and introduces an analysis process for an optimum Q varactor through co-simulation methodology.

Chapter 5 presents the design procedure of low-power low-phase noise single and quadrature LC VCOs, and provides simulation results in UTSi SOS 0.5 μm process from post-layout designs.

Chapter 6 concludes this thesis by comparing the overall VCO performance with other VCOs presented in the literature and presents suggestions for future work.

Chapter 2

Negative Transconductance Voltage-Controlled Oscillator Fundamentals

An oscillator is a circuit with a sustained oscillation without input stimulus. The oscillator needs to be stabilized in frequency to correct frequency instability caused by inherent parasitic resistances of its integrated components, effects of the noise sources and its nonlinear operation associated with phase noise. This chapter focuses on the oscillation theory, the operational analysis and the phase noise characteristic of a negative transconductance (-G_m) voltage-controlled oscillator (VCO).

2.1 -G_m Oscillation Theory

Most mobile applications adopt a method of frequency synthesis for signal demodulation and modulation using a local phase-locked loop (PLL). In order to upconvert outgoing baseband or downconvert incoming RF signals, it is necessary to provide controllable periodic signals to a mixer. A VCO is required to generate variable oscillation frequency to meet the telecommunication standard.

An RF oscillator is characterized by a self-sustaining mechanism to oscillate at a specific frequency band. The continuous oscillation can be implemented and analyzed with a

feedback network for amplifying periodic signals. Figure 2.1 depicts the linear time-invariant (LTI) system with feedback.

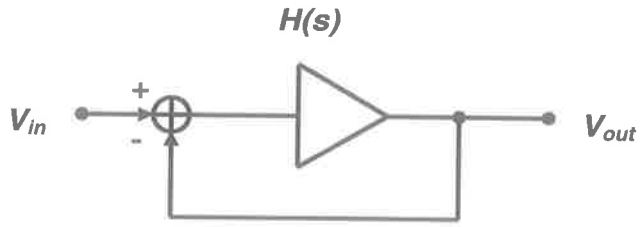


Figure 2.1: Linear time invariant (LTI) system with feedback.

The transfer function of the system in Figure 2.1 is:

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{H(s)}{1 + H(s)}. \tag{2.1}$$

The conditions for oscillation to occur requires that the magnitude of the loop gain at an oscillation frequency is equal to unity and the phase shift is zero.

2.1.1 One-port Oscillator

An oscillator with a frequency selective network (i.e. LC resonator) can be analyzed with a one-port network as in Figure 2.2.

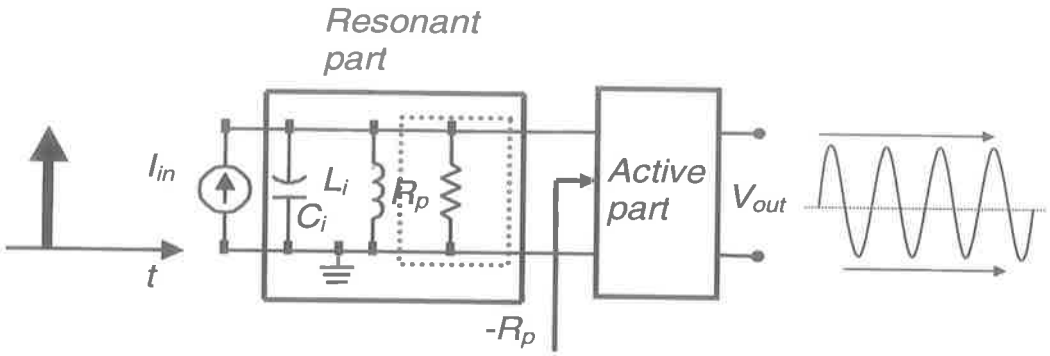


Figure 2.2: One-port oscillator.

C_i, L_i and R_p represent an ideal capacitance, inductance and a parasitic resistance

of the LC tank[1], respectively. Looking into the active part, $-R_p$ denotes a negative resistance of the active MOSFET pair to cancel the parasitic resistance. The current source of I_{in} models an initial noise current injected into the tank circuit, which is originated from the active part.

A typical LC VCO can be divided into two functional blocks of an active part and a resonant part as shown in Figure 2.3.

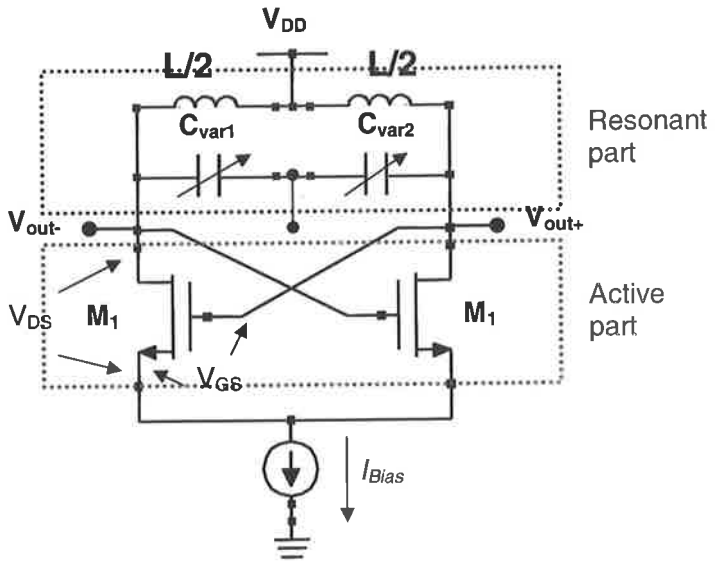


Figure 2.3: Typical NMOS pair VCO schematic.

The resonant part consists of an integrated inductor and a variable capacitor tuned to generate a resonant frequency. If the inductor and capacitor are ideal, energy loss is not occurred in the tank since no parasitic resistance exists. Consequently, the resonant part can infinitely provide oscillation without damping the output signals.

However, all of actual integrated components commonly have the parasitic resistance due to their metalisation or defect during fabrication resulting in unavoidable charge loss (i.e. electric and magnetic energy loss). Accordingly, the tank represents a decaying oscillatory behaviour due to reduced signal power and eventually oscillation stops as

[1]The parasitic resistance actually indicates a wide range of parasitic resistances added from the adjacent components to the tank.

depicted in Figure 2.4.

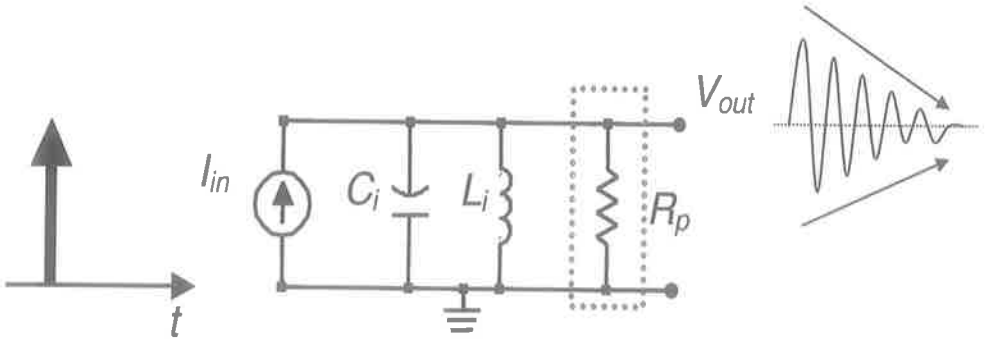


Figure 2.4: Damping oscillatory behaviour by parasitic resistance of the tank.

To sustain oscillation, the corresponding energy loss in the tank is required to be compensated by an energy source such as BJT or MOSFET active device. From this viewpoint, active devices work as a compensatory factor for the lossy components. The negative transconductance[2] (or $-G_m$) is adopted for the LC VCO to provide a compensatory meaning against the energy consumption by the parasitic resistances.

2.1.2 -G_m Oscillator

As for generation mechanism of the negative resistance, it is intuitive to inspect DC operation of the -G_m oscillator. Since the NMOS pair in Figure 2.3 operates in saturation region, the bias current (I_{bias}) can be defined as:

$$I_{\text{bias}} = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_{GS} - V_{TH})^2, \tag{2.2}$$

provided that a long channel MOSFET model is used neglecting body effect at low frequency. The transconductance of each transistor in the NMOS-pair configuration is derived as:

[2]Passive devices cause energy dissipation by thermal heating. Contrary to the customary meaning, minus (-) in front of the negative resistance ($-R_p$) indicates supplying energy such as a power supply or an active device.

$$G_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH}). \tag{2.3}$$

If ideal active devices of the NMOS pair are used, each side of the NMOS pair can be modelled as a cyclostationary[3] current source of which characteristic is dominated by the geometry and fabrication process as shown in Figure 2.5.

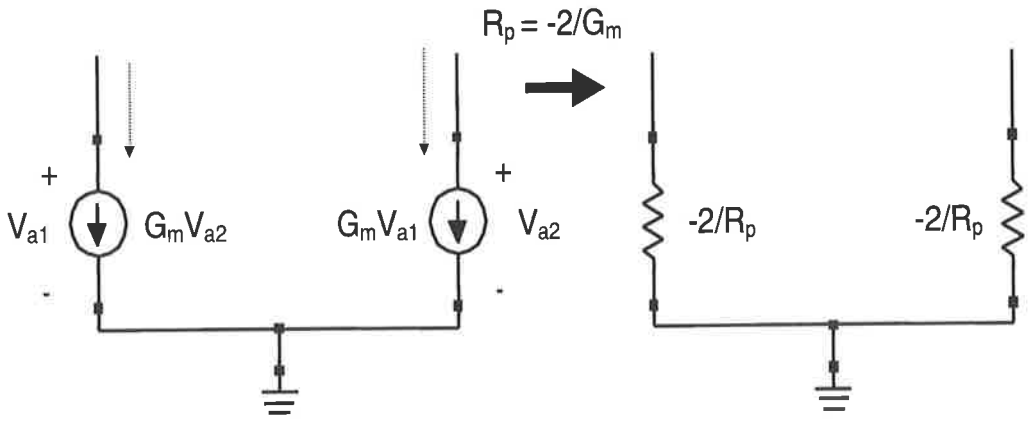


Figure 2.5: Conceptual negative resistance of the LC VCO.

Since the G_m parameter can be replaced with negative resistance, the NMOS-pair active part of the oscillator is simplified to the two resistive components. In DC analysis, the tank inductors work as a series of shortened metal strips (i.e. short circuit) and the variable capacitors become an opened node by frequency characteristic of the capacitor dielectric material. Consequently, the negative resistance becomes connected to the equivalent tank of the simplified VCO of Figure 2.2 in parallel and cancel the energy loss in the tank at alternative current (AC) response.

Contrary to a conventional in-/output system, the VCO has no input port for stimulating the oscillator to induce regular output signals as can be seen in Figure 2.6.

Subsequently, the startup of oscillation seems to be vague. Such ambiguity can be settled by thermal noise of the active part which affects the initial oscillation startup of the VCO.

[3]Generally speaking, each side of the MOSFET pair regularly turns on/off regarding on the oscillation period to generate a differential output.

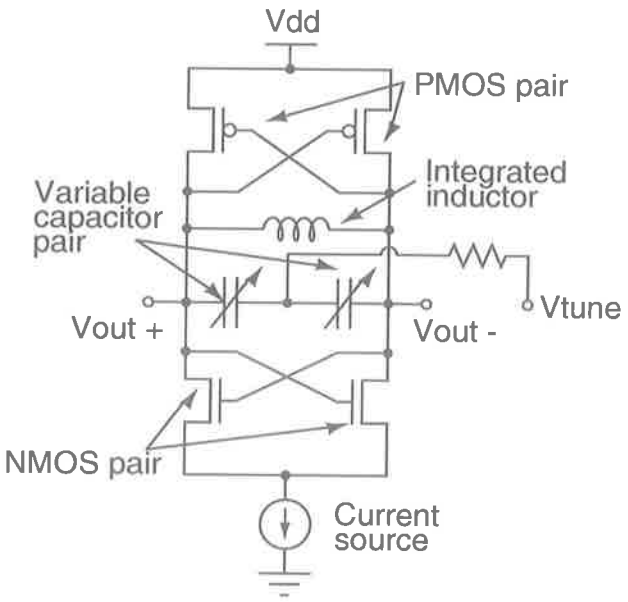


Figure 2.6: Typical complementary $-G_m$ VCO schematic.

Thermal noise has a quasi-constant power up to 100 GHz (white noise) compared to flicker or power noise and is generated in the transistors as the bias current flows through the active part. In addition, thermal noise by resistive component of the tank inductor provides a startup factor for oscillation. Within a frequency band determined by the resonant part, the thermal noise is amplified with differential outputs along the feedback loop and repeated to be suppressed by the resonant part. Such a cyclic operation drives the loop gain of the oscillator over 1 and with voltage limiting mechanism, forces the oscillator into a steady state oscillation.

2.1.3 Analysis of Complementary $-G_m$ Oscillator

In contrast to NMOS or PMOS-only cross-coupled oscillators, a complementary $-G_m$ oscillator (also known as a double cross-coupled oscillator) has a differential voltage swing limited by supply voltage (V_{DD}). An NMOS-only cross-coupled oscillator generates an output voltage swing over V_{DD} at the drain port due to the same bias reference to V_{DD}. Meanwhile, the complementary cross-coupled oscillator shuts off the bias cur-

rent at the same situation since the PMOS cross-coupled pair goes into cutoff mode. Furthermore, the typical $-G_m$ oscillator generally adopts a current source to provide a stable bias current through a current mirror. Therefore, the output swing is limited by the transistor gains of the cross-coupled N/PMOS pairs and the bias current. As a result, the maximum differential amplitude at the output ports can reach close to V_{DD} without cutting off the output swing, through setting the zero crossing-point of the differential voltage swing at half V_{DD}[4].

As shown in Figure 2.7, the complementary $-G_m$ oscillator can be reconstructed with two inverters from the original schematic of Figure 2.6.

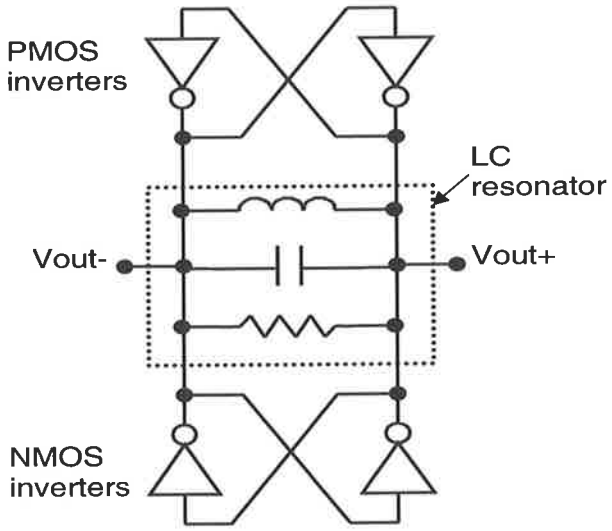


Figure 2.7: Equivalent complementary $-G_m$ oscillator with inverters.

Since a CMOS inverter consists of a couple of NMOS/PMOS transistors, the simplified oscillator results in two individual $G_{M,\text{nmos}}$ (NMOS transconductance) and $G_{M,\text{pmos}}$ (PMOS transconductance) combined in parallel. The negative resistance can be written as:

$$R_{neg} = \frac{-2}{G_{M,\text{nmos}} + G_{M,\text{pmos}}}, \tag{2.4}$$

[4]The output amplitude of NMOS or PMOS-only counterparts is only dependant on the tail current.

provided that the NMOS and PMOS pairs are sized appropriately. Such an increase in the total negative resistance leads to enlarge the MOSFETs gain as large as twice at a given bias current. Hence, this results in a better phase noise characteristic of the cross-coupled VCO contrary to an NMOS or PMOS-only counterpart. Such CMOS inverters are provided by the IC manufacturing companies in optimised full custom layout cells and can be easily utilised for optimal VCO design[5].

2.1.4 Frequency Tuning Range of $-G_m$ Oscillator

The oscillation frequency of an LC VCO is determined by a combination of the LC-tank inductance and capacitance of which impedance magnitude becomes equal. Consequently, the oscillation frequency is set by the resonant frequency of the tank[6] and is defined as:

$$f_0 = \frac{1}{2\pi\sqrt{L(C_{\text{var}} + C_{\text{par}})}}, \tag{2.5}$$

where f_0 is the oscillation frequency, C_{var} and C_{par} are the tank varactor capacitance and parasitic capacitance, respectively and L is the tank inductance.

The total LC-tank capacitance that determines the oscillation frequency with the tank inductance is dominated by a parasitic capacitance of the N/PMOS cross-coupled pair, the tank varactor capacitance and the inductor parasitic capacitance. The inductor forms its parasitic capacitance by a synthetic combination of a crosstalk capacitance between adjacent wires, a coupling capacitance between input and output ports and an overlap capacitance between the metal strips and the cross connection. In addition, a field oxide capacitance and a substrate capacitance can be included to the total inductor parasitic capacitance. The varactor capacitance is mainly determined by the intrinsic capacitance in inversion or accumulation operation mode. Since the tuning range (F_{tune}) is represented with a ratio of the maximum (f_{max}), minimum (f_{min}) and center (f_c) frequencies as:

[5]Strictly speaking, it is mainly limited to digital applications.

[6]A word of "resonant"means an equilibrium status in which no energy exchange occurs between the tank inductor and capacitor at a certain frequency.

$$F_{\text{tune}} = \frac{f_{\max} - f_{\min}}{f_c} = 2 \times \frac{f_{\max} - f_{\min}}{f_{\max} + f_{\min}}, \tag{2.6}$$

the actual tuning range is rewritten as:

$$F_{\text{tune}} = 2 \times \frac{\frac{1}{\sqrt{C_{\text{par}}+C_{\min}}} - \frac{1}{\sqrt{C_{\text{par}}+C_{\max}}}}{\frac{1}{\sqrt{C_{\text{par}}+C_{\min}}} + \frac{1}{\sqrt{C_{\text{par}}+C_{\max}}}}. \tag{2.7}$$

From Eq.(2.7), it can be said that C_{par} broadly contributes to the oscillation frequency and particularly, the largest tuning range is achievable if the C_{par} is the smallest. Looking into the N/PMOS cross-coupled pairs at the two differential output nodes in Figure 2.6, a gate-to-source capacitance (C_{gs}) and a gate-to-drain capacitance (C_{gd}) can be represented as parasitic capacitances added into the tank capacitance. Figure 2.8 shows the two parasitic capacitances in a double cross-coupled LC oscillator.

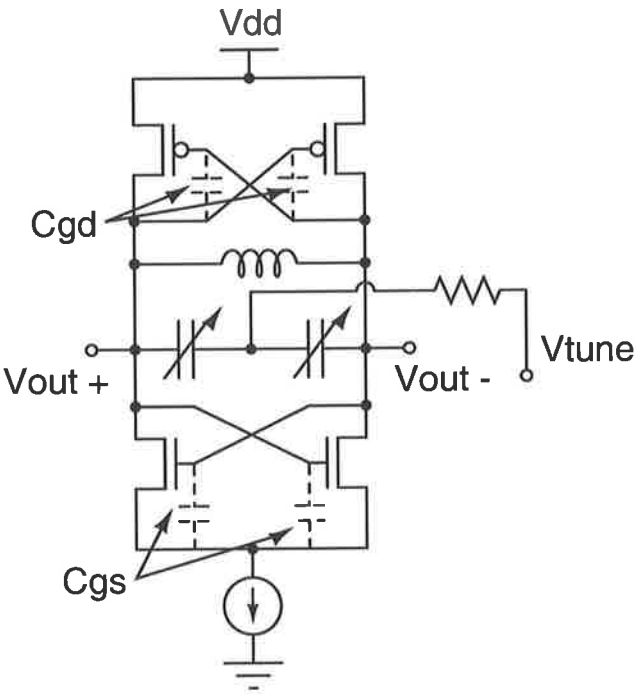


Figure 2.8: Parasitic capacitances of C_{gd} and C_{gs}.

Assuming that a virtual ground is connected to the common node of the tank varac-

tors, the net capacitance tunes the LC oscillator to a lower oscillation frequency and results in a frequency deviation from the targeted oscillation frequency. In designing an oscillator, consideration of the parasitic capacitance becomes an important issue because a tradeoff exists between the device size and tuning range. In order to obtain a large amplitude for low phase noise, the device size must be as large as possible since the gain (G_m) of the cross-coupled pair is proportional to $\frac{W}{L}$. However, the increased device size correspondingly increases the parasitic capacitance and affects the tuning range of the oscillator.

In addition, the gate resistance works as a frequency-limiting factor of the negative G_m oscillator at high frequency. As demonstrated in Figure 2.9, a gate resistance (R_g) is in series with a gate capacitance of a cross-coupled active device in the small signal model at high frequency[7].

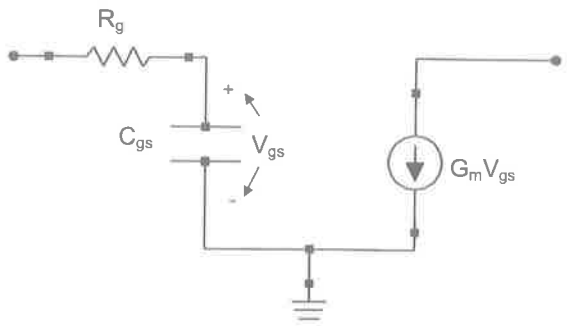


Figure 2.9: Simplified small signal MOSFET model at high frequency.

From Figure 2.9, the combined R_g and C_{gs} have a characteristic of a low pass filter. Consequently, the input admittance includes a pole determined by the value of R_g and C_{gs} and tends to increase the magnitude of the negative resistance at high frequency. To minimise the parasitic resistance, the MOSFETs of the oscillator must be laid out with a multiple finger structure.

[7]A gate-to-drain capacitance (C_{gd}) is ignored due to the fact that it can be added into the tank circuit as a lumped element.

2.2 Phase Noise Fundamentals

2.2.1 Phase Noise Definition

For RF oscillators, the most critical characteristic is frequency stability. Oscillator noise characteristic related to the stability is mainly estimated with jitter in time domain for clock recovery and phase noise in frequency domain for frequency synthesis.
Phase noise is usually quantified by the noise power of a single sideband in an 1 Hz bandwidth at an offset angular frequency ($\Delta\omega$) from the fundamental angular frequency (ω_0). It has a unit of decibel below the carrier signal per Hertz (dBc/Hz) and is defined as:

$$L\{\Delta\omega\} = 10\log\left[\frac{P_{sb}(\omega_0 + \Delta\omega_{,1Hz})}{P_c}\right], \tag{2.8}$$

where $P_{sb}(\omega_0 + \Delta\omega_{,1Hz})$ represents the single sideband power at an offset angular frequency of $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz.
Assuming that an oscillator generates a pure sinusoidal signal, i.e. $V_{\text{out}}(t) = A\sin(\omega_0 t + \theta)$, the output signal of the ideal oscillator has only one frequency component (Dirac Impulse) in frequency domain. Here, A, ω_0 and θ are defined as the amplitude of the sinusoidal output, the oscillation angular frequency and the initial phase reference of the oscillator, respectively.
However, an actual oscillator presents time-dependant fluctuations of output amplitude ($A(t)$) and phase ($\theta(t)$) caused by inherent noises of the integrated devices and its nonlinear operation. Correspondingly, the stainless output spectrum is rearranged by [51]:

$$V_{\text{out}}(t) = V_0[1 + A(t)]\sin(\omega_0 t + \theta(t)), \tag{2.9}$$

where V_0 is the voltage amplitude of the output waveforms. In frequency domain, as a result, the oscillation frequency band spreads to both sidebands centered with the fundamental impulse spectrum by random variation of the amplitude and phase components in time domain. Figure 2.10 illustrates a comparison between an ideal sinusoidal spectrum and an actual output spectrum with phase noise.

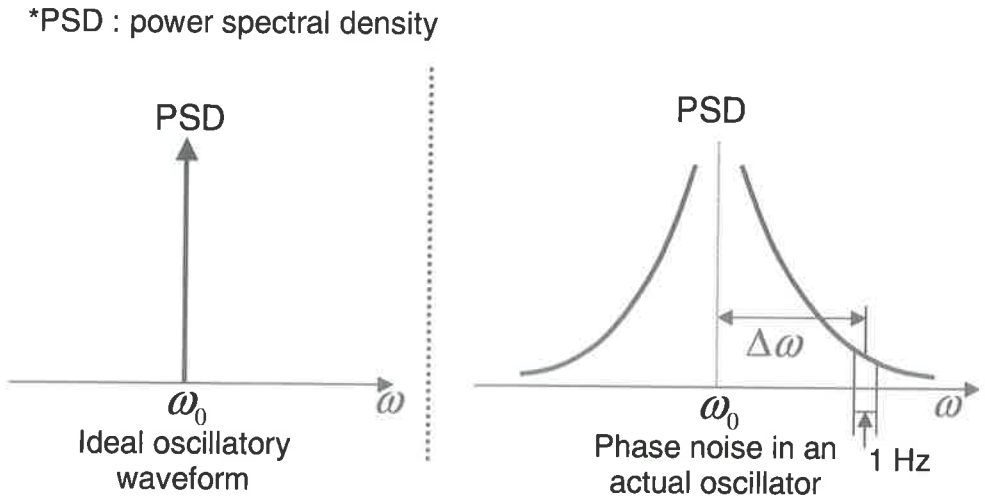


Figure 2.10: Ideal sinusoidal output and actual oscillation spectrum with phase noise.

The fluctuations of amplitude and phase in oscillatory outputs can be observed through impulse response of the oscillator [51]. Figure 2.11 illustrates the impulse response of an ideal oscillator with regard to its output amplitude and phase.

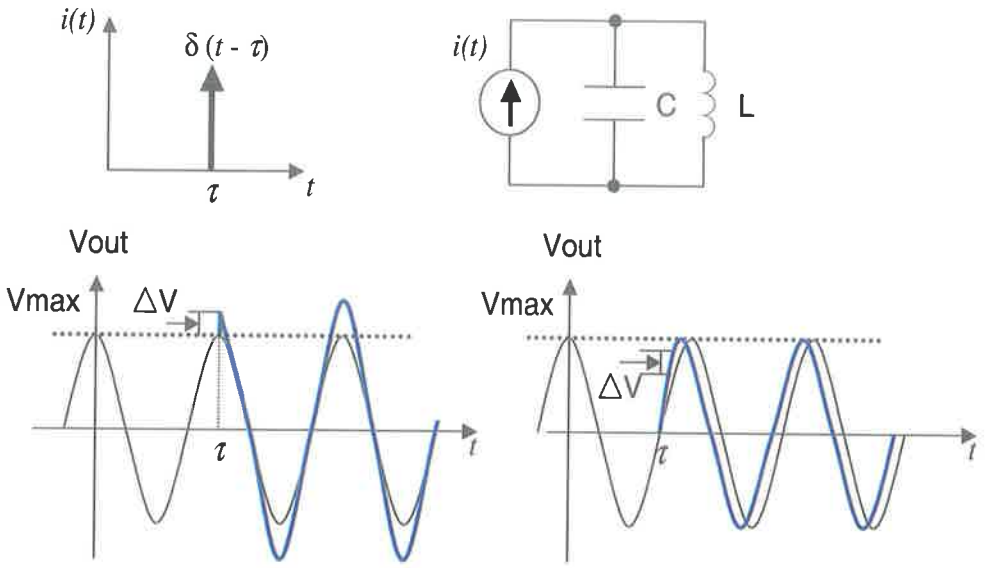


Figure 2.11: Instantaneous impulse response on amplitude and phase of an ideal LC oscillator.

If a current impulse is injected at the maximum voltage, only an amplitude change is occurred without phase shift. In case of the amplitude impulse response, AM noise is attenuated by a voltage limiter (i.e. automatic gain control (AGC)) or a nonlinear limiting mechanism of the oscillator by a tail current and a supply voltage. In RF systems, the output of an oscillator is amplitude limited before it flows into the input of a mixer.

On the other hand, there will be a maximum phase shift with a minimum effect on the amplitude will result if the injected current is applied at the zero crossing point as shown in Figure 2.11. Contrary to the amplitude impulse response, the excess phase is indefinitely sustained since the excess phase is not disappeared or extinguished by the AGC or the nonlinearity of the circuit. For these reasons, phase noise primarily contributes to the noise characteristic of the oscillator.

2.2.2 Phase Noise Model I - Linear Time Invariant Model

The semi-empirical (heuristic) model known as the Leeson-Cutler phase noise model [52] is based on an LTI system for an LC tank oscillator. This model predicts the phase noise ($L\{\Delta\omega\}$) to be:

$$L\{\Delta\omega\} = 10\log\left\{\frac{2FkT_a}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q_e\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}, \tag{2.10}$$

where F is an empirical parameter (known as "device excess noise number"), k is Boltzmann's constant, T_a is the absolute temperature, P_{sig} is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q_e is the effective Q factor of the tank including all of the loadings and $\Delta\omega$ is the offset angular frequency from the carrier and $\Delta\omega_{1/f^3}$ is the angular frequency of the corner between $1/f^3$ and $1/f^2$ region (as shown in Figure 2.12).

The equation for Leeson-Cutler model can effectively explain the typical phase noise characteristics in all of the three regions in Figure 2.12 assuming that F and $1/f^3$ are accurately known. However, the difficulty in predicting the phase noise performance using this model comes from the fact that F and $\Delta\omega_{1/f^3}$ are fitting parameters. In initial design status, these empirical parameters are seldom known since F excludes

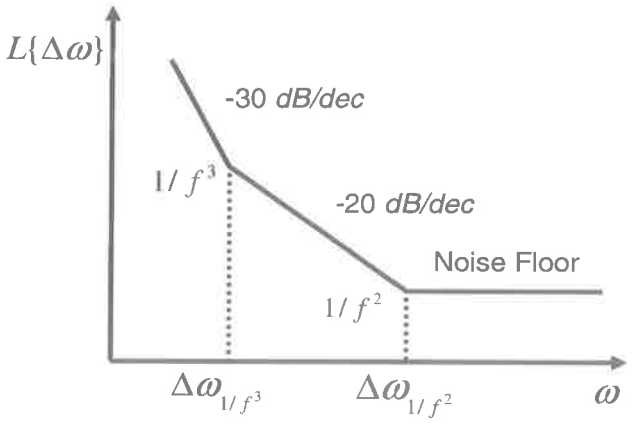


Figure 2.12: Typical plot of the phase noise of an oscillator versus carrier offset ($\Delta\omega$).

nonlinear frequency conversion effects and $1/f^3$ is not equal to the $1/f$ noise corner of the active devices. Furthermore, this phase noise model is based on a linear oscillator in steady state, which can explain a narrow range of phase noise in a practical case. Therefore, the model has a limited usage in estimating the phase noise performance for a discrete VCO design with a relatively high Q inductor.

2.2.3 Phase Noise Model II - Linear Time Variant Model

An oscillator in practice is characterized by time-varied nature periodically and modelled by a linear time-variant (LTV) system [53] (known also as Hajimiri model). This model quantifies the phase noise through applying a series of current impulses representing the noise sources of the integrated devices of the oscillator. The current impulses results in an instantaneous voltage change across the capacitor of the oscillator (no effect on the current through the inductor) and shift both of the tank amplitude and phase depending on the injected time. Subsequently, a small amount of the injected charge can be modelled as a linear relation with the resultant phase shift as:

$$\Delta\phi = \Gamma(\omega_0\tau)\frac{\Delta V}{V_{\max}} = \Gamma(\omega_0\tau)\frac{\Delta q}{q_{\max}}. \tag{2.11}$$

The function, $\Gamma(x)$, is called the impulse sensitivity function (ISF) of which impulse response can verify the conversion of the device noise in the oscillator to phase noise

more accurately. The ISF can be expressed as a Fourier series since it is a periodic function by:

$$\Gamma(\omega_0\tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n), \tag{2.12}$$

where θ_n is the phase of the nth harmonic and c_n is the coefficient at the nth harmonic. This noise model can also account for the upconversion of $1/f$ noise into in-phase noise (low-offset phase noise) and the noise folding of the oscillation frequency harmonics into phase noise. In particular, it is verified that the $1/f$ noise upconversion can be minimised through acquiring the minimum DC coefficient, c_0 of the ISF. Since the c_0 of the ISF depends on the symmetry of the output waveforms [53], a complementary $-G_m$ oscillator suppresses the upconversion more compared to non-complementary oscillators. It is due to this fact that the complementary $-G_m$ oscillator generates more symmetric waveforms assuming that both gains of N/P cross-coupled active devices are equal.

The shortcoming of the LTV model is likewise the LTI model in that both models lack a physical insight: First of all, a physical insight is lacked in the model. The LTV model adopts a complicated modelling method using a mathematical approach to explain the generation mechanism of phase noise. Accordingly, the model is not straightforward to practically explain the physical mechanism of phase noise. In particular, an optimised noise modulating function (NMF) to explain a noise by cyclostationary variation of operating points in cross-coupled MOSFETs is actually difficult to obtain. It is because the calculation is dominantly based on the minimization of DC coefficient of ISF at each node of the oscillator through its numerous iteration. In addition, flicker noise upconversion to phase noise cannot be clearly explained using this model. In common, accurate noise model for MOSFET devices are still not available for LTV systems including the LTI model.

To give a physical insight for phase noise, Rael and Abidi [54] introduces a physical process of phase noise dedicated in resonator-based oscillators. This process is based on the thermal induced noise of the LC resonator, tail current and cross-coupled pair including flicker noise upconversion. Compared to the Hajimiri model, it seems to be derived to explain the noise conversion mechanism more clearly on the basis of

the physical operation of differential LC oscillators. Meanwhile, it provides a clue for validity to filter the 2^{nd} harmonic, which is applied to the design of low noise oscillators presented in this research. This model will be described briefly in Chapter 5.
In this research, an approach to low phase noise of a differential LC oscillator is performed based on the LTV model with the physical understanding of phase noise conversion mechanism. In the next Chapter, symmetric on-chip inductors for high quality factor are designed based on 2.5 dimension modelling environment. The optimisation procedure and final inductors for targeting LC VCOs in Chapter 5 are introduced.

Chapter 3

On-Chip Planar Inductors for Low Phase Noise LC VCOs

In obtaining low phase noise LC VCOs, it becomes a key issue to reduce inevitable energy loss occurred in the LC-tank circuit. In particular, the tank Q is governed by the lowest Q factor among integrated components such as on-chip planar inductors and varactors inclusive of external components of LC VCOs. Since on-chip inductors generally exhibit a worst Q factor, high Q inductor design is essential for low phase noise LC VCOs.

In this chapter, an energy loss mechanism in on-chip inductors is explained and a variety of inductors which are currently being investigated are introduced. For the LC-tank inductor, symmetric planar inductors are designed and analyzed on 2.5D EM simulation environment in 0.5 μm UTSi SOS[1] CMOS process. These inductors are optimised with constrained sets for a single and quadrature LC VCO operating at 5.8 GHz in a given area.

3.1 Introduction

An inductor is a critical component of wireless RF systems, which have prompted a great deal of efforts towards high performance and high integration density. Since

[1]Peregrine Semiconductor Inc. (http://www.peregrine-semi.com/)

the successful implementation of on-chip inductors [55], inductances up to 20 nH are realizable in silicon-compatible IC processes using planar spiral geometries [56]. On-chip planar inductors are currently utilised in oscillators, amplifiers and filters along with impedance matching and transformation network.

3.1.1 The Definition of Inductor Q Factor

For passive devices, Q factor has a significant meaning to estimate the performance. This is because the performance of RF micro-systems such as low noise amplifiers (LNAs) and VCOs is related to the device quality.
In general, the Q factor of an inductor can be expressed as:

$$Q_L = \frac{\omega_L L}{R_{es}} = \frac{2\pi f_L L}{R_{es}}, \tag{3.1}$$

where Q_L indicates Q factor of the inductor, R_{es} is the effective series resistance of the inductor, L is the equivalent inductance of the inductor, ω_L is a radian frequency and f_L is the operation frequency of the inductor. R_{es} can be explained with the energy loss of the inductors due to the substrate loss, radiation of thermal energy and voltage drop in the inductor metal tracks. That is, the energy loss occurred in the inductor strips dominates the performance of the inductor. In terms of energy loss, Q factor can be also defined as:

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}}. \tag{3.2}$$

As indicated by Eq.(3.2), Q factor indicates how much energy is lost among the energy stored in an inductor per cycle when AC currents flow along the inductor.

3.1.2 Electromagnetic Loss Mechanism in On-Chip Inductors

In general, EM fields are formed as shown in Figure 3.1 when an AC current source is applied to the in/output ports of an inductor.
The fields are mainly translated into two parts:

- Electric fields by voltage difference along the spiral traces (→), between the metal tracks (→), and between a ground plane and the spiral strips (→)

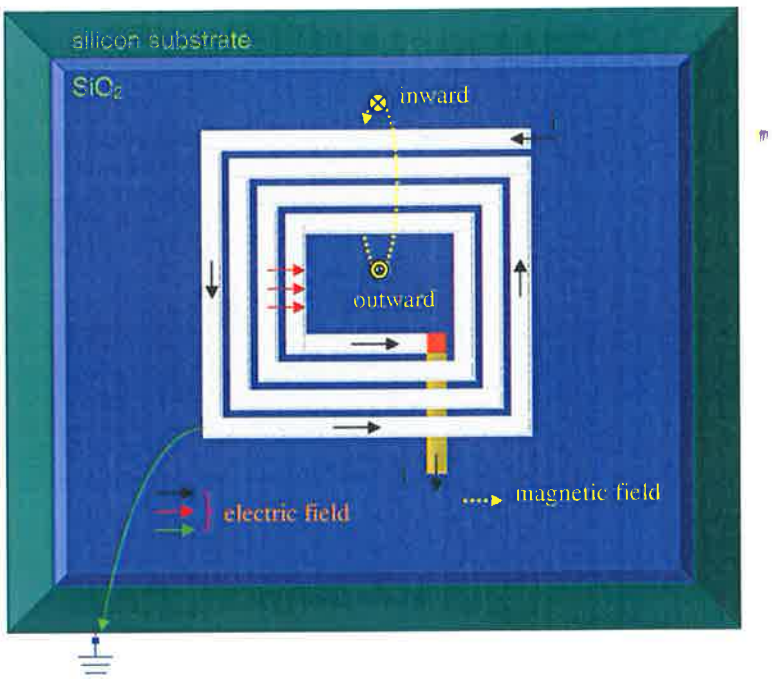


Figure 3.1: Electromagnetic fields of on-chip inductors on silicon substrate.

- Magnetic field by AC current signals flowing along the spiral traces (⇢)

Such EM fields formed in the monolithic inductor build up several types of energy losses. These losses are:

1. Ohmic Loss

   This loss occurs by resistive components of winding inductor strips which obstructs current signal flows (→) and produce voltage drops (⇢). It usually depends on the metalisation thickness and type of materials used in a fabrication process. Therefore, thick top metal layer and high conductive material such as copper (Cu) can be utilised for this purpose.

2. Capacitive Coupling Loss

   A path of capacitive coupling forms through the substrate (⇢) in that the substrate layer is generally grounded as described in Figure 3.1. This coupling effect can be diminished by utilizing the top metal layer of an IC manufacturing process

as well as a thick oxide far from the ground plane to reduce the parasitic capacitance. Taking these issues into consideration can improve inductor Q factor.

3. Magnetic Coupling Loss

This type of loss takes place by the following two physical phenomena.

- Skin Effect

  Since a current flows along the skin layer of the inductor tracks at high frequency (skin effect), the effective resistance of a conductive metal layer increases with regard to frequency increase. It is due to the fact that the effective area flowing current is reduced to skin depth. The formula for skin depth (η) is given by:

$$\eta = \sqrt{\frac{\rho}{\pi f \mu}}, \tag{3.3}$$

  where ρ is the conductivity of inductor metal strips, f is the operation frequency and μ is the relative permeability of the metal line[2]. Intuitively, the more the metal line is thickened, the more skin effect will be relatively alleviated. This implies that the width of inductor strips is critical to govern the Q factor in designing on-chip inductors.

- Eddy Current

  According to Maxwell's equations, time-varying magnetic field of conductors naturally induces a current flow (eddy current) given by:

$$\oint \vec{E} \bullet d\vec{l} = -\iint_{surface} \frac{\partial \vec{B}}{\partial \vec{t}} \bullet d\vec{S}. \tag{3.4}$$

  This eddy current is generated to a direction of protecting the change of the time-varying magnetic field. Also, the effect becomes more serious as frequency increases due to the fact that induced electric field is proportional to

[2]For instance, 75 μm metalisation thickness of 4.5×10^7 S/m conductivity at 1 MHz becomes 2.37 μm at 1 GHz.

the value of $\partial\vec{B}/\partial\vec{t}$. Therefore, this current gradually diminishes the magnitude of the magnetic field and inductance loss occurs. Figure 3.2 illustrates the eddy current in the substrate. Since such magnetic field concentrated

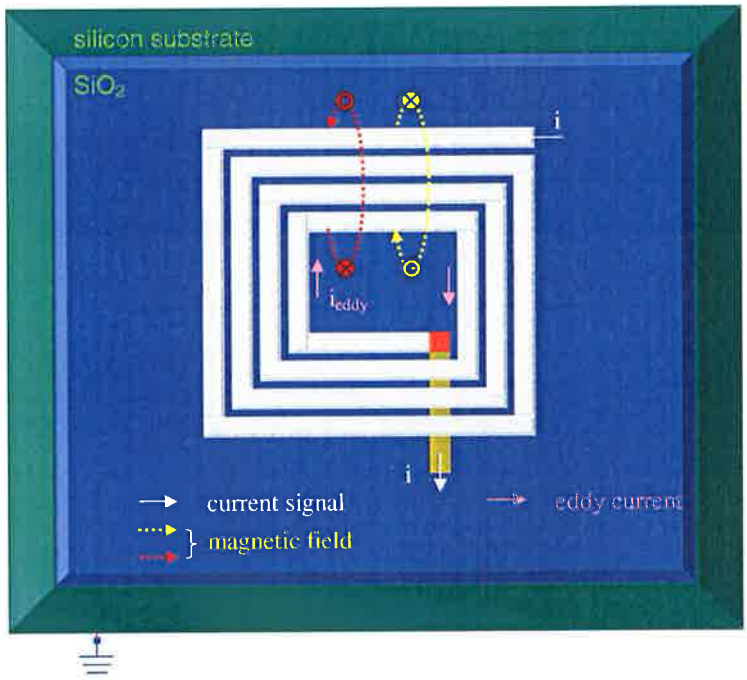


Figure 3.2: Eddy current in the substrate.

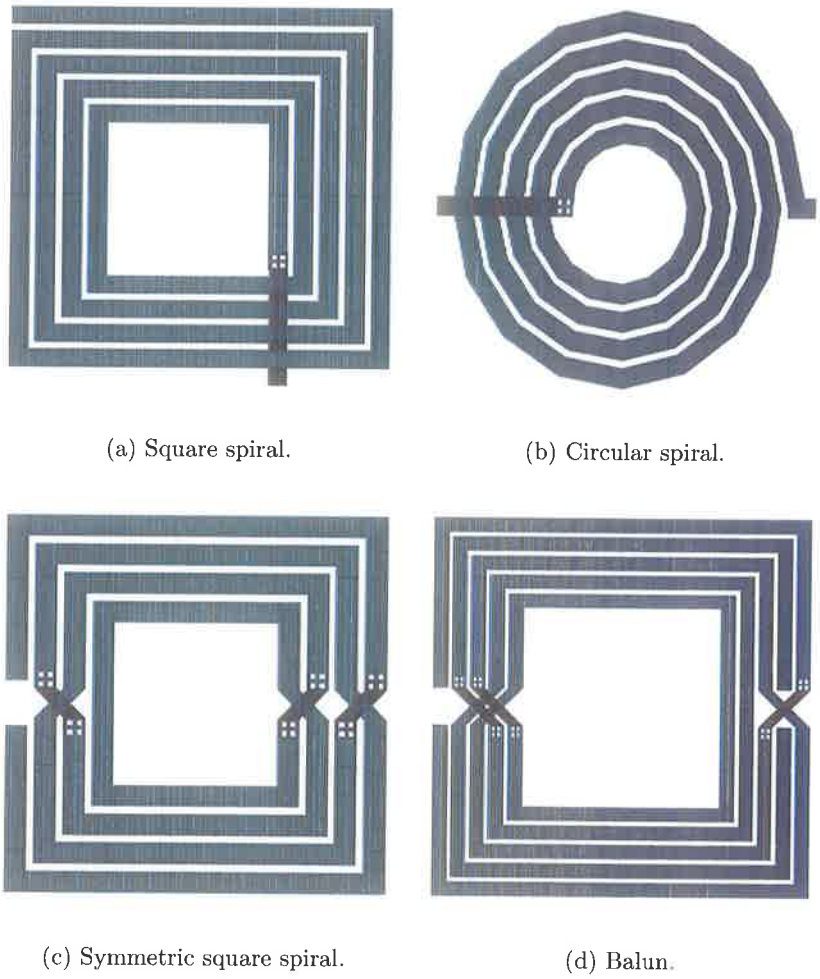
in the inner turns of the inductor induces eddy current below the inductor, energy loss with reduced inductance lowers Q factor. This can also explain a nonuniform current flow in the inner turns. To diminish undesirable effects by this current, hollowing the inner turns can be considered[3].

3.2 Integrated Inductors

In this section, configurations of integrated inductors under investigation are introduced in terms of merits and demerits briefly.

[3]For high frequency RF IC applications, this effect becomes less significant due to low inductance requirement.

ential / suspended inductors are also utilised to improve Q factor. Figure 3.6 describes typical monolithic inductors.



(a) Square spiral.

(b) Circular spiral.

(c) Symmetric square spiral.

(d) Balun.

Figure 3.6: On-chip planar inductors.

In general, an on-chip inductor based on silicon substrate of typical 1-100 Ω-cm resistivity suffers from energy loss by magnetically induced current. In order to diminish such effects, patterned ground shield (PGS) [42] is suggested to lessen magnetic loss through adopting grounded shields with patterned metal film. However, the finite shield resistance works as a factor of additional energy loss and

lower inductance. It also causes an image current induced by magnetic field below the ground shields.

A multi-level layer inductor [59] enables smaller occupied area, higher Q factor and increased inductance in a given area. In case of dual metal-layer inductors, the total metal resistance approaches nearly twice that of single metal-layer inductors. On the other hand, the overall inductance can reach four times, providing that magnetic coupling between dual metal layers has no loss. Accordingly, Q factor of dual metal-layer inductors becomes twice that of single metal-layer inductors from the definition of Q factor by:

$$Q_{\text{dual}} = \frac{4\omega L}{2R_{es}} = 2\frac{\omega L}{2R_{es}} = 2Q_L. \tag{3.5}$$

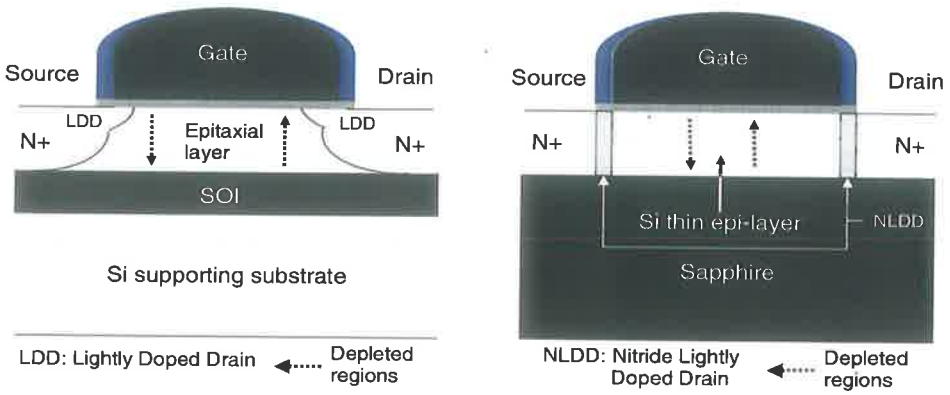
In reality, however, the Q factor is affected by the non-uniform resistance of each metal layer, which usually has different metal thickness depending on the metal-level. In addition, the parasitic and interwinding capacitance to the substrate layer tend to increase. Consequently, it is necessary to pass an additional post-processing step in fabrication process to increase resistivity of high-conductive silicon substrate. Via arrays can be utilised for reducing interconnection resistance between multi-level metal layers while simulation time and design complexity of the inductor structure are quite increased.

On the other hand, a symmetric on-chip inductor [44][60] is investigated to demonstrate benefits to acquire a higher Q factor than other single-ended (asymmetric) inductors. In particular, it can provide a favourable inductance at a given area by strong mutual inductance. Since a top-level metal layer is mainly utilised for the symmetric inductor, it is advantageous to lower the metal resistance assumed the thick top-level metalisation is provided. UTSi SOS process supports the thick top metal layer, which is three times compared to typical top metal thickness of general digital CMOS processes. In this thesis, the symmetric inductor (also known as differentially excited inductor) is researched to obtain a high Q factor at high frequency on sapphire substrate. Further details are presented in the next section.

3.3 Monolithic Inductor Design

3.3.1 Silicon-on-Sapphire Substrate

As mentioned in Section 3.1.2, a conductive substrate such as in bulk CMOS processes works as a critical factor for energy loss. Accordingly, breakthroughs for avoiding or lessening energy loss by EM field effects are quite necessary. On this account, SOI process, especially SOS process offers advantages of low substrate loss caused by high resistive sapphire material and low capacitive coupling to the substrate. Compared to separation by implantation of oxygen (SIMOX)-SOI process, UTSi SOS process provides a thick sapphire substrate that constitutes the whole substrate layer on which a thin epitaxial film is deposited. Figure 3.7 illustrates NMOS structures in the two representative SOI processes.



(a) SIMOX-SOI NMOS.

(b) UTSi-SOS NMOS.

Figure 3.7: SIMOX-SOI and UTSi SOS NMOS FET structures.

General silicon dioxide (SiO_2) film has a loss tangent[4] of around 0.005 in contrast to the smaller value of < 0.0001 for sapphire material at 3 GHz [61]. Hence, higher loss occurs in SOI substrate when a thin dioxide layer is exploited instead of the thick sapphire substrate. In addition, the improved isolation and lower self-heating effects by

[4]Loss tangent indicates how much electromagnetic waves get damaged when passing through a dielectric material.

high thermal conductivity (sapphire: 0.46 W/cm·K, SiO_2: 0.014 W/cm·K) [62] provide advantages of reduced signal interference and alleviation of lowering inductance in integration of monolithic inductors. Considering the characteristic of the thick sapphire film, magnetic loss, which is serious in bulk substrate at high frequency, does not occur because of the nearly perfect insulating material. Therefore, induced currents are negligible in the substrate layer. Since passive micro-components can be formed on field oxide (FOX) region [63], on-chip symmetric inductors in this research are designed without the thin silicon epitaxial layer.

3.3.2 Metalisation Modelling for Quasi-3D EM Simulation

General three dimension (3D) EM field simulation can be used to obtain accurate simulation results close to expected measured values. However, it requires a long simulation time and a large physical memory due to the need of processing large quantities of data. Meanwhile, 2.5D simulation methodology can support an enough accuracy with less computational resources.

2.5D stands for a stacked structure with 2D infinite planes. Consequently, integrated components necessary to model partial dielectric layers such as transistors or on-chip capacitors are ineligible in 2.5D modelling method. Furthermore, all of the metal layers are regarded as thin conductive layers. Such a modelling environment may cause undesirable effects in performance estimation of the integrated inductors owing to a substantial coupling effect between the side-walls of the metal tracks. It becomes a critical factor if the metal strips of typical on-chip inductors are configured in the same thickness like the turn spacing[5]. In 2.5D EM simulation environment, accordingly, it is preferable to remodel all of the metal layers into two identical metal layers with an air layer as shown in Figure 3.8. This approach will be referred to as quasi-3D modelling. Each metal layer is modelled as a pair of identical metal strips with half thickness of the original metal layer. Between the divided metal layers, an additional air layer of relative permittivity ϵ_r=1 is inserted with the same thickness of the metal layers [64]. Figure 3.9 demonstrates metal configurations derived from 2.5D and quasi-3D modelling methods.

[5]This phase can be neglected if the spacing between metal traces is much larger than the thickness of metal layers.

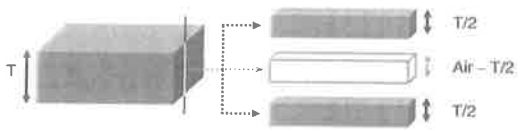
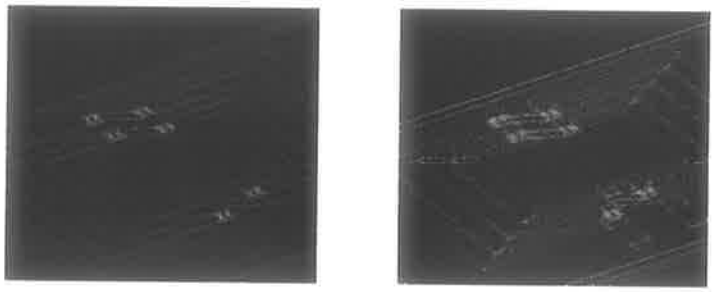


Figure 3.8: Metal configuration for quasi-3D modelling (T: metal thickness).



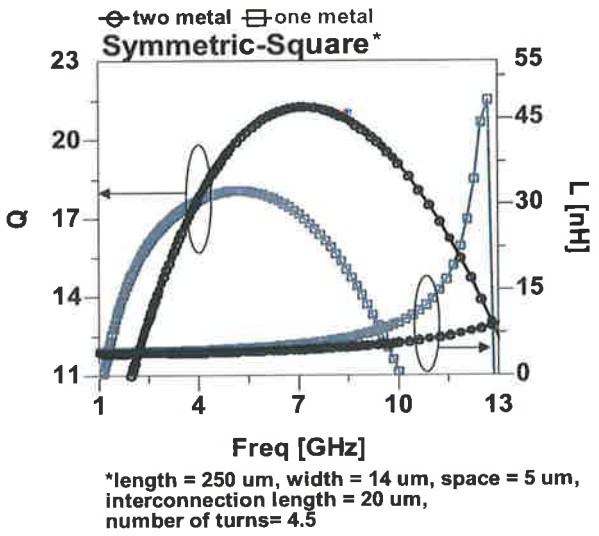
(a) 2.5D modelling. (b) Quasi-3D modelling.

Figure 3.9: Configuration of a symmetric-square inductor in 2.5D/quasi-3D modelling.

The approach to quasi-3D metal modelling can more effectively explain the dependency of the series resistance (R_s) on frequency variation. It is due to the fact that the currents flowing along the metal traces crowds into the skin layer as the frequency increases according to skin depth. Comparison with the EM simulation results of a symmetric inductor using only one metal layer and two identical metal layers is illustrated in Figure 3.10.

This figure shows the Q factor obtained from the 2.5D modelling demonstrates a lower value compared to the case adopting the two metal modelling method. It is due to the fact that the metal strips relatively come to exhibit a lower thickness at the same frequency. In addition, a larger capacitance by the lower thickness between the thin metal traces are more reflected onto the simulation results. In consequence, the self resonant frequency (F_{srf}) of the inductor starts to decrease. Hence, the quasi-3D modelling for metalisation can consider the effective metal depth, which affects the evaluation of an accurate Q factor under 2.5D EM simulation environment.

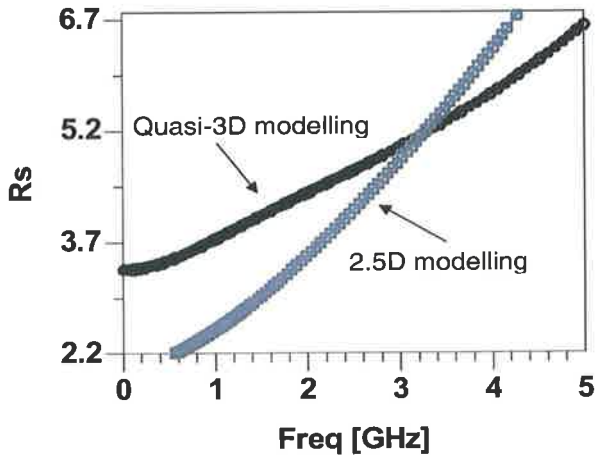
UTSi SOS process (0.5 μm 3-metal/1-poly) layers are shown in Figure 3.11 with thick-



Since the sidewall capacitance in 2.5D modelling (one metal) is more reflected into the simulation result due to the thinner metal thickness, the highest Q factor with the self-resonant frequency is shifted to lower frequency band compared to the result using quasi-3D modelling (two metal).

Q : quality factor
L: inductance

(a) Q factor.



Because of increased metal thickness by the internal air layer of quasi-3D modelling, Rs in 2.5D modelling has a higher value at high frequency. Therefore, it affects Q curve variation between the modelling methods as shown in Figure 3.10(a).

(b) Series resistance (R_s).

Figure 3.10: Comparison of Q factor and R_s of a symmetric-square inductor.

ness, conductivity, relative permittivity of each metal and dielectric layer. The metalisation configuration introduced for quasi-3D modelling in Section 3.3.2 is illustrated in Figure 3.12.

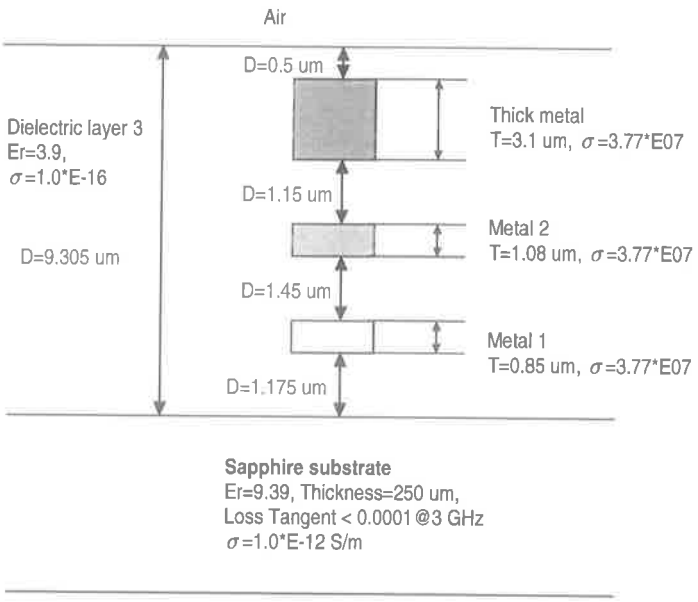


Figure 3.11: UTSi SOS process layers in cross section.

3.3.3 Differentially Driven Symmetric Inductors

Symmetric inductor type [44] exploits a pair of asymmetric inductors using mainly top-level conductors. Figure 3.13 shows a typical symmetric inductor with current signal flows.

Such a symmetric inductor is formed with symmetrical interconnection of two identical spiral (asymmetric) inductors through several cross-over and cross-under connections centering around a common node. As illustrated in the Figure 3.13, a pair of asymmetric spiral inductors with 2 turns consist of a symmetric inductor of 4 turns in which signal currents (i_1, i_2) flow in the same direction. Common node for center-tapping [60] can be connected to ground plane to acquire symmetric substrate parasitics[6]. As can be expected, stronger mutual coupling between adjacent conductor strips increases the inductance in the given area. Contrary to the case connecting two asymmetric inductors in series horizontally, the symmetric inductor can provide an advantage of space efficiency. It is due to reducing the mutual coupling between the pair. As a result,

[6]It can be connected to supply voltage for biasing active devices.

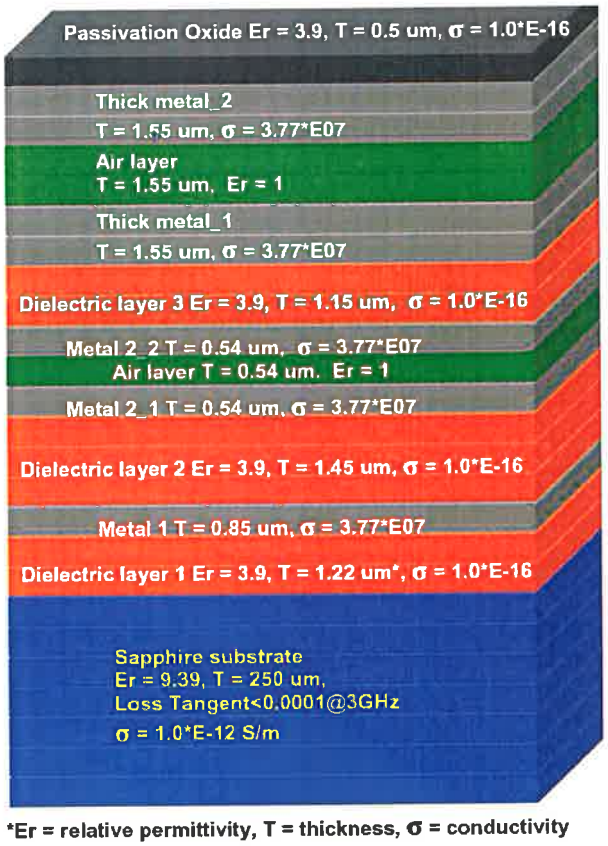


Figure 3.12: Modified metalisation in cross section for 2.5D EM simulation.

a symmetric on-chip inductor can realize high inductance and chip area efficiency by replacing two identical inductors with a single coil.

Q Enhancement Mechanism of A Symmetric Inductor

Since the voltage phase between the two input ports of the symmetric inductor is out of phase by 180°, a current path (- - →) is formed along an equivalent pi (Π) network as illustrated in Figure 3.14.

Z_{d1} and Z_{d2} represent an equivalent of silicon dioxide, substrate capacitance and substrate resistance. They are connected in series and generate an effect of deriving higher impedance path in substrate layer compared to a single-ended inductor. In particular,

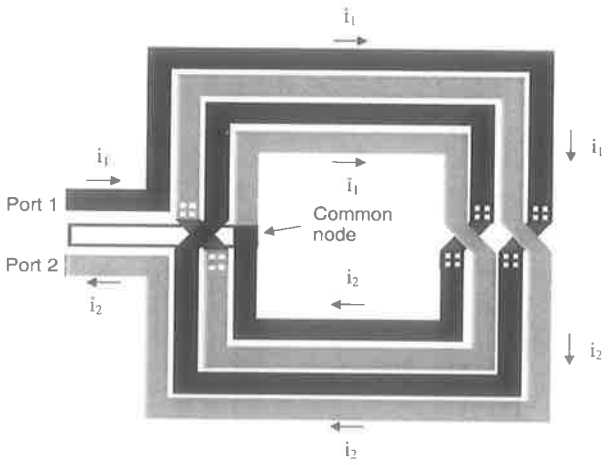


Figure 3.13: Top view of a symmetric square inductor with current flow.

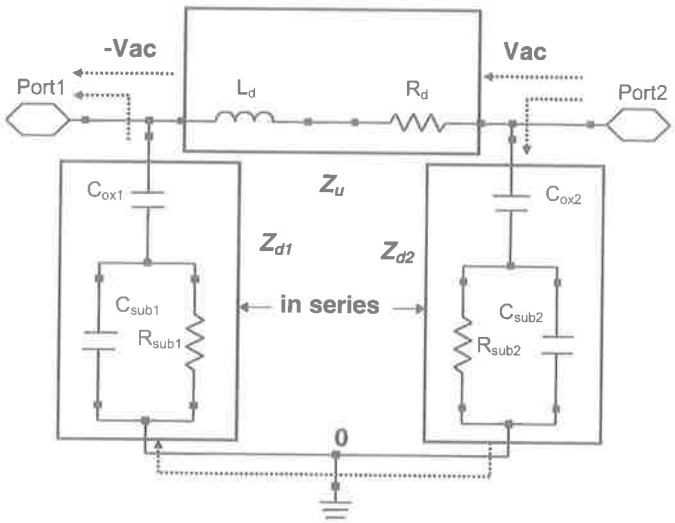


Figure 3.14: Current path in the lumped model of a symmetric on-chip inductor.

such advantageous effect clearly appears at high frequency bands rather than at low frequency. The detailed analysis demonstrated in Appendix A shows that magnetically induced current into the substrate is reduced at high frequency and hence the inductor Q factor increases.

Small Signal Models of A Symmetric Inductor

In order to extract lumped model parameters of the symmetric inductor, it is necessary to induce a small signal model which has a physical meaning in narrow frequencies. This lumped equivalent circuit is required to estimate the large-signal performance of integrated inductors and derived for CAD purposes such as co-simulation with active devices and other integrated components.
Single-ended inductors are generally excited by AC source at one port while the other port is grounded or connected to supply voltage. Figure 3.15 demonstrates a simplified small signal model of the inductor.

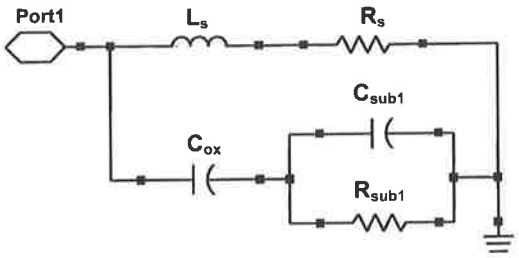


Figure 3.15: Small signal model of a single-ended inductor.

Contrary to the single-ended inductor, a symmetric inductor is driven by differential voltage signals from the two input ports and consequently, the equivalent lumped model of the symmetric inductor can be illustrated as in Figure 3.16.

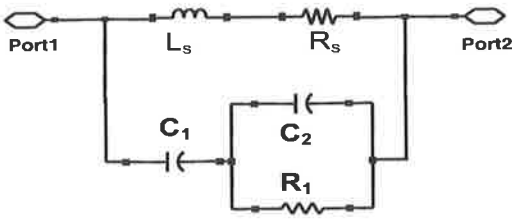
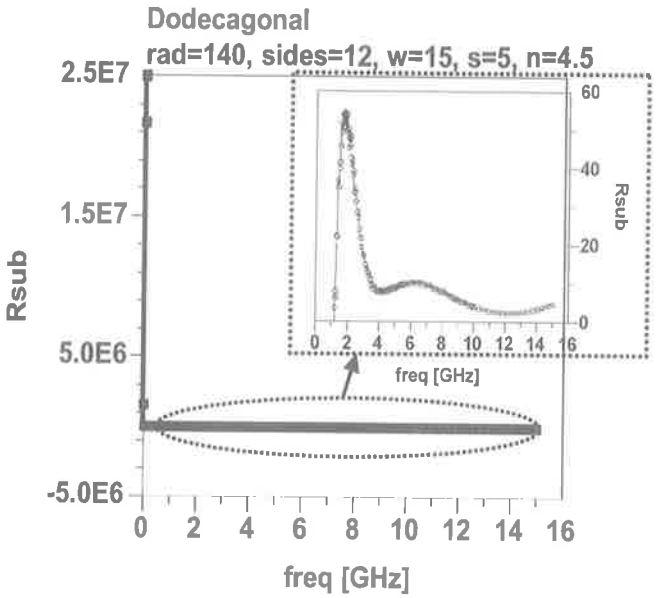


Figure 3.16: Small signal model of a symmetric on-chip inductor.

Since sapphire is nearly a perfect insulating material, substrate loss can be negligible [46] as mentioned in the previous section. However, induced substrate loss in the sapphire substrate can be observed at radio frequency as shown in Figure 3.17 by EM

simulation. In other words, substrate energy loss is unavoidable as long as the loss tangent of the sapphire material is not zero. The inner figure of Figure 3.17 is magnified showing the substrate resistance at high frequency.



As shown in the magnified figure, energy loss in sapphire substrate can be induced by small resistive components at high frequency. It is due to the fact that the sapphire material is not a perfect insulator.

Figure 3.17: Substrate resistance (R_{sub}) in UTSi SOS process.

Therefore, the substrate resistance (R_{sub}) can be considered for an accurate physical modelling of the symmetric inductor.

The lumped model parameters in Figure 3.16 can be extracted from differential S-parameter [44] as follows.

$$S_d = S_{11} + S_{22} - S_{12} - S_{21} \tag{3.6}$$

$$Z_d = Z_{11} + Z_{22} - Z_{12} - Z_{21} = 2 * Z_o\left(\frac{1+S_d}{1-S_d}\right) \tag{3.7}$$

$$Q_d = \text{Im}(Z_d)/\text{Re}(Z_d) \tag{3.8}$$

$$L_d = \text{Im}(Z_d)\frac{1}{\omega} \tag{3.9}$$

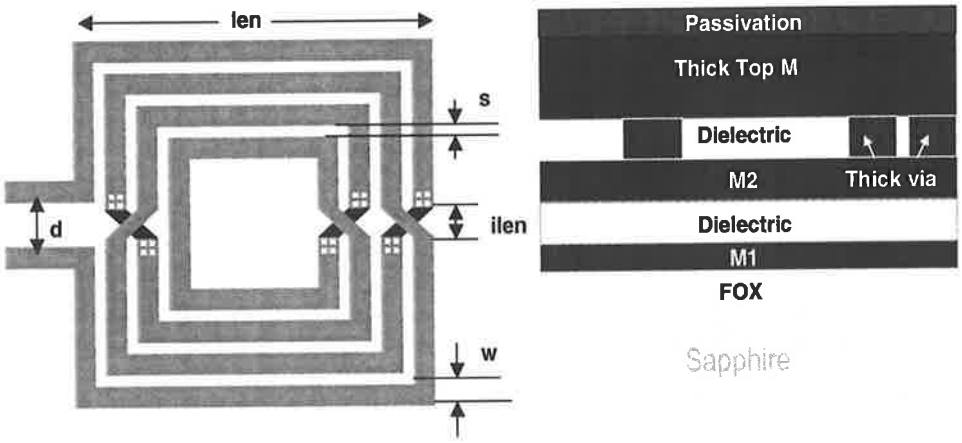
$$R_d = \text{Re}(Z_d), \tag{3.10}$$

where S_d and Z_d indicate differential S-/Z-parameters to derive the Q factor of the differential system (i.e. the symmetric inductor). Z_o is known to be characteristic

impedance and typically is 50 Ω. Also, L_d and R_d are the series inductance and resistance of the inductor, respectively. The derivation of the lumped model parameters is further discussed in Appendix A.

Design Parameters of Symmetric Inductors

Using the thick top-level metal layer of UTSi SOS process, symmetric inductors are designed and simulated on 2.5D EM field simulator of Momentum integrated in ADS[7]. As for the design parameters, one-side length/radius (**len**/**rad** for symmetric square and circular inductors, respectively), spacing (**s**), width (**w**), interconnection length (**ilen**) of cross-over/under metal layers and distance between two input ports (**d**) are to be considered as shown in Figure 3.18(a). Figure 3.18(b) shows the corresponding cross sectional view.



(a) Design parameters. (b) Cross-section view.

Figure 3.18: Design parameters of a symmetric-square inductor with the cross-section view.

Since the parasitic capacitance is proportional to the number of turns, the dimensions of the inductors are adjusted or limited to set an inductance value for the targeted

[7]http://eesof.tm.agilent.com/

frequency of 5.8 GHz LC VCO. The number of the metal turns (**n**) is set to 4 in order to obtain 3.5–5 nH inductances as an initial design value.

3.4 Simulation Results

EM simulation using the metalisation modelling method introduced in Section 3.3.2 is performed to validate Q factor estimation for symmetric inductors. To estimate the inductance of symmetric inductors, ASITIC [65] is exploited before EM simulation using the metalisation structure in Figure 3.12. The technology file for the symmetric inductors in UTSi SOS CMOS process is listed in Appendix B.

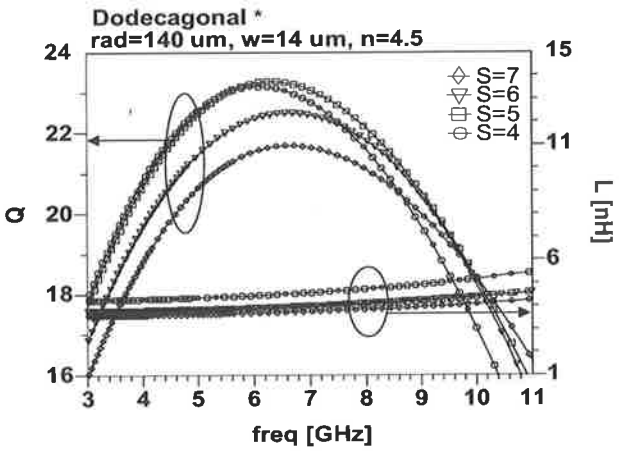
Generally, minimum spacing for asymmetric inductors is needed to keep maximizing magnetic coupling at low frequency while a larger spacing is required at high frequency owing to proximity effect and magnetic coupling [56]. To obtain initial startup parameters for symmetric inductors design, EM simulation is performed on asymmetric-dodecagonal inductors with regard to spacing and width variations as shown in Figure 3.19.

In the given geometry with optimum spacing (**s** = 5 μm) and width (**w** = 14 μm) at highest Q factor in Figure 3.19, the simulation results in Figure 3.20 are obtained by spacing variation from 5 μm to 8 μm for symmetric square inductors.

A usable frequency bandwidth (i.e. F_{srf}) is increased as the spacing increases, while the highest Q factor at 7 μm spacing starts to decrease. Contrary to typical asymmetric inductors, Figure 3.20 shows a wider spacing than the minimum spacing is required to achieve higher Q factor for symmetric inductors. In addition, the inductance is gradually diminished by decreased magnetic coupling as the spacing increases.

The next simulation results shown in Figure 3.21 are obtained by varying metal width for higher Q factor.

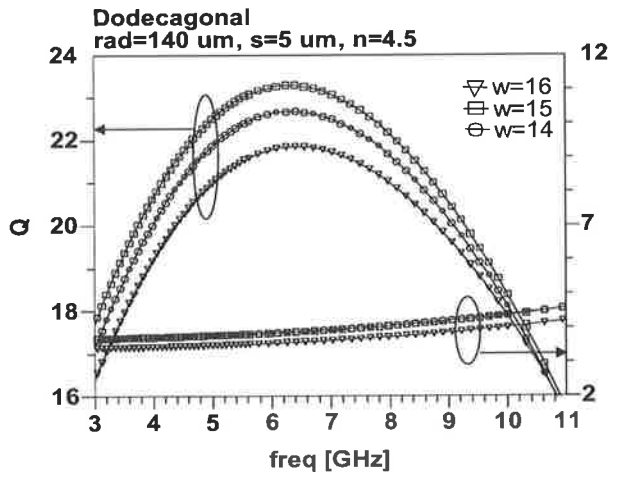
Due to the fact that the vertical length and horizontal width of the symmetric inductors in Figure 3.21 are fixed, the distance between opposite sides becomes close as the width increases. As a result, the negative mutual coupling is increased in the centre area and the inductance is dropped by the increased negative mutual coupling. In addition, since a wider conductor strip causes a higher skin effect by nonuniform current [66],



These simulation results demonstrate: a) asymmetric inductors exhibit the highest Q factor at the minimum spacing (s).

* indicates these inductors have 12 angles.

(a) Spacing variation.



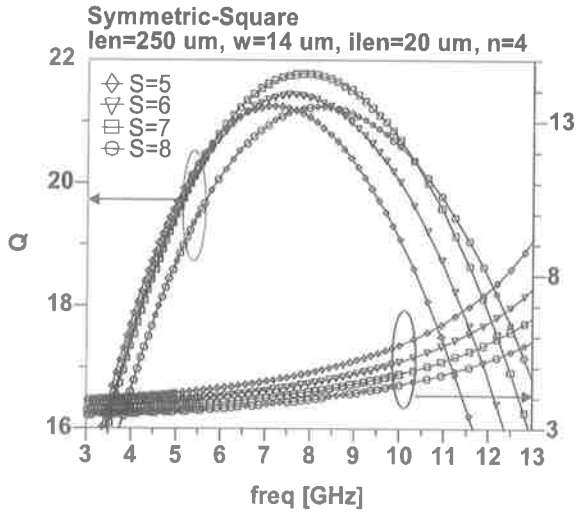
These simulation results demonstrate: b) the width (w) of the inductors can be used to adjust the Q factor significantly. It is due to nonuniform current by skin effect at high frequency.

(b) Width variation.

Figure 3.19: Q factor of the asymmetric-dodecagonal inductors with regard to spacing and width variations.

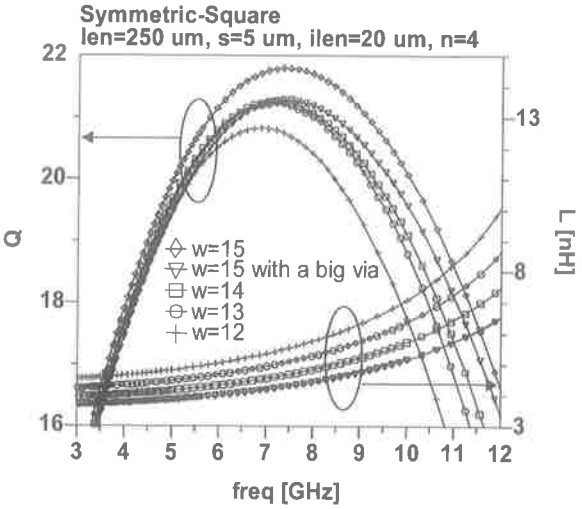
15 μm is used as the maximum width in a given layout area. As the metal strip width increases, F_{srf} is decreased with Q factor by the increased resistance.

In this research, all inductor designs are consistent with UTSi SOS design rules including via layers. Meanwhile, another EM simulation is conducted for the inductor with



Contrary to the case of asymmetric inductors, the highest Q factor occurs at wider spacing than the minimum value in the given geometry of the symmetric inductors.

Figure 3.20: Q factor of the symmetric square inductor as a function of spacing.



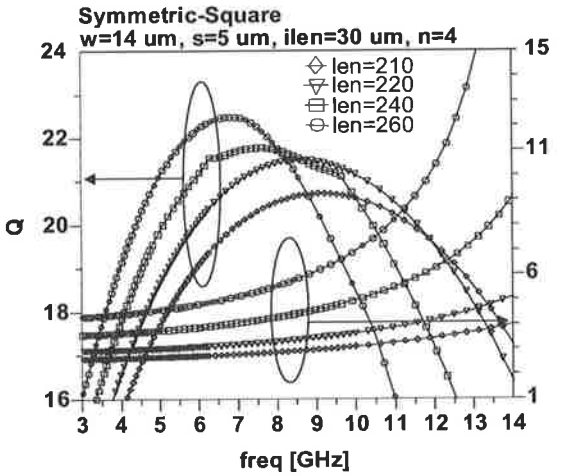
This simulation demonstrates that the Q factor of the symmetric inductors is much dependant on the width variation as in case of asymmetric inductors. It is due to the fact that the range of Q factor variation is wider compared to the simulation results by spacing variation.

Figure 3.21: Q factor versus operation frequency according to width variation.

a square via which is larger than the typical via to take its effect into consideration. Contrary to an expectation for a better performance by reduced via resistance, the symmetric-square inductor adopting the typical via exhibits a slightly higher Q factor in UTSi SOS process as shown in Figure 3.21.

Figure 3.22 illustrates the Q factors dependance on dimension variations of symmetric-

square inductors.



As each side of the length (len) is increased, it is shown that Q factor is improved by reducing negative mutual coupling effect and eddy current flowing along the metal strips in the centre area.

Figure 3.22: Comparison of Q factor depending on length variation in symmetric-square inductors.

According to Craninckx and Steyaert [41], eddy currents are generated at high frequency in the center of monolithic inductors. Consequently, it is desirable to widen the empty centre for the purpose of high Q factor. Figure 3.22 demonstrates improved Q factors are obtainable as the hollow center of the symmetric-square inductors are widened. From this result, hollowing the center will be utilised for negligible effect on the inductor Q for LC VCOs to be presented in Chapter 5.

EM simulations by varying the interconnection length (**ilen**) are performed to validate its effects on Q factor as depicted in Figure 3.23.

The minimum length of 20 μm can be applied to interconnect cross-over/under metal interconnections in the given geometry. The simulation shows that the Q factor is gradually increased from 20 μm to 40 μm **ilen** while it is continuously diminished until 60 μm. As the **ilen** value increases, cross-over and cross-under metal interconnections in Figure 3.23 become more perpendicular and negative mutual coupling effect is gradually weakened. As a result, inductance is steadily increased by the Greenhouse formula [67]. Meanwhile, a magnetic field becomes asymmetric since the symmetric inductor is transfigured to an elliptical geometry by the increased interconnection length. This has influence on magnetic distribution in the symmetric inductor and

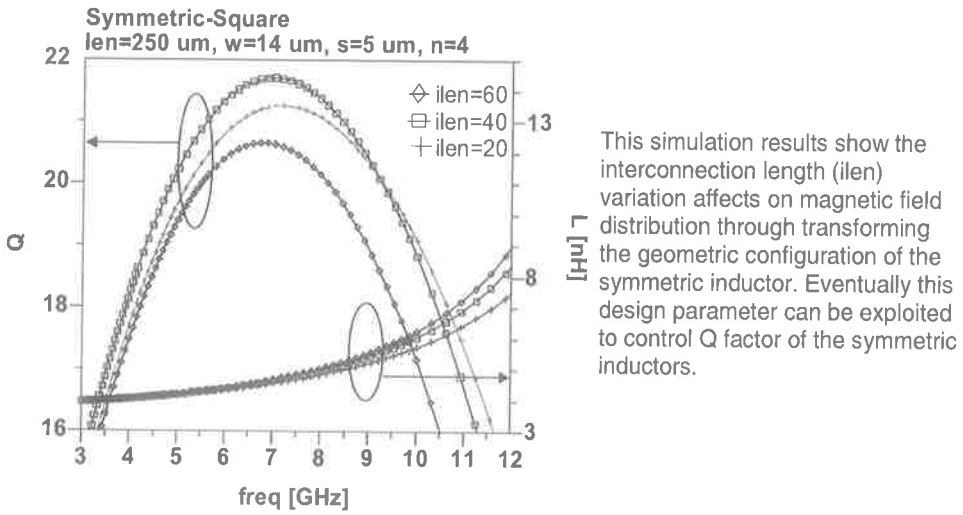


Figure 3.23: Q factor depending on **ilen** variations in symmetric-square inductors.

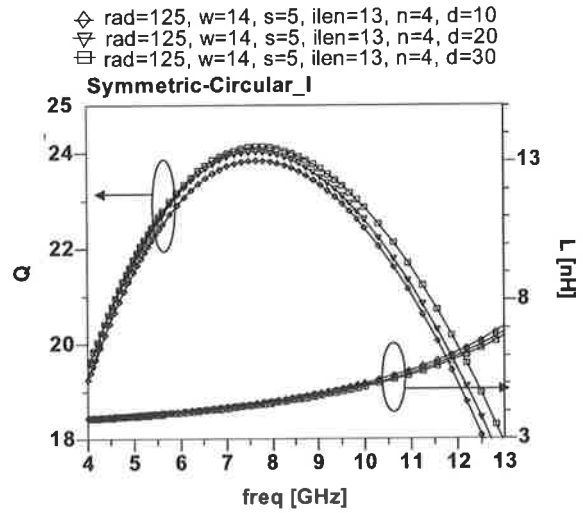
causes undesirable effect on Q factor. Therefore, this simulation result manifests the interconnection length can be used as a factor to adjust Q factor.

On the basis of the previous simulation results, optimisation is conducted with symmetric circular inductors (Strictly speaking, these symmetric inductors have 12 angles). The design parameters of **space/width/ilen** are varied while a horizontal width of 250 μm and a vertical length of 287 μm are fixed with 4-turn. To confirm the effect of the distance between the two ports, EM simulation is performed with **d** parameter. By enlarging the **d** parameter, Figure 3.24 shows the inductance is gradually decreased because of a shorter metal trace as frequency of operation increases.

In addition, Q factor is increased by reduced effective resistance of the metal strips in that negative mutual coupling by differential voltages of 180° out of phase becomes diminished. At the given geometry, the simulation shown in Figure 3.24 supports **d** effect on the Q factors and inductances is negligible. Therefore, **d** is set to 30 μm for symmetric-circular inductors.

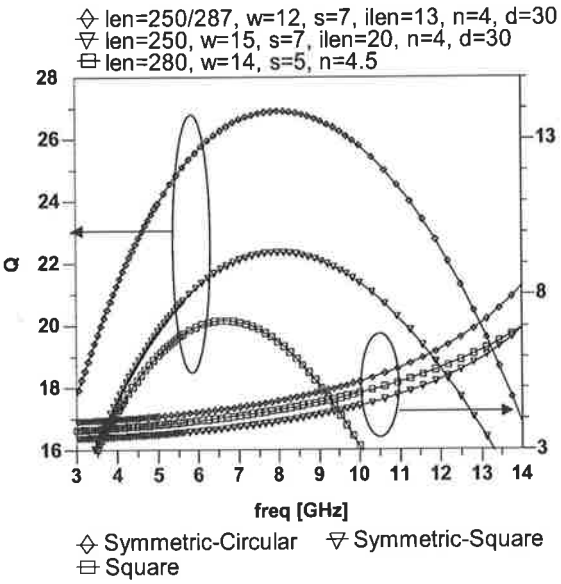
Figure 3.25 compares the Q factors among the optimised square/symmetric-square/symmetric-circular inductors.

As clearly indicated, a symmetric circular inductor can provide the highest Q factor compared to other kinds of planar inductor types. The symmetric-circular inductor is



This simulation shows that the distance variation between the two ports have a negligible effect on the Q factor.

Figure 3.24: Q factor dependance on distance parameter variation in symmetric-circular inductors.



The design parameters on top of this figure indicate the optimised values for each inductor at the highest Q factor. From this figure, the symmetric inductor, particularly the symmetric circular inductor enables area efficient inductance and higher Q factor compared to the asymmetric inductor.

Figure 3.25: Comparison among square/symmetric-square/symmetric-circular inductors.

configured at the highest Q factor as shown in Figure 3.26.

The performance of such symmetric-circular inductors are compared with literatures

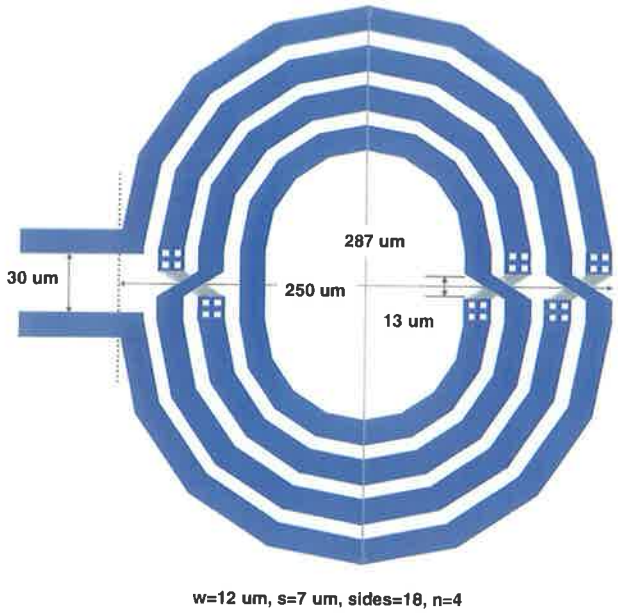


Figure 3.26: Most optimised symmetric-circular inductor layout with the design parameters.

as shown in Table 3.1.

Table 3.1: Comparison of a variety of inductors in literature. ($\mathbf{T_m}$: metal thickness, ρ_{wafer}: substrate resistivity)

Inductor type/substrate	ρ_{wafer} **(Ω-cm)**	$\mathbf{T_m}$	**L (nH)**	Q_{peak} **/GHz**
Multi-layer (2-metal) [68]	1–10	3 μm (Cu)	4	13.1/5.65
Multi-layer (3-metal) [43]	12	4.3 μm	2.2	16/2
PGS [42]	11–19	2 μm	7.4	6.76/2
SOI [69]	10 k		2.60	11.3/5.3
GaAs-multi-layer (2-metal) [70]	30	2/1 μm (Au)	4.9	35.9/4.7
symmetric-circular [this work]	$\mathbf{10^{-14}}$ **[62]**	**3.1 μm (Al)**	**4.4**	**26.9/8**

3.5 Final Symmetric Circular Inductor Design for 5.8 GHz LC VCO

Contrary to asymmetric inductors, a rule dominating the Q factor of the symmetric inductors cannot be easily induced. It is because two identical asymmetric inductors interact with each other in EM fields depending on their geometrical configurations. However, it clearly can be said that circular symmetric inductors are advantageous to obtain higher Q factor on the basis of the S-parameter simulation results.

In designing integrated inductors, the design procedure is closely related to the overall design process of the LC VCO. It is owing to the fact that the LC tank capacitance is correlated with the parasitic capacitances of adjacent active devices, integrated inductor including tank varactors and interconnecting metalisation. In particular, it is difficult to accurately estimate the interconnection parasitic capacitance in the initial design process. This is because the fact that the fundamental frequency obtained from 2.5D modelling deviates by nearly 700 MHz compared to the simulation results of the LC VCO schematic. Furthermore, tuning the dimensions of the integrated inductors is performed only in narrow range since a large finger number in active devices can be unavailable for high frequency applications due to increased tank capacitance. Hence, it is necessary to consider the parasitic capacitance variation in the inductor design when the layout configuration of the LC VCO is changed.

As for the final inductor design, it is desirable to hollow the inner space of the inductor to reduce mutual negative coupling for high Q. In order to move the highest Q point to the operation frequency of the LC VCO targeted in the research, the dimensions of the inductors are needed to be much larger than the current geometries as demonstrated in Figure 3.22. However, since it is related to increased inductance with an issue of chip area efficiency, it becomes limited to a certain value by a designer depending on the operation frequency. In consequence, a method to reduce the number of inner turns can be chosen with a shrunken radius to adjust Q factor and inductance.

Figure 3.27 illustrates the Q factors and inductances of the two final symmetric inductors altogether with the optimised circular inductor with 4 turns.

At the given geometry of 12 μm width and 7 μm space, the total number of turns

Chapter 4

Silicon-on-Sapphire MOSFET Varactor

As an integrated component of an LC tank circuit, a varactor (which is originated from a **var**iable cap**acitor**) also has a key part in the phase noise performance of an LC VCO. Such a varactor is mainly classified into three types of a P/N junction diode, switched capacitor and MOSFET. Recently, the MOS varactor is becoming widely used for better phase noise performance and easier implementation. This chapter focuses on the role and characteristic of the MOS varactor including an SOS MOS varactor. In addition, it introduces a procedure to obtain an optimum varactor Q. Co-simulation for high Q tank is performed with the most optimised inductor presented in Chapter 3 on the basis of 0.5 μm UTSi SOS MOSFET models.

4.1 Introduction

In general, the oscillation frequency of LC VCOs is determined by the combination of effective inductance and capacitance in the LC tank. Since a passive inductor is not suitable to vary its inductance electrically, it is necessary to apply a capacitor which has an ability of tuning the capacitance.

Provided that total charge of the capacitor has the following characteristic [71],

$$q(v) = c_i v + c_l v_l \ln\left[\cosh\left(\frac{v - v_i}{v_l}\right)\right], \tag{4.1}$$

where c_i and v_i are an initial-bias capacitance and voltage, respectively and c_l indicates an increased capacitance when v_l is applied to the capacitor. The charged capacitance can be calculated from the charge-conserved model as in Eq.(4.2). Since $C(v) = dq(v)/dv$,

$$C(v) = \frac{dq(v)}{dv} = \frac{d}{dv}\left(c_i v + c_l v_l \ln\left[\cosh\left(\frac{v - v_i}{v_l}\right)\right]\right) = c_i + c_l \tanh\left(\frac{v - v_i}{v_l}\right). \tag{4.2}$$

The capacitance transition by input DC bias can be obtained as shown in Figure 4.1.

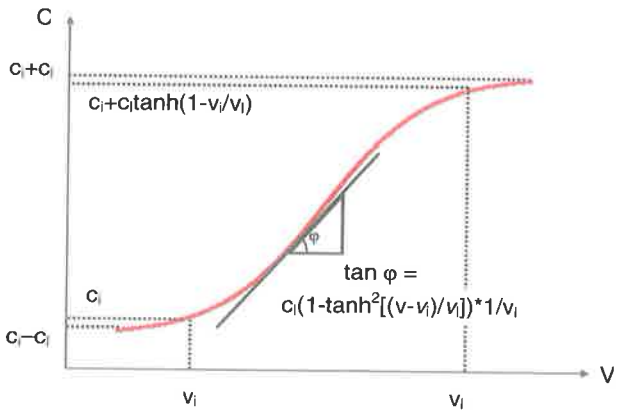


Figure 4.1: Nonlinear capacitance transition versus DC bias.

Such an induced capacitor model is fitted for a nonlinear characteristic in tuning the capacitance. Actually an active device such as a P/N diode or MOSFET can work as a general tuning element which has a function to adjust its capacitance by control input. From such a viewpoint, an integrated active component of a tank circuit is widely utilised for tuning the oscillation frequency of LC VCOs.

The key parameters to evaluate a varactor performance are the min/max capacitance ratio ($C_{\max}/C_{\min}$), linearity of a tuning frequency ($K_{\mathrm{VCO,max}}/K_{\mathrm{VCO,min}}$[1]) and the varactor Q. Since $C_{\max}/C_{\min}$ parameter can be nearly identified with the tuning range of

[1] K_{VCO} denotes a frequency gain to a control voltage for tuning the varactor and can be expressed

LC VCOs, it is required to be large to maximize the tuning range. $K_{\mathrm{VCO,max}}/K_{\mathrm{VCO,min}}$ ratio must be close to one in order to improve the linearity of the tuning frequency. Tank Q of LC VCOs can be also affected by varactor Q [42] as:

$$\frac{1}{Q_{\mathrm{total}}} = \frac{1}{Q_L} + \frac{1}{Q_{\mathrm{var}}} + \frac{1}{Q_{\mathrm{ext}}}, \tag{4.3}$$

where Q_{total} is an LC tank Q factor, Q_L, Q_{var} and Q_{ext} are the Q factors of the LC tank inductor, the integrated tank varactor and the N/PMOS cross-coupled pair, respectively. As indicated in Eq.(4.3), it is critical to improve the varactor Q to achieve low phase noise assuming that the on-chip inductor Q is reasonably high. In particular, the varactor Q tends to abruptly decrease at high frequency compared to that of the on-chip inductor as shown in Figure 4.2[2]. As a result, the varactor plays also very important role in enhancing the performance of LC VCOs.

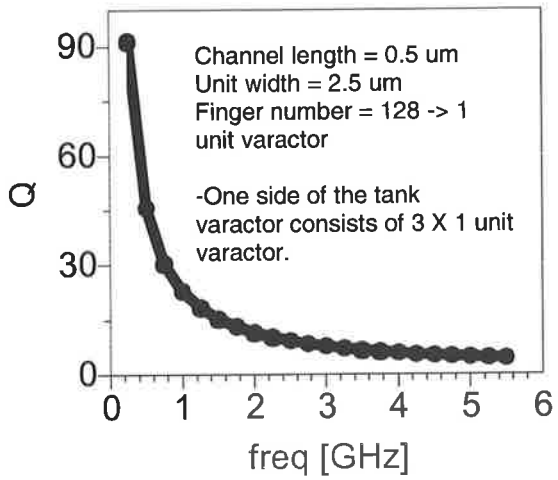


Figure 4.2: Varactor Q transition versus operation frequencies.

as follows.

$$K_{\mathrm{VCO}} = df(V_{\mathrm{tune}})/d(V_{\mathrm{tune}})$$

[2]The Q curve of the PMOS varactor is derived for a frequency range between 0.25 GHz and 5.5 GHz in TSMC 0.18 μm RF CMOS process using 1-port S-parameter simulation.

4.2 Junction Diode Varactor

The junction diode varactor has been employed in discrete LC VCO regime before the advent of a MOS varactor. The operation of the junction diode varactor is similar to the MOS varactor in that the tuned capacitance is achieved by varying the depleted parasitic capacitance through reversing bias voltage in the P/N junction. As shown in Figure 4.3, the holes in the p-type region are drifted to the anode port of the diode and the electrons are attracted to the cathode port when a reverse bias voltage is applied to the P/N junction.

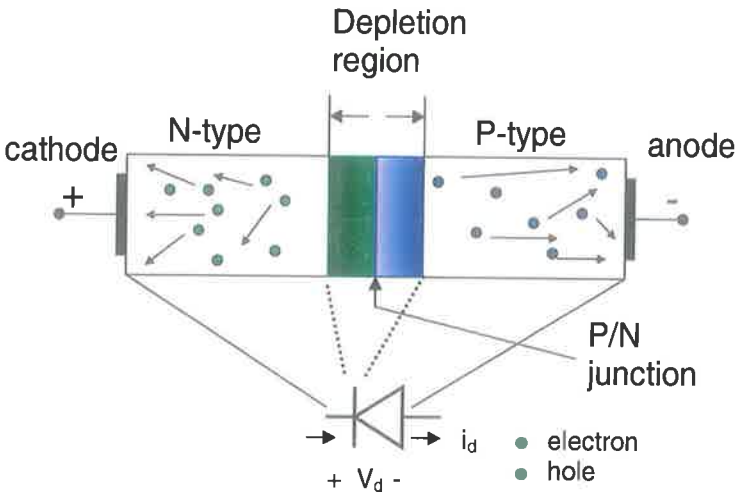


Figure 4.3: P/N junction diode.

Around P/N junction, the transferred charges of free holes and electrons leave the area depleted and the width of the depleted layer is directly proportional to the applied reverse bias voltage. Consequently, the capacitance component (C) corresponding to the increased width (d) is reduced in inversely proportion to the increased reverse bias by $C = \epsilon S/d$ (ϵ: dielectric constant, S: capacitive area in square meters). Since the junction capacitance is varied by the bias voltage, the diode varactor capacitance (C_v) can be defined as a function of the control voltage[3] (V_c) as:

[3]Packaging capacitance between the anode and the cathode ports must be added while it is omitted in Eq.(4.4) in that the capacitance is absorbed into the junction capacitance.

$$C_v = \frac{C_{jo}}{\left(1 + V_c/V_j\right)^N}, \tag{4.4}$$

where C_{j0} is the zero-bias junction capacitance, V_j is the built-in potential in P/N junction and N is a grading coefficient determined by doping profile (typically, 0.5 ~ 2) in the diode. Figures 4.4 and 4.5 represent the vertical structure and the optimised layout of a P/N junction diode varactor in a conventional CMOS process.

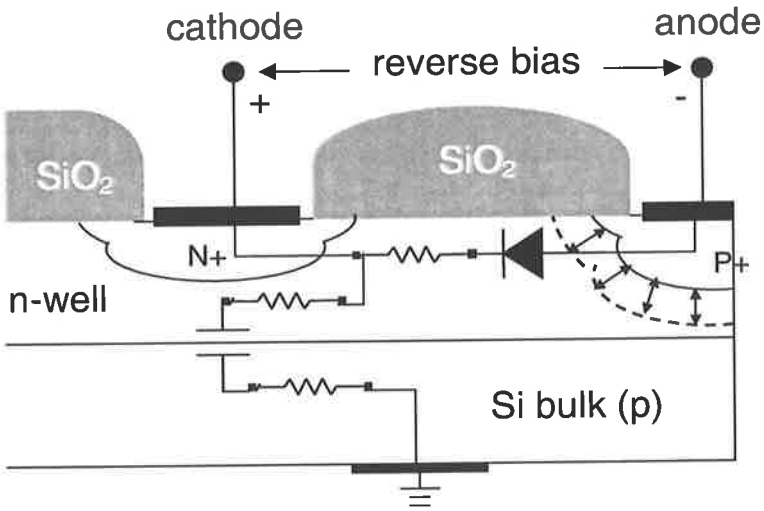


Figure 4.4: P/N junction diode structure in general CMOS process.

Black arrows (⟷) in Figure 4.4 indicate the depleted layer width, which is controlled by the reverse bias voltage in the p+/n-well junction. The resistor symbol represents the n-well resistance.

From Eq.(4.4), a doping concentration must be decreased or the bias range of the control voltage must be widened to enlarge the depleted parasitic capacitance. However, an additional processing step is required to increase the doping charge density and a bias voltage range is limited by the system specifications. On this account, an island style layout configuration can be used to increase the varactor diode capacitance as shown in Figure 4.5. This configuration provides more lateral junction capacitance compared with a diode of large p+/n- diffusion areas[4].

[4]Actually, the layout dimension of the junction diode must be considered to obtain optimised

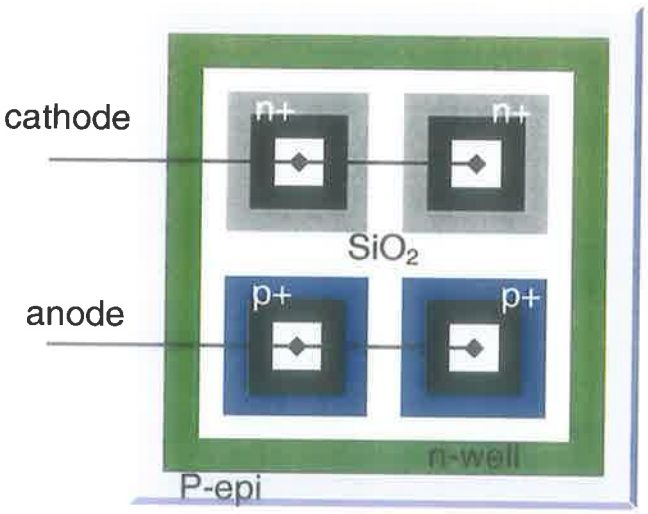


Figure 4.5: Unit-cell layout of a P/N junction diode varactor.

In typical CMOS processses, the junction diode varactors can be generally fabricated with three junction structures such as n+/p-bulk, p+/n-well and n-well/p-bulk. The p+/n-well junction structure is known to be the most suitable for the general diode varactors due to the fact that the p- silicon bulk is typically grounded.

In case of implementing such a diode varactor as a discrete IC component, it can be modelled as described in Figure 4.6[5] [72].

The key component governing Q factor of the diode varactor is the series resistance (R_s) as shown in Figure 4.6. The resistance can be lowered by increasing doping concentration relatively larger in n-well than p-bulk. Accordingly, the varactor Q can be easily enhanced by increasing the charge density during the fabrication process. Meanwhile it has a drawback to be forward biased when large voltage swings are generated in the tank circuit. In addition, the P/N diode generally has an inferior performance compared to the MOS varactor in terms of tuning range and phase noise when is applied to LC VCOs [73].

performance of the diode in that tradeoff between Q and C_{max}/C_{min} is caused by its denser layout.

[5] L_s models bonding wires connecting the diode die to the bonding pads and C_p indicates a parallel capacitance between the anode and the cathode which is formed when reverse bias is applied to the ports.

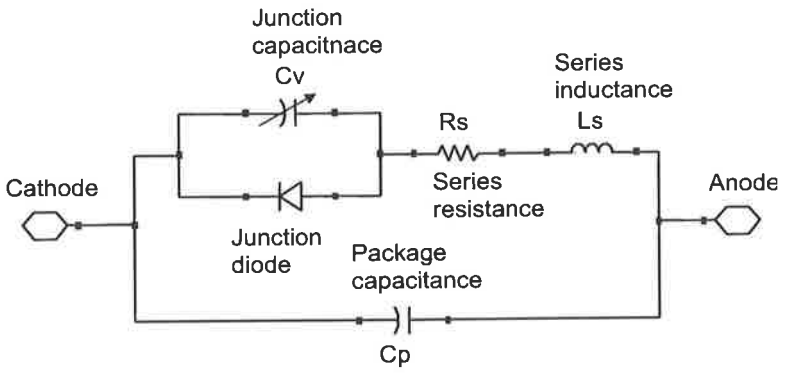
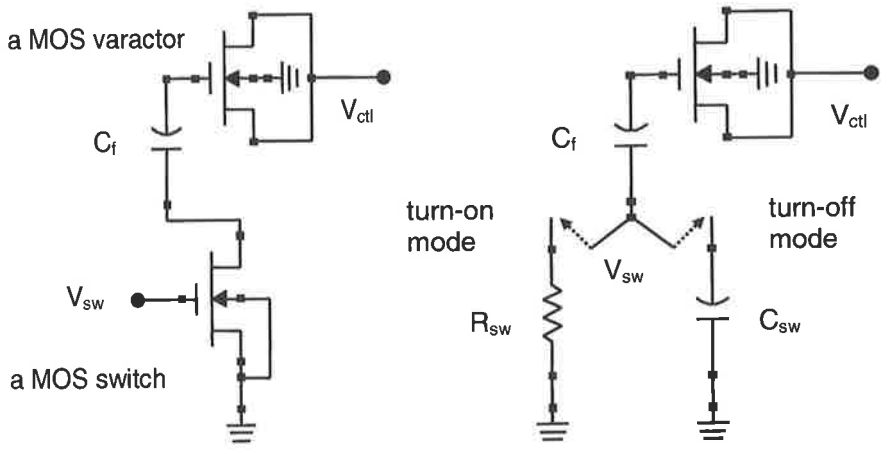


Figure 4.6: An equivalent model of a P/N junction diode varactor in general CMOS process.

4.3 Switched Capacitor

A switched capacitor is derived from a concept of selecting capacitances discretely among on-chip array capacitors using MOSFET switches [74]. Figure 4.7 illustrates a switched capacitor with a MOS varactor and its equivalent model in turn-on/off modes.



(a) Switched capacitor with a MOS varactor.

(b) In turn-on/off modes.

Figure 4.7: A switched capacitor and its equivalent model in turn-on/off modes.

C_f can be a MOSFET with a linear C-V characteristic while an on-chip linear capacitor is typically used for its high Q factor. Since an integrated MOS varactor generally tends to be abruptly degraded at high oscillation frequency of LC VCOs, a switched capacitor can be adopted to compensate the degraded LC tank Q. In Figure 4.7, C_{sw} is regarded as a capacitance between the drain and the body ports in turn-off mode and R_{sw} is approximated to the channel resistance of the MOSFET switch.

The MOSFET switch turns on/off by the control input signals (V_{sw}) and C_f becomes in series with the drain capacitance of the MOSFET switch in turn-off mode. Since C_{sw} is generally much smaller compared to C_f, the combined capacitance becomes $C_{\min}$ which is lower than C_{sw}. In this case, there must be a tradeoff between the Q factor of the total switch capacitor and $C_{\max}/C_{\min}$ ratio constituted of C_f and C_{sw} combination. It is because the Q factor depends on the conductance of the switch and the impedance of C_f by Eq.(4.5):

$$Q_{sw} = \frac{1}{2\pi f C_f R_{sw}}. \tag{4.5}$$

In order to improve the Q_{sw}, a wide MOSFET switch is recommendable to increase the conductance. However, the drain to bulk capacitance (C_{sw}) becomes larger and $C_{\min}$ is relatively increased. Therefore, the total $C_{\max}/C_{\min}$ turns to be decreased and the tuning range of the varactor becomes reduced. On this account, the dimensions of the switch must be carefully chosen considering the fixed capacitance to get an optimised switched capacitor.

In turn-on mode, R_{sw} is connected in series with C_f and the effective capacitance becomes nearly C_f if the impedance of C_f is much larger than that of R_{sw}. Accordingly, it is desirable to select the shortest transistor length. As a result of advances in fabrication process, it can gradually obtain a decent Q due to reduced channel resistance by scaling down the transistor dimensions.

4.4 MOSFET Varactor

A MOS varactor is utilised as an integrated component of an LC tank in that the channel capacitance of the device with a thin gate oxide capacitance is controllable by

applied tuning voltages. This bias voltage is fed from a PLL loop filter which operates as a voltage integrator transferring AC current equal to the phase difference of a PLL phase detector. As a rule, the gate port of the MOS varactor is connected to an output port of the LC VCO. The source/drain ports are tied together and connected to a tuning bias voltage. The body port can be utilised as a control input to increase a tuning frequency. Figure 4.8 illustrates a typical NMOS varactor in a conventional CMOS process.

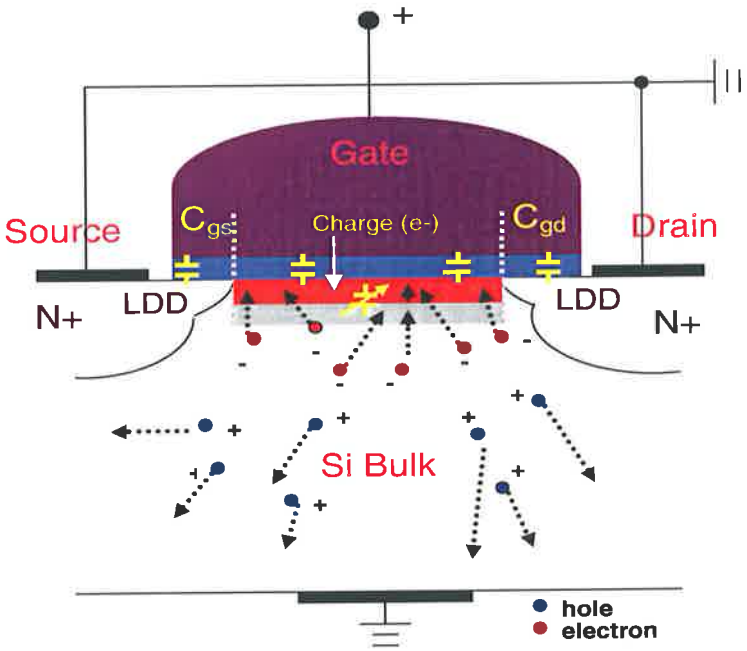


Figure 4.8: NMOS varactor structure on Si substrate.

As shown in Figure 4.8, overlap capacitance (between the poly gate and the LDD region) and a parallel plate capacitance (between the poly-gate and the channel) relatively have a constant value to the gate bias. The overlap capacitance is modelled in SPICE model as C_{gs} and C_{gd} as shown in Figure 4.8. On the other hand, a distributed channel capacitance below the boundary of the thin oxide film is modulated by the channel thickness variation. Since the varactor capacitance is defined by an arithmetic combination of C_{ox} and C_{ch} as:

$$C_{\text{var}} = \frac{C_{ox} \times C_{ch}}{C_{ox} + C_{ch}}, \tag{4.6}$$

the channel capacitance formed by forward/reverse biased voltages dominates the varactor capacitance and characterizes nonlinearity.

Typically, the capacitance is dependant on three operation modes of the MOS varactor: accumulation, depletion and inversion modes. Provided NMOS is in depletion mode ($V_{FB} < V_{GB} < V_{th}$, where V_{FB} is a flat band voltage[6], V_{GB} is a potential difference at the gate port to the bulk voltage and V_{th} is a threshold voltage of the NMOS transistor.) as an initial status, free electrons start to gather in the depleted p-type area ([redacted]) under the boundary of the gate SiO_2 if V_{GB} is over the threshold voltage (V_{th}). Since the Si bulk electrically has a neutral attribute, this status is called inversion mode because the charge concentration of free electrons (major carrier for NMOS) is larger than that of free holes (minor carrier for NMOS). In this inversion state, the carrier concentration linearly increases with regard to the amount of the increased V_{GB} per unit gate area and vertically the depleted thickness increases as well. Consequently, the charge density in the given unit area becomes nearly constant regardless of V_{GB} and C_{var} is approximated to C_{ox}.

On the contrary, free holes are attracted to stack as V_{GB} is decreased below V_{FB} since a negative gate bias repels free electrons into the deep Si bulk as depicted in Figure 4.9. Similarly to the inversion state, C_{ox} and Debye capacitance (ε_{si}/L_D ($\simeq C_{ch}$), where $L_D = \sqrt{(\varepsilon_{si} V_T)/(q \cdot P_s)}$) [75] become connected in series. L_D nearly reaches 0 as the charge density (P_s) of the stacked holes is increased. Therefore, the total capacitance of the MOS varactor in deep accumulation state is approximated as follows.

$$C_{\text{var}} = \frac{1}{\frac{1}{C_{ox}} + \frac{L_D}{\varepsilon_{si}}} \simeq C_{ox} \tag{4.7}$$

In other words, most of the p-type net charge existed in the Si substrate are distributed below the boundary of the gate oxide. This can be configured as a simple capacitor with two parallel metal plates. The Figure 4.10 demonstrates the capacitance transition of

[6] V_{FB} indicates a MOSFET is under equilibrium state in which energy band of the poly-gate is equal to that of the silicon bulk.

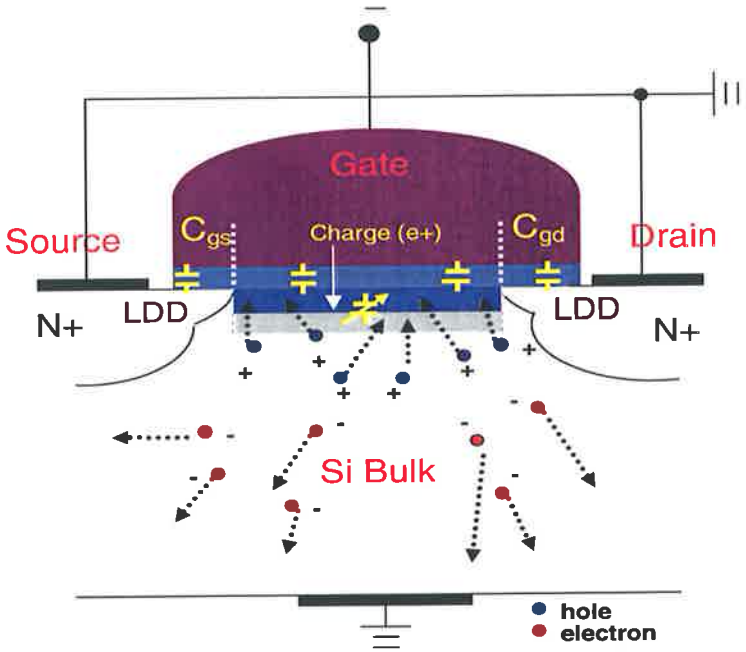


Figure 4.9: Accumulation mode of an NMOS varactor in bulk CMOS process.

the varactor with respect to DC input bias in the three operation modes[7].
Andreani, Mattisson *et al.* [50] and Ainspan, Plouchart *et al.* [76] verified that the MOS varactor operating in accumulation mode presents relatively a better phase noise performance compared to other modes. A phase noise improvement of 1 to maximum 7 dB is reported contrary to a typical P/N junction varactor, an inversion mode varactor and a three-terminal gated varactor.

4.4.1 Ultra Thin Silicon-on-Sapphire MOSFET Varactor

An SOS MOSFET varactor is structured with n+ diffusions of an NMOS (or p+ diffusions for a PMOS) in contact with a thick sapphire substrate. Accordingly, a junction capacitance (C_j) of the source and the drain diffusions to the substrate can be set to zero. It is due to the fact that the junctions of the channel edges and the

[7]The varactor C-V curve is derived using NMOS device models of TSMC 0.18 μm RF CMOS technology.

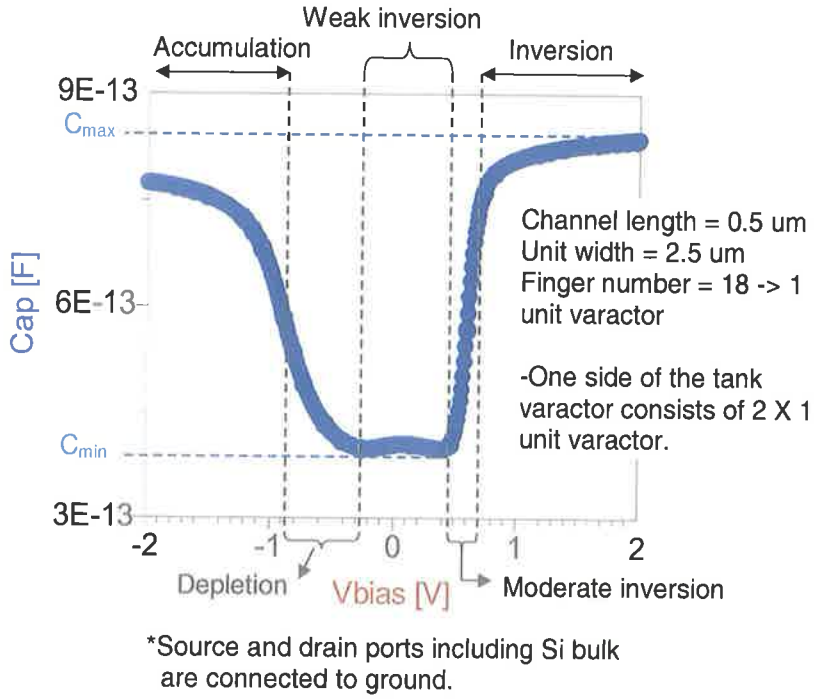


Figure 4.10: Capacitance variation of an NMOS varactor versus DC input bias.

substrate edges bordering on the diffusions can be acceptably ignored. Furthermore, a zero-bias perimeter capacitance (C_{jsw}) of the drain and the source diffusions is also proximate to zero because of the peculiar isolated structure[8]. Figure 4.11 illustrates the thin Si epi-layer of an NMOS which is almost fully depleted by a negative bias with other parasitic capacitances.

Such a configuration provides an advantage of simplicity in modelling the varactor capacitance resulting in a linear C-V curve and influences the tuning linearity of LC VCOs. On the other hand, the n+ diffusion layer is in contact with the sapphire substrate. Therefore, a route to provide the minority carrier (free hole) is intercepted together with the FOX when the MOS varactor operates in strong accumulation mode. Therefore, an accumulation mode MOS varactor in UTSi SOS process is not supported

[8]Typically, the thin silicon film is fully depleted according to the bias and the modulated capacitance becomes close to C_{ch}. Consequently, C_{gbo} is absorbed into the C_{ch} to be zero.

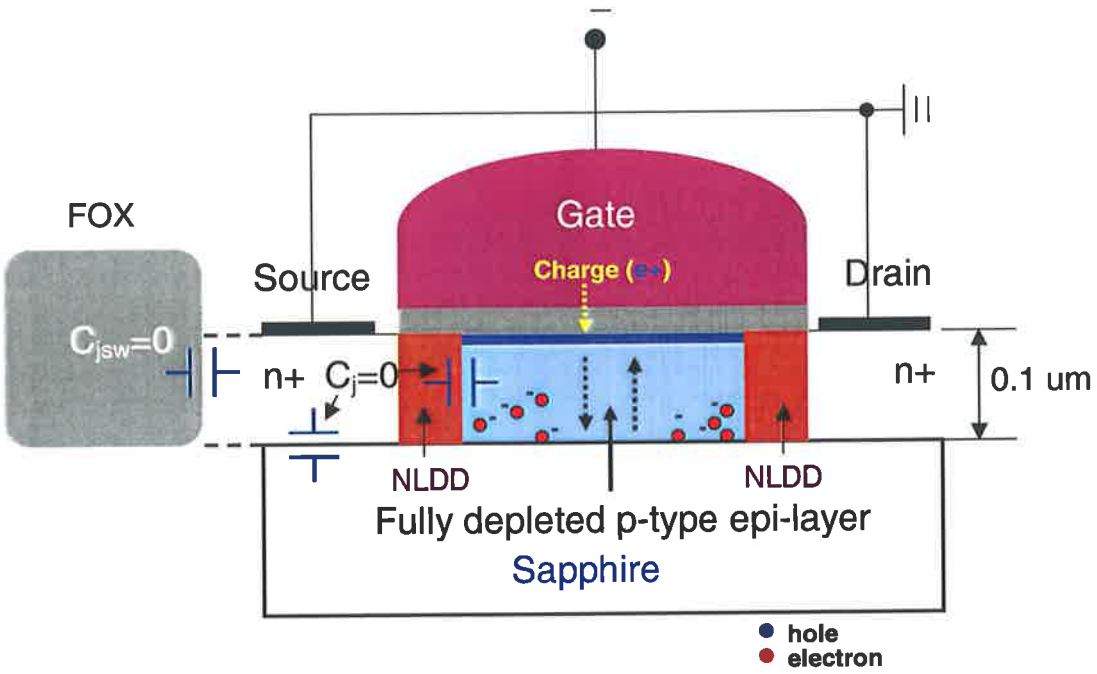


Figure 4.11: Configuration of an SOS NMOS varactor structure in a weak accumulation mode.

due to the MOS structure. Moreover, since the varactor capacitance in the accumulation mode can be nearly approximated to zero as in a depletion mode, only a depletion and an inversion modes can be utilised in UTSi SOS process as in Figure 4.12.

In both of the accumulation and inversion modes, the varactor seems to have a constant capacitance from the Figure 4.12[9]. Contrary to the C-V curve in Figure 4.12, however, the effective capacitance of the p-channel MOS varactor is diminished as the gate bias voltage is positively increased due to a depletion effect in the poly-silicon gate as described in Figure 4.13.

The poly gate becomes depleted as a result of the positive charge attracted on the contact area as the depleted p- Si bulk by positive bias to a PMOS. Consequently another capacitor is formed in series to the varactor gate. The induced capacitor

[9]In the accumulation mode, the varactor capacitance can be approximated to a constant value due to quite low density of the free holes stacked in the channel region

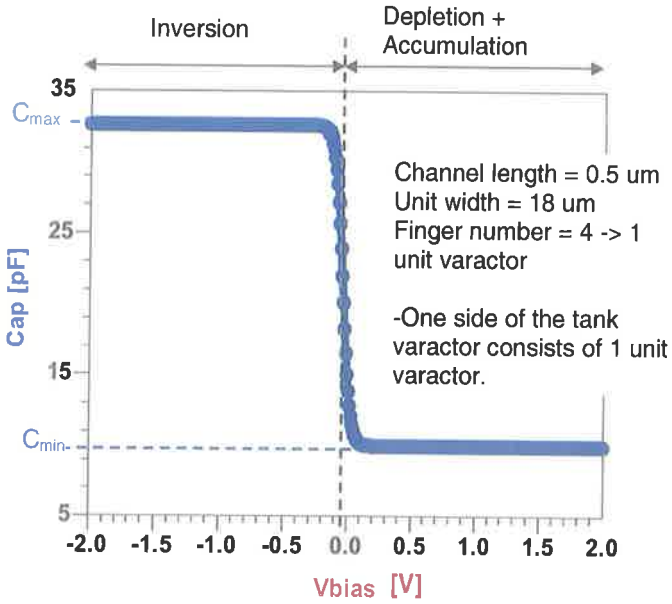


Figure 4.12: Capacitance variation of an SOS PMOS varactor versus DC input bias.

reduces the total capacitance according to the input bias voltage.

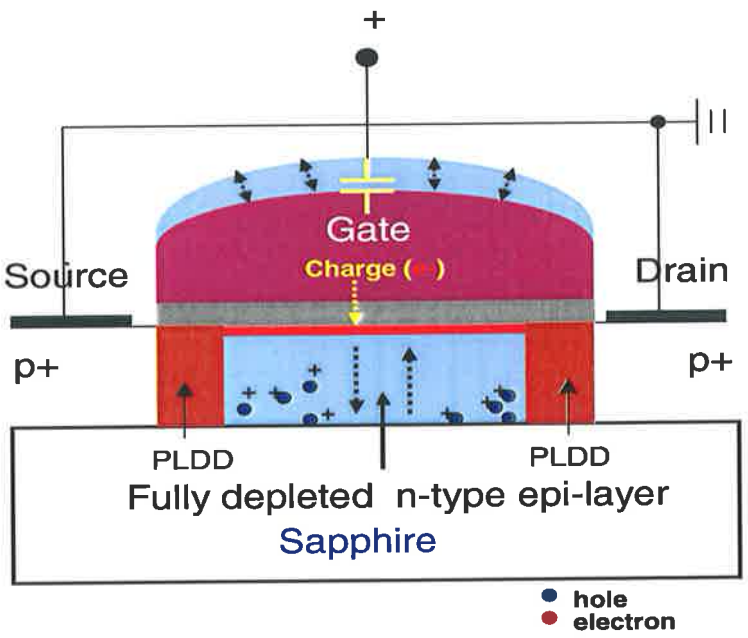
Note that the effect of poly-silicon depletion in UTSi process is not modelled in the SPICE model. In addition, Peregrine NMOS SPICE models do not adequately take kink effect into consideration while p-channel MOSFETs are reported as insignificant [77]. As shown in Figure 4.14, the kink effect is clearly appeared in the NMOS compared to the I-V curve of the PMOS.

The PMOS devices operating only in the depletion and inversion modes are exploited in this thesis. For an accurate modelling of the SOS MOS varactors, commercial device modelling tools such as MEDICI[10] or IC-CAP[11] can be used.

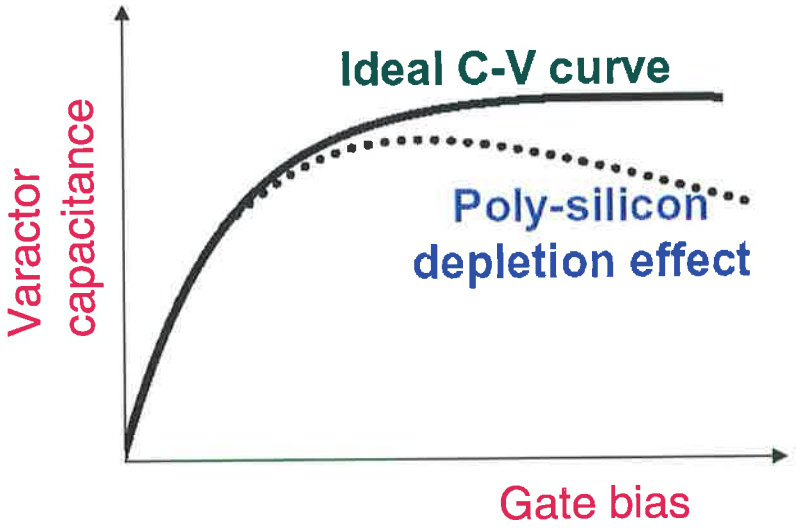
4.4.2 Large-Signal Effect of a MOS Varactor

As illustrated in Figure 4.12, the C-V curve of the SOS MOS varactor has a sharp transition in a small range of bias voltages (small-signal DC response). This makes the

[10]MEDICI is a registered trademark of Avant! Corporation which is now merged into Synopsys.
[11]IC-CAP is a registered trademark of Agilent.



(a) Physical view of poly gate depletion.



(b) Comparison of ideal/real varactor capacitances.

Figure 4.13: Depletion effect in the poly-silicon gate of an SOS MOS varactor.

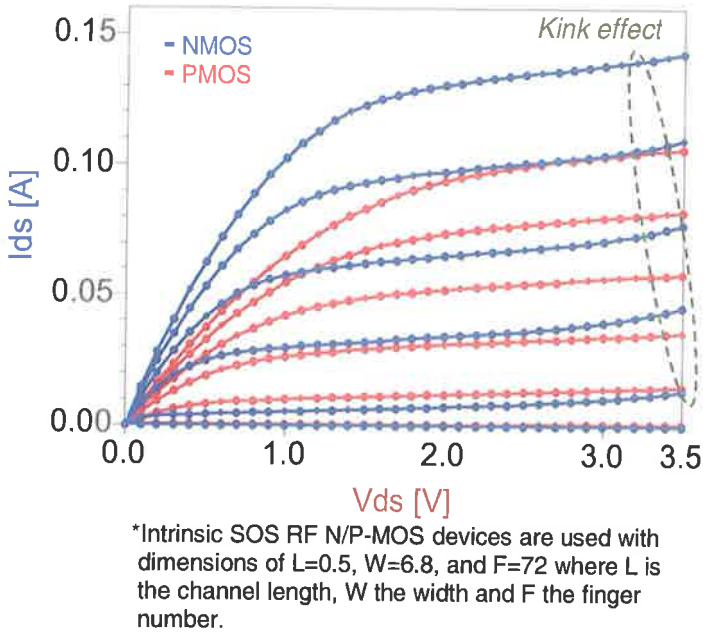


Figure 4.14: Kink effect in SOS N/P-channel MOSFETs.

varactor tuning range sensitive to input bias. In addition, such a varactor results in a more nonlinear characteristic when applied to the tank circuit of the LC VCO.

However, the LC oscillator generally responds to the average varactor capacitance rather than to a specific capacitance on the C-V curve. In addition, the varactor C-V curve becomes more linear since a relatively large AC voltage compared with the bias voltage transition between $C_{\max}$ and $C_{\min}$ is applied across the varactor during oscillation. In other words, the tuning curve becomes more nonlinear to smaller tank voltage amplitude.

To obtain such an average capacitance (C_{avg}) mathematically, the oscillation output is assumed to be purely sinusoidal at the fundamental frequency (f_0), i.e. no higher order harmonics[12]. If the output signal is presumed $v(t) = A\sin(\omega_0 t) + B$ (where A represents the output voltage amplitude, B is an arbitrary DC voltage reference applied to the varactor and ω_0 is the radian oscillation frequency), C_{avg} and $i(t)$ can be derived

[12]Such approximation is meaningful only for a linear time-invariant system at its fundamental frequency and adopted to look into the average capacitance transition of a MOS varactor.

from Eq.(4.1) as follows[13].

$$C_{avg} = \frac{\text{rms}(i(t))\big|_{f_0}}{\text{rms}(\frac{dv}{dt})\big|_{f_0}} \tag{4.8}$$

$$\begin{aligned} i(t) = \frac{d(q(v(t)))}{dt} &= \frac{d}{dt}\left(c_i v(t) + c_l v_l \ln\cosh\left[\frac{v(t)-v_i}{v_l}\right]\right) \\ &= c_i\frac{dv(t)}{dt} + c_l \tanh\left[\frac{v(t)-v_i}{v_l}\right]\frac{dv(t)}{dt}, \end{aligned} \tag{4.9}$$

where $\text{rms}(i(t))\big|_{f_0}$ indicates a root-mean-square (**rms**) current at the oscillation frequency. Since $dv(t)/dt = A\omega_0\cos(\omega_0 t)$, then:

$$i(t) = c_i A\omega_0\cos(\omega_0 t) + c_l A\omega_0\cos(\omega_0 t)\tanh\left[\frac{A\sin(\omega_0 t)+B-v_i}{v_l}\right]. \tag{4.10}$$

Since each **rms** value can be determined from Fourier series coefficient a_1, $\text{rms}(\frac{dv}{dt})\big|_{f_0}$ becomes:

$$\text{rms}(\frac{dv}{dt})\big|_{f_0} = \frac{2}{T}\int_0^T A\omega_0\cos^2(\omega_0 t)\ dt = A\omega_0. \tag{4.11}$$

In the same manner,

$$\text{rms}(i(t))\big|_{f_0} = \frac{2}{T}\int_0^T \left(Ac_i\omega_0\cos^2(\omega_0 t) + Ac_l\omega_0\cos^2(\omega_0 t)\tanh\left[\frac{A\sin(\omega_0 t)+B-v_i}{v_l}\right]\right) dt. \tag{4.12}$$

Accordingly,

$$C_{avg} = c_i + \frac{2c_l}{T}\int_0^T \tanh\left[\frac{A\sin(\omega_0 t)+B-v_i}{v_l}\right]\cos^2(\omega_0 t)\ dt. \tag{4.13}$$

Assuming that $B - v_i = 0$ for simplicity, if λ is assigned to $A\sin(\omega_0 t)/v_l$, thus

[13]From Eq.(4.1), C_{avg} and dq/dv can be rewritten as

$$C_{avg} = \text{rms}(dq/dv)\big|_{f_0} dq/dv = dq/dt \times dt/dv = i(t) \times dt/dv.$$

$$\begin{aligned} \frac{d\lambda}{dt} &= \frac{A}{v_l}\omega_0 \cos(\omega_0 t) \\ dt &= \frac{v_l}{A\omega_0 \cos(\omega_0 t)} d\lambda \\ T &= \frac{\sin^{-1}\frac{\lambda v_l}{A}}{\omega_0}. \end{aligned} \tag{4.14}$$

Therefore, Eq.(4.13) can be rearranged as:

$$C_{avg} = c_i + \frac{2c_l}{T}\int_0^{\frac{\sin^{-1}\frac{\lambda v_l}{A}}{\omega_0}} \tanh(\lambda)\left(1 - \frac{v_l^2\lambda^2}{A^2}\right) d\lambda. \tag{4.15}$$

Taken into account of c_l, v_l and T, these parameters are determined by the system environment and an arbitrary time period of the oscillation frequency to calculate the capacitance. For that reason, it can be said the values are fixed to certain parameters (namely, constant values). As a result, the voltage amplitude of the tank circuit ultimately governs the average capacitance (C_{avg}). In the next chapter, this will be further considered altogether with the tuning configuration.

4.5 LC Tank Co-simulation

All of the active device models in the design kit provided from Peregrine Semiconductor are based on BSIM3v3.2 [78], which predicts Q factors of the MOS varactors inaccurately. It is due to the fact that the channel resistance is not accurately modelled in the device models when an inversion layer between the drain and the source diffusions is formed. Furthermore, contact resistances of the active devices are not taken into consideration in the models. Consequently, these factors must be reflected into designing LC VCOs to correctly estimate the phase noise performance.

4.5.1 MOS Varactor Q

Similarly to an on-chip inductor or an MiM capacitor, Q factor concept can be applied to active devices. In case of a MOS varactor, the Q factor can be defined as:

$$Q_{\text{var}} = \frac{1}{\omega_0 R_s C_{\text{var}}}, \tag{4.16}$$

where ω_0 represents the fundamental frequency of the oscillator, and R_s and C_{var} are the series resistance and the capacitance of the varactor. In the inversion mode, the R_s is composed of the gate resistance, varactor contact resistance, inversion channel resistance and interconnection resistance between the varactors[14].

The channel resistance and the poly-gate resistance can be regarded as a resistance in series with the oxide gate capacitance while a variable capacitance by the bias voltage is formed between the channel region and the poly gate. Moreover, the channel resistance of the varactor is dependant on the inverted layer conductivity. Such an operational configuration results in a complicated analysis for the distributed MOSFET layout as an RC transmission line. Consequently, it can be said that the analysis result is mainly dominated by the varactor geometry and the channel length modulation.

4.5.2 Optimum Varactor and Co-simulation with a Symmetric Inductor

Similarly to the on-chip capacitor, the gate area ($W \times L$, where W is the gate width and L is the gate length.) of the MOS varactor determines the capacitance by:

$$C_{\text{var}} = 3.9 \times \epsilon_{ox} \frac{WL}{t_{ox}}. \tag{4.17}$$

From Eq.(4.17), the gate resistance (namely, the varactor dimension) can be expected to govern the varactor Q. Since the fundamental frequency is set to 5.8 GHz and the optimised inductance is in the order of 2 nH (as discussed in Chapter 3), the varactor capacitance of around 0.376 pF[15] is required from $f_0 = 1/2\pi\sqrt{LC}$. However, the total tank capacitance is mainly determined by a combination of the varactor tuning capacitance, the parasitic capacitances of the integrated inductor and active device layout including metal interconnection. Accordingly, it is necessary to take all

[14]Note that an accumulation mode varactor is not applicable in UTSi SOS CMOS process.

[15]The actual varactor capacitance tends to increase due to the overlap and the fringing effects caused by the MOS finger structure.

of the circuit layout capacitance into consideration if possible to accurately estimate the oscillation frequency. Note that the capacitance necessary for the 5.8 GHz LC VCO is selected on the basis of the EM simulation of the LC VCO layout in Chapter 5.
Since UTSi SOS process is mainly dedicated to FD CMOS, only FD PMOS device operating in inversion mode is exploited for the LC tank varactor. It is due to lesser kink effect and lower flicker noise compared to the NMOS counterpart.
According to Andreani and Mattisson [73], a MOSFET channel can be modelled as a one-dimensional RC delay network and a series resistance (R_s). This resistance can be approximated to $R_{ch}/12$ when the transistor is operating in the inversion mode. As a result, the varactor Q can be rewritten as:

$$Q_{\text{sos,var}} = \frac{1}{\omega_0 R_s C_{\text{var}}} = \frac{12}{\omega_0 C_{\text{var},\square} W L R_{ch}}. \tag{4.18}$$

Since the channel resistance can be estimated from $\partial I_{DS}/\partial V_{GS}$ when $V_{DS} = 0$, R_{ch} for the SOS MOS varactor can be derived from I_{DS} as follows:

$$I_{DS} = \frac{1}{2n}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}), \tag{4.19}$$

where n points out N factor which is called as a body-effect coefficient affecting on the transconductance of SOI MOSFETs and it typically has a value of 1.05 to 1.1 in the case of FD SOI MOSFETs[16] [79], μ_p and C_{ox} are the hole mobility and unit gate capacitance, and λ represents the channel length modulation coefficient.
Consequently,

$$R_{ch} \simeq \partial V_{GS}/\partial I_{DS}\big|_{V_{DS}=0} = \frac{nL}{k_p(V_{GS} - V_{th})W}, \tag{4.20}$$

where k_p is $\mu_p C_{ox}$. MOSFET models of UTSi SOS process are similar to BSIM3-SOI FD models in terms of a depleted degree of the thin Si epitaxial film. The n factor of the SOS MOSFET is set to 1.05 [80].
From $\epsilon = \epsilon_{ox} \times \epsilon_r = 8.86 \times 10^{-14}$ F/cm $\times$ 3.9 $\approx$ 0.34554 pF/cm, $C_{\text{var},\square}$ and C_{var} can be induced by:

[16] In case of typical CMOS transistors, the N factor ranges 1.3–1.5.

$$C_{\text{var},\square} = \frac{\epsilon}{t_{ox}} = \frac{0.34554 \times 10^{-12}\ \text{F/cm}}{0.01 \times 10^{-8}\ \text{cm}} = 0.34554 \times 10^{-2}\ \text{F/cm}^2. \tag{4.21}$$

$$C_{\text{var}} = 0.34554 \times 10^{-2}\ \text{F/cm}^2 \times WL\ \mu\text{m}^2 = 34.554 \times 10^{-12} \times WL\ \text{F}. \tag{4.22}$$

Since the hole conductivity (μ_p) is 280 $\text{cm}^2/\text{V} \cdot \text{sec}$ for the intrinsic UTSi SOS PMOS, k_p becomes 0.9675 A/V^2. The SOS varactor Q in the inversion mode can be rewritten using the Eq.(4.16) at 5.8 GHz as:

$$\begin{aligned} Q_{\text{sos,var}} &= \frac{12k_p(V_{GS} - V_{th})}{\omega_0 C_{\text{var},\square} n L^2} \\ &= \frac{12 \times 0.9675 \times (V_{GS} - V_{th})}{2\pi \times 5.8 \times 10^9 \times 0.34554 \times 10^{-10} \times 1.05 \times L^2} \\ &= \frac{11.61 \times (V_{GS} - V_{th})}{1.322 L^2} \\ &\simeq \frac{8.782 \times (V_{GS} - V_{th})}{L^2}. \end{aligned} \tag{4.23}$$

Therefore, a minimum gate length (i.e. 0.5 μm) for optimum Q must be chosen for a low series resistance (R_s), thereby a high Q varactor. Although $V_{GS} - V_{th}$ is determined by the design specification, $Q_{\text{sos,var}}$ approaches 14 at 5.8 GHz at the minimum gate length of 0.5 μm when $V_{GS} - V_{th}$ is set to 0.4 V, which is half of the targeted bias voltage of the LC oscillator[17]. To entirely observe the tank Q transition, a co-simulation method is utilised with physical design data of the tank inductor instead of investigating the varactor Q separately. It is because the SPICE model of the varactor mutually interact with the inductor EM simulation result including the parasitic components. Note that since 2.5D EM simulator can manage only the structure data of passive devices, the layout configuration effect of the active devices is not truly reflected into the co-simulation.

[17]Since the introduced Q formula is valid for varactor Q estimation only in the strong inversion, it does not show the Q dependance on R_{ch} and C_{var} by input control signals. As the width is fixed for the tuning capacitance at the oscillation frequency, the SPICE modelling method for parasitic effects is actually limited to explain the Q transitions depending on the different device models.

In the RF SOS MOSFET models provided by Peregrine Semiconductor, two types of unit gate widths are given to 6.8 μm and 18 μm for the intrinsic PMOS devices. In addition, the device models are divided into three transistor types according to threshold voltages of -0.03, -0.25 and -0.6 V. In general, the switching speed of a transistor tends to increase owing to higher standby current as the threshold voltage lessens. In addition, the kink effect in the SOS MOSFETs is mitigated on account of being more fully depleted, which enhances the prediction of the SPICE model behaviour.

On the other hand, abnormal operation of the varactor can occur on account of leakage current when low threshold voltage varactors are utilised. Consequently, the co-simulation is performed with the whole device models at the minimum length of 0.5 μm. In the next section, the tank Q curves are derived and analyzed from the co-simulation results depending on the device models.

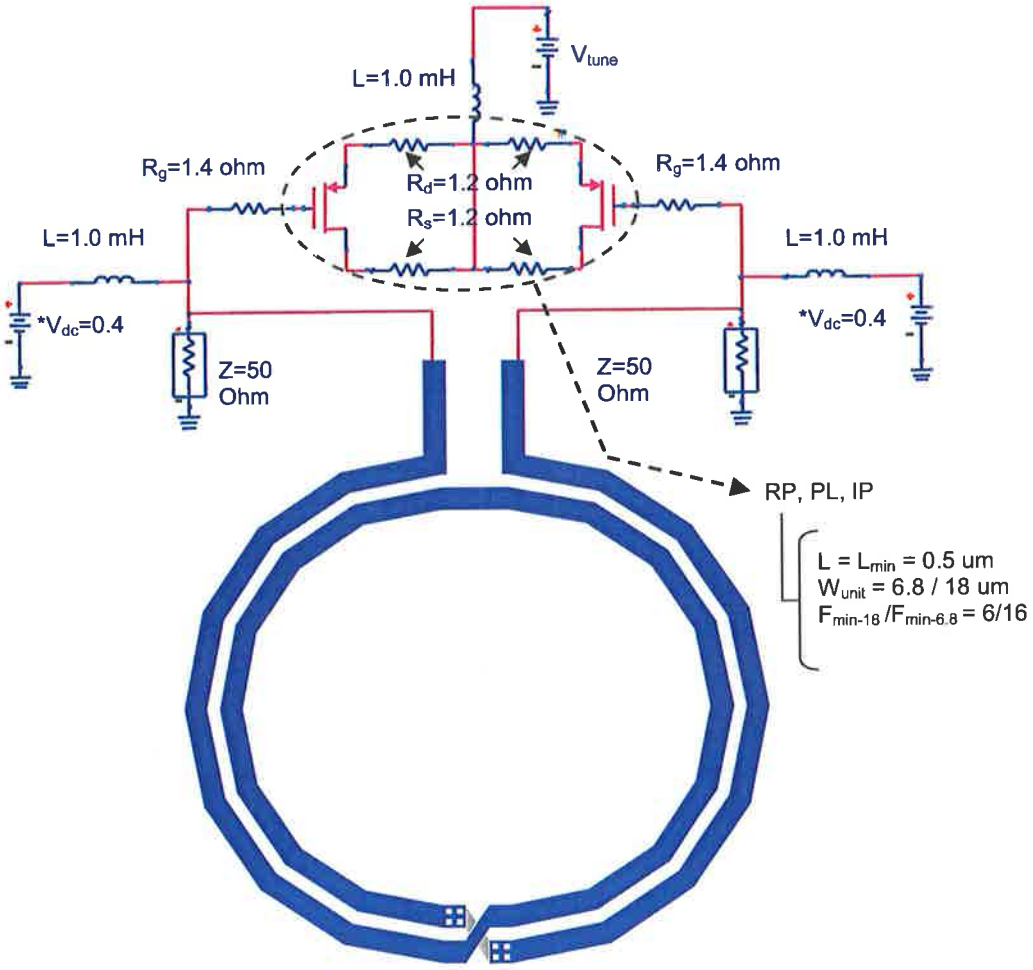
4.6 Experimental Co-simulation Results

Since the drain/source ports of the tank varactor are tied and connected to a tuning bias voltage, the common node becomes grounded in AC analysis. In addition, the common node of the symmetric inductor presented in Chapter 3 is theoretically grounded. As a result, the tank can be analyzed with 2-port pi (Π) network as shown in Figure 4.15.

Although the control voltage range for tuning the varactor capacitance is actually set below the power supply voltage (around 10 $\sim$ 20 %), the tuning bias is ranged to 0.8 V considering a marginal increase of the power supply voltage. Note that the range of the tuning bias is fixed while the upper and the lower limits may be differently applied depending on the models. All varactors in this research operate in inversion mode by applying a positive bias to PMOS MOSFET models.

The contact resistances (R_d, R_s and R_g) at the gate/source/drain ports are referred to in [81] and connected at each port with the worst case value as shown in Figure 4.15.

Since the 5.8 GHz LC VCO has a tuning range of around 700 MHz, all of the device models have same dimensional configurations. Therefore, the minimum channel length of 0.5 μm for low channel resistance is equally applied to all device models. In addition,

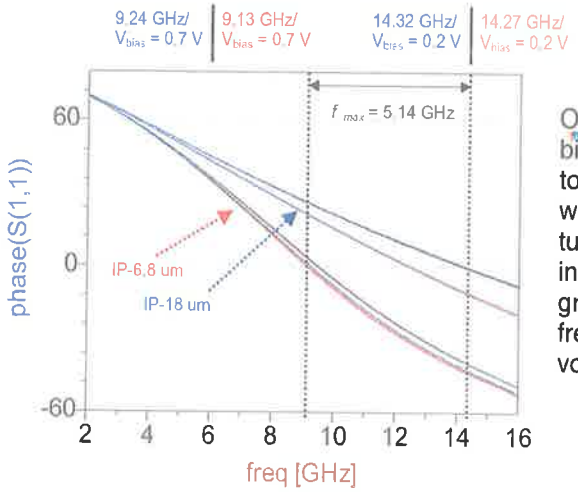


*RP : regular threshold voltage (Vth) p-channel transistor of -0.6 Vth
*PL : low threshold voltage p-channel transistor of -0.25 Vth
*IP : intrinsic p-channel transistor of -0.03 Vth
*L_{min} : minimum gate length ; *W_{unit} : unit gate width
*F_{18} & $F_{6.8}$: minimum finger numbers for the active models with the unit gate widths of 18 um and 6.8 um, respectively
*V_{dc} becomes 0.45 V in case of the quadrature VCO

Figure 4.15: Co-simulation schematic for the tank Q estimation.

the finger number for the same tuning frequency range is set to 16 for RP/PL/IP[18] 6.8 μm and 6 for RP/PL/IP 18 μm models. As the SOS MOSFET models (RP/PL/IP)

[18]Refer to Figure 4.15.

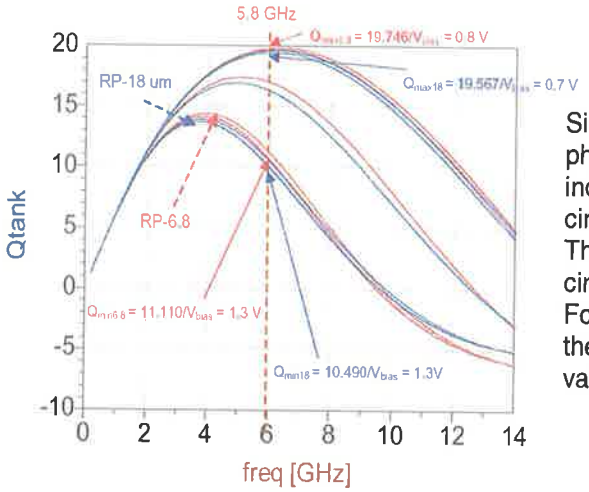


On the whole, the narrowest tuning bias range (both 0.5 V) compared to other device models are used with the IP models, which enable a tuning range of 5.14 GHz. This indicates IP models are relatively greater tuneable due to their higher frequency sensitivity to tuning voltage.

Figure 4.18: S(1,1) phase of the tank circuit with IP 6.8 μm/18 μm models.

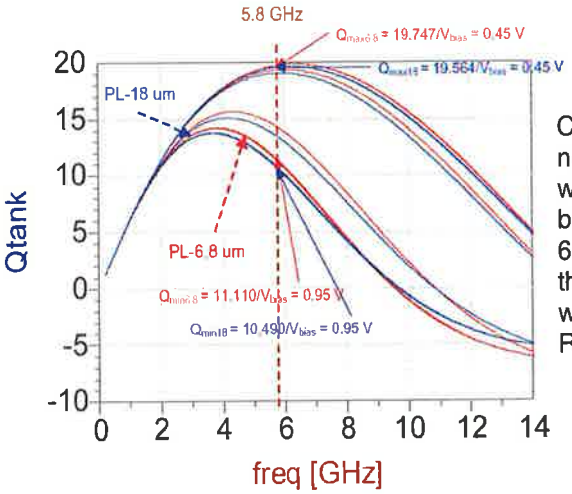
be the most desirable for the tank varactor of the single and quadrature LC VCOs in terms of wide tuning range. Meanwhile, the tuning ability of the RP-6.8 μm model is relatively inferior to other device models.

Figures 4.19, 4.20 and 4.21 demonstrate the tank Q factors as a function of the tuning voltage range.



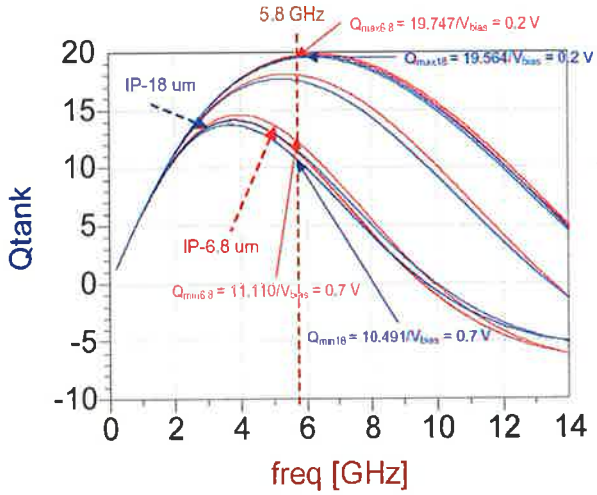
Similarly to the case of S(1,1) phase, the blue line and figures indicate the Q factor of the tank circuit using the RP-18 um model. The red counterpart is for the tank circuit using the RP-6.8 um model. For the most part, the Q factor by the RP-6.8 um exhibits the highest value within 0.6 Vbias range.

Figure 4.19: Tank Q with RP 6.8 μm/18 μm models.



Compared to the RP models, the nearly same Q variation occurs with a narrower range of the tuning bias voltage (0.5 Vbias). Also, PL-6.8 um model has better Q values than PL-18 um model on the whole which is similar to the case of the RP models.

Figure 4.20: Tank Q with PL 6.8 μm/18 μm models.



As a whole, the Q factor of the IP models draws a similar curve compared with the previous two models within 0.5 Vbias range. Thus, Q factor variation according to the device models can be negligible.

Figure 4.21: Tank Q with IP 6.8 μm/18 μm models.

Similarly to the maximum frequency tuning characteristics in Figures 4.16, 4.17 and 4.18, the tank Q exhibits a negligible difference at 5.8 GHz irrespective of the device models. The PL-6.8 μm/IP-6.8 μm models relatively show the more stable Q factor distribution. This is due to the fact that the lowest Q factors of the two models occur at higher tuning bias voltage compared to the RP model.

At the current stage, it can be said that the IP model is more applicable for wide tuning

frequency range of the targeted LC VCOs. In particular, the IP model characterizes the lowest threshold voltage. In case of the RP or PL models, an additional circuit is required to shift or increase the voltage level of the tuning bias due to higher tuning voltage level. Considering the low power supply voltage of the targeted LC VCOs, this design scheme is not desirable owing to increased power consumption and circuit complexity. On the whole, since Q factor difference with regard to the device models is also negligible, the IP 6.8 μm model is more acceptable due to its wider tunability and lower threshold voltage. This model will be exploited in designing the LC VCO. The next chapter will present the overall design of a single and quadrature LC VCOs.

Chapter 5

LC VCO Design, Layout and EM Simulation

In this chapter, both of the symmetric inductor and the PMOS varactor presented in the previous chapters are implemented into the overall design of a single and quadrature LC VCOs. The design procedure of the single and quadrature LC VCOs is demonstrated in detail with the schematic and layout simulations. EM simulations are conducted using the quasi-3D metalisation modelling for layout simulation of the LC VCOs. The post-layout simulation issues of the VCO circuits are also discussed.

5.1 Introduction

In the previous chapters, the theory of $-G_m$ oscillator, the symmetric inductors and the tank circuit using the PMOS varactors are discussed for a differential LC oscillator design to be presented in this chapter. Although the design procedure of the inductor and the tank circuit are sequentially introduced, the real design process of an RF oscillator is not progressed in the same manner. Since the design of the individual components influences the whole design process of the LC oscillator, a series of retreats to the design of the components are inevitable for the synthetic design. For instance, the parasitic components of the overall oscillator layout impacts on the prediction of the oscillator frequency of operation. As a result, the fundamental frequency of the oscilla-

tor has a deviation of 12 % (approximately 0.7 GHz) compared to that obtained from the schematic simulation. In addition, a necessity for adjusting the tank inductance and capacitance ratio is required depending on the gain of the N/PMOS pairs during the design phase. As the size of the differential pair FETs are enlarged to increase the pair FETs gain, the available tank capacitance to tune the oscillation frequency must be reduced. This requires an adjustment of the tank inductance and necessitates lowering inductance to oscillate at the required tuning frequency. By energy conservation theorem, the energy stored in the tank inductor (P_{Ltank}) and capacitor (P_{Ctank}) at the resonant frequency must be the same by:

$$P_{\mathrm{Ltank}} = \frac{L_{\mathrm{tank}} I_{\mathrm{peak}}^2}{2}, \qquad P_{\mathrm{Ctank}} = \frac{C_{\mathrm{tank}} V_{\mathrm{peak}}^2}{2} \tag{5.1}$$

$$P_{\mathrm{Ctank}} = P_{\mathrm{Ltank}} \longrightarrow \frac{C_{\mathrm{tank}} V_{\mathrm{peak}}^2}{2} = \frac{L_{\mathrm{tank}} I_{\mathrm{peak}}^2}{2}, \tag{5.2}$$

where I_{peak} is a peak tank current, V_{peak} is a peak tank voltage, L_{tank} is a tank inductance and C_{tank} is a tank capacitance. From Eq.(5.2), the energy loss (P_{loss}) occurred in the tank can be expressed as:

$$P_{\mathrm{loss}} = I_{\mathrm{peak}}^2 R_{\mathrm{tank}} = C_{\mathrm{tank}} \frac{R_{\mathrm{tank}} V_{\mathrm{peak}}^2}{L_{\mathrm{tank}}}, \tag{5.3}$$

where R_{tank} is a tank resistance. From the Eq.(5.3), the ratio of $L_{\mathrm{tank}}/C_{\mathrm{tank}}$ influences the power consumption of the oscillator to compensate the tank energy loss. The reduced inductance is also connected to the diminished voltage amplitude of the tank circuit. Because the tank voltage amplitude (A_{tank}) is related to L_{tank} by [54]:

$$A_{\mathrm{tank}} = \frac{4 R_p I_{\mathrm{bias}}}{\pi} \approx \frac{4 \omega_0 L_{\mathrm{tank}} I_{\mathrm{bias}} Q_{\mathrm{tank}}}{\pi} = 8 f_0 L_{\mathrm{tank}} I_{\mathrm{bias}} Q_{\mathrm{tank}}, \tag{5.4}$$

where R_p is a parallel inductor resistance. Consequently, a high L_{tank} with a high Q_{tank} enlarges the signal power of the LC-tank and improves phase noise performance of the LC VCO according to Eq.(2.10) in Chapter 2. Meanwhile, an increased tank inductance to amplify the tank voltage amplitude necessitates is generally accompanied by a larger parasitic capacitance. The increased transistor size also directly affects power consumption and noise. As a result, the tuning frequency range is relatively

reduced with increased noise power. The finger number of N/PMOS pairs and tank varactors also needs to be decreased to oscillate at a targeting frequency. In particular, RF oscillators designed for narrow band communications are required to have a wider tuning frequency to compensate for variation in the fabrication process.
As there are currently no plans for fabricating the designs, some of the issues related to testing the VCOs have not been considered in this thesis. However, the comparison between the different design procedures will be discussed.

5.2 LC Oscillator Design

5.2.1 Single LC Oscillator Design

The starting point of the LC oscillator design is to set a power supply voltage[1]. Since the oscillator is targeted to low power consumption, the initial supply voltage for the single VCO is set to a minimum of 0.8 V. As discussed in Chapter 2, the symmetry of the VCO waveforms is critical for the low phase noise. For this symmetrical outputs, it is required that the LC VCO is designed using N/PMOS pairs and the transconductances of the NMOS and PMOS devices need to be equal to swing the outputs at a half V_{dd}[2]. Such a biasing method is also advisable for driving the output signals into the CMOS buffering inverter of a mixer input port.
However, this design methodology is necessary to be adjusted for low power LC VCO design in SOS CMOS process. From the Figure 2.6 in Chapter 2, the biasing point (V_B) can be calculated by:

$$V_B = V_{dd} - |V_{th,\mathrm{pmos}}| - \frac{I_{\mathrm{bias}}}{G_{M,\mathrm{pmos}}}, \tag{5.5}$$

where V_{dd} is the power supply voltage, $V_{th,\mathrm{pmos}}$ is the threshold voltage of the PMOS

[1]Generally speaking, The power supply voltage is actually set by a system specification in which the oscillator is integrated. This initial specification of a VCO is dependant on tank inductor Q due to requirement for negative resistance to compensate the tank loss.

[2]Actually, the finger number works as a limiting factor for optimizing the performance of an LC VCO in its design procedure since the gain of the differential pair FETs are determined by the geometry, i.e. W/L.

pair FETs, I_{bias} is the bias current of the oscillator and $G_{M,\text{pmos}}$ is the transconductance of the PMOS pair FETs. From the Eq.(5.5), it seems that the W/L ratio of the PMOS pair dominates the symmetry of the oscillator output waveform due to influence of PMOS transistor gain. However, SOS PMOS transistors have a higher hole conductivity compared to the counterparts in general CMOS processes [20]. Such a higher conductivity directly increases the transistor gain and provides merits of reducing the finger number of the PMOS pair in the LC VCO. Consequently, a double finger number of PMOS pair is not necessarily required for symmetric output. Moreover, the differential output amplitude of the designed LC VCO has a 0.3 V at most. Considering the threshold voltage of the N/PMOS pairs, output asymmetry by different transistor gain between the pairs can be regarded to be insignificant compared to the output voltage amplitude. It is due to the fact that increasing the finger number to obtain a larger transistor gain can achieve more symmetrical outputs, while the noise sources affecting phase noise performance are eminently increased. This causes an increase of noise power in the output signals and VCO power consumption. Therefore, such a tradeoff will be taken into consideration during the VCO design procedure.

In determining the gain of the cross-coupled N/PMOS pairs, it is necessary to derive the parallel resistance (R_p) from the inductors in Chapter 3. The 2-turn symmetric inductors with 140 μm and 120 μm radius have inductances of around 2 nH and 1.6 nH, respectively, at 5.8 GHz as shown in Figure 5.1.

The R_p ($R_{p,140}$ for 2-turn 140 μm inductor and $R_{p,120}$ for 2-turn 120 μm inductor) can be estimated by:

$$R_{p,140} = 2\pi f_0 L Q_L = 2\pi \times 5.8 \times 2.0 \times 22.25 \approx 1.62 \text{ k}\Omega \tag{5.6}$$

$$R_{p,120} = 2\pi f_0 L Q_L = 2\pi \times 5.8 \times 1.63 \times 21.78 \approx 1.29 \text{ k}\Omega \tag{5.7}$$

To cancel the R_p, the N/PMOS pairs must provide enough gain to satisfy the initial startup condition. Therefore, the magnitude of negative resistance (R_{neg}) presented in Chapter 2 must be larger than the R_p. The startup condition of the LC VCO can be derived by:

$$\left|\frac{-2}{G_M}\right| > R_p, \tag{5.8}$$

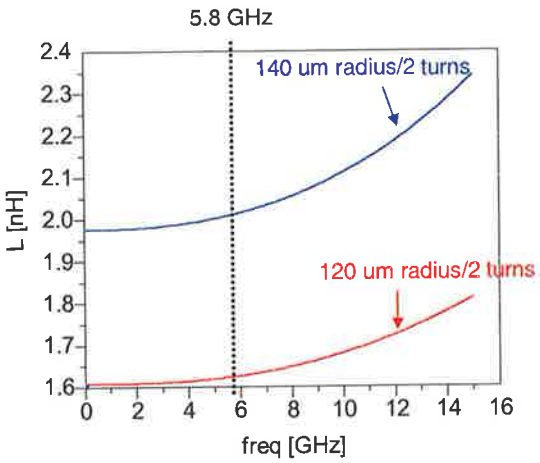


Figure 5.1: Inductances of the 2-turn 120/140 μm inductors.

where G_M indicates the total gain of the cross-coupled N/PMOS pairs. As long as G_M exceeds 1.23 mS for a single VCO and 1.54 mS for a quadrature LC VCO from the Eq.(5.8), the oscillator will safely start to generate output signals. Since the R_p has a high equivalent resistance by high Q factor of the inductor, the cross-coupled pairs can use a small number of fingers due to the fact that lower transistor gains are required. This also enables the design of a low power LC oscillator in SOS CMOS process.

As the threshold voltage of each device model affects the amplitude of the cross-coupled LC VCOs, the low threshold devices are desirable to obtain a larger output swing. In addition, the power of noise signals imposed on the output signals is relatively increased if the amplitude of the output swing becomes smaller. Meanwhile, a loading effect to the LC tank resonator is different depending on channel output resistance of each device model. Since the P/NMOS cross-coupled pairs of the LC VCO operate in triode region during a large portion of oscillation period, the channel resistance works as an important factor to govern the LC-tank Q. As the resistance increases, the loading effect retrogrades the tank Q and the phase noise performance is worsened.

In this research, MOSFET device models with the threshold voltages of 0.14 V/ -0.25 V for NMOS and PMOS cross-coupled pair, respectively are chosen due to their low output resistances. A minimum channel length of 0.5 μm is equally applied to the design of the single and quadrature LC VCOs. The finger numbers are chosen to

cient of the active FETs, $g_{m,\text{bias}}$ is the transconductance of the current source FET and V_0 is $4R_{\text{tank}}I_{\text{bias}}/\pi$ [84]. It is due to the fact that the filtering inductor is replaced with the current source for cutting off the low frequency upconversion. Since $\gamma\frac{4}{9}g_{m,\text{bias}}R$ in the Eq.(5.9) becomes zero, F comes to $1+\gamma$ (i.e. minimum noise factor) as a result. In addition, phase modulation by thermal noise of the cross-coupled pair depends on the common-mode impedance between the NMOS pair and the current source. As the impedance on the node increases, the cross-coupled pair is less driven into triode region and the transconductance is increased. Using a planar inductor of a high inductance, a high impedance path instead of the current source is easily formed. Therefore, this approach replacing the current source with an inductor reduces F and can improve the phase noise performance based on the Eq.(2.10) in Chapter 2.

To block the second harmonic, a symmetric circular inductor with 7 turns is used in the single LC oscillator to form a high impedance at $2f_0$. Since the LC oscillators presented in this thesis are designed to have a tuning range of more than 301 MHz at 5.8 GHz center frequency, a frequency band of 11 GHz to 12 GHz is critical for the second harmonic suppression. For this purpose, four types of symmetric circular inductors with 5 to 8 turns are designed and simulated to obtain a high impedance within the frequency band. To achieve a higher inductance in a smaller area, a symmetric inductor is reinduced from the tank inductor for the single LC VCO and modified to the equivalent of 198 μm vertical length by 180 μm horizontal width, 6 μm width with 3 μm spacing. Figures 5.3 and 5.4 show the inductor configuration utilised for suppressing the second harmonic with the impedance.

At 11.67 GHz, the highest impedance of the 7-turn symmetric inductor reaches around 10.8 kΩ which is governed by the Q factor. To attenuate the drain current noise of the NMOS pair, an MiM capacitor of 15 pF is located between the common node of the NMOS-pair and ground pad[5]. The final single VCO is depicted in Figure 5.5 with the optimised tank circuit presented in Chapter 4.

[5]A large MiM capacitor is desirable due to compensation for the parasitic capacitance variation of the filtering inductor.

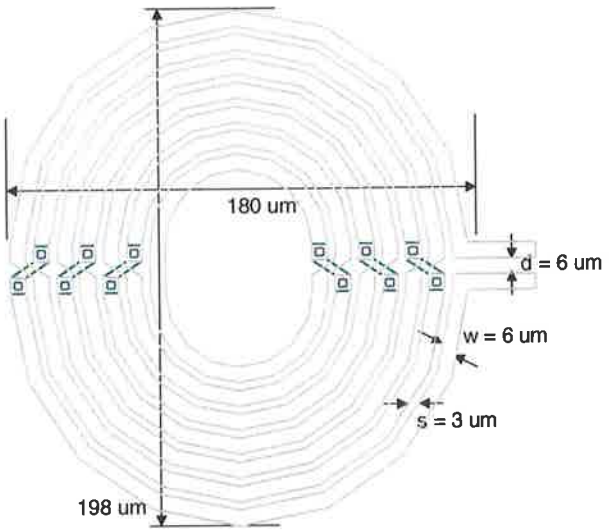


Figure 5.3: Symmetric circular inductor for suppressing the second harmonic.

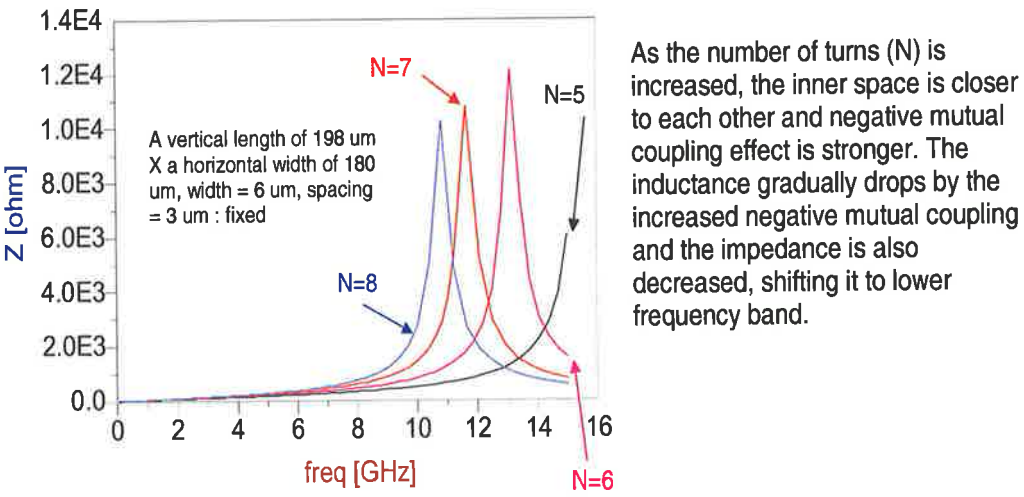


Figure 5.4: The impedance of the symmetric inductor at $2f_0$.

5.2.2 Quadrature LC Oscillator Design

Modern transceivers of low-intermediate frequency (IF) or zero-IF architectures employ in-phase and quadrature demodulation and modulation to cancel the image frequency without an image-rejecting filter. This facilitates that the IF signals with the identi-

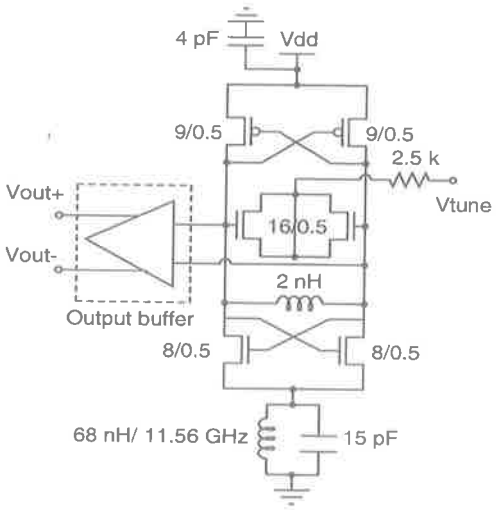


Figure 5.5: Final single LC VCO schematic with a noise filter.

cal polarities are reinforced after recombining the paths while the image signals with opposite polarities are cancelled out.

To generate quadrature signals (i.e. 0° and 90°), a frequency doubling by master-slave flipflops or a polyphase filtering with an RC-CR phase-shift network can be used [85]. However, these methods are directly connected to the issue of the power consumption and phase noise by increased noisy active components. As an alternative, two identical VCOs [86] can be exploited as long as one of the VCO cores dissipates less power than the master-slave flipflops for doubling the frequency. In addition, this architecture provides a high voltage swing which is advantageous to drive a frequency divider or a mixer circuit. Figure 5.6 illustrates the design of the quadrature LC VCO with the two identical single VCOs presented in the thesis.

The design procedure for the single LC VCO is equally applied to the design of the quadrature LC VCO. Owing to the fact that the quadrature VCO operates at the same oscillation frequency of the single VCO, the same noise filter is exploited into the two identical single VCOs. The tank inductor for the quadrature VCO is adopted from the optimised inductor (2-turn 1.63 nH) designed in Chapter 3. To couple the two VCOs, the PMOS with the minimum 8 finger number equal to the PMOS pair is connected in parallel with the pair. The reason for using the PMOS transistors rather

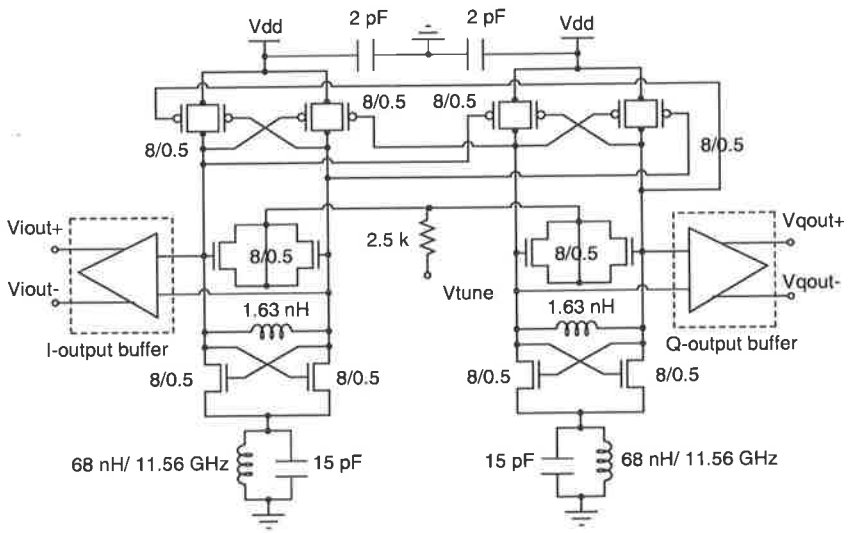


Figure 5.6: Final quadrature LC VCO schematic with noise filters.

than NMOS counterparts is related to the low noise characteristic. Since the coupling PMOS of each single VCO is connected to the tank circuit, the varactor capacitance of the tank circuit need to be adjusted in order to oscillate at the targeting frequency of 5.8 GHz. In consequence, the finger number of each tank varactor is reduced to 8, half the varactor finger number of the single VCO.

5.3 Single/Quadrature LC VCO Layout

The circuit layout of the single and quadrature LC VCOs is performed with Momentum layout editor [87] targeting Peregrine 0.5 μm 1-poly 3-metal SOS CMOS process (FC process). The design kit of the Peregrine FC process is based on the RF IC design flow of Cadence CAD tool package [88]. Due to unavailability of the Cadence CAD tool during the design phase, the design kit the author referred is only exploited for a schematic simulation with ADS device models and all of the layouts are manually laid out based on the design manual.

The design process does not take into account the testing environment provided that a mixer connected to the oscillator has an input buffer. This is due to the fact that

the buffer at the mixer input ports can be utilised to lower a loading effect by different output impedance. To consider the testing environment of the LC VCOs, a large resistors should be used at the output ports to diminish the effect of the output impedance, which is added in measuring the output power or phase noise with a 50 Ω test equipment. However, this approach significantly deteriorates the oscillator output power by the signal degradation. As a result, a buffering method can be utilised since the fluctuation of the oscillation frequency by loading the output impedance (pulling figure) can be minimised by the gate capacitance of the MOSFET buffer. This is because the gate capacitance of the buffer provides a much higher impedance compared to the output impedance of the VCO.

To accommodate the pad effect on the tuning frequency, 100 μm pads with a pad pitch of 150 μm are used as shown in Figure 5.7.

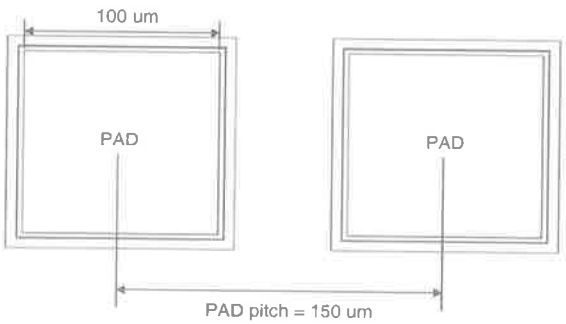


Figure 5.7: Pad pitch for microprobing.

In practical oscillators, a leakage current with a small noise power from the loop filter of a PLL can cause an unexpected frequency modulation on the varactor operation. In order not to induce such undesirable signals into the control input node, a poly-silicon (PS) resistor is used between the V_{tune} pad and the node for a control input of the tank varactor. The resistance of the PS resistor (R_{poly}) is determined by:

$$R_{\text{poly}} = \frac{L_p}{W_p} R_{\text{poly},\square}, \tag{5.10}$$

where W_p and L_p indicate the width and the length of each rectangle poly-silicon, respectively. Figure 5.8 shows the layout configuration of the PS resistor.

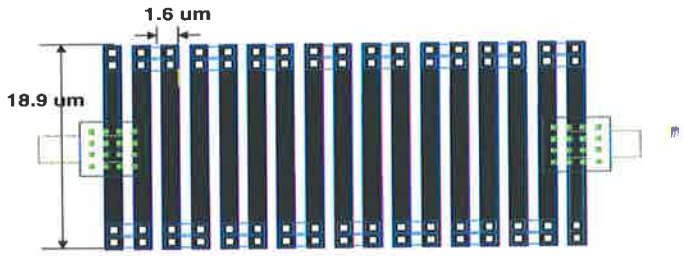


Figure 5.8: Poly-silicon resistor layout.

The sheet resistance ($R_{\text{poly},\square}$) of the rectangle poly is set to 12.5 $\Omega/\square$ with a unit width of 1.6 μm and a unit length of 18.9 μm. Therefore, the 2.5 kΩ is implemented with 17 rectangles of poly-silicons. Here, the exact resistance of the PS resistor is not important.

A 4-pF MiM capacitor consisted of 2 top metal layers on top of the VCO is used to bypass high frequency noise flowing through the power supply. Figure 5.9 shows the 4-pF MiM capacitor layout designed using a thicktop metal and metal-2 layers.

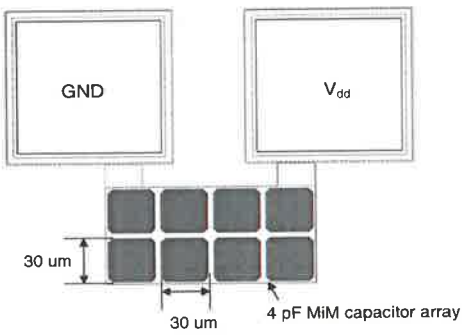


Figure 5.9: 4-pF MiM capacitor layout of the single VCO.

Since the MiM capacitor unit cell is flexible to adjust the dimension based on the unit capacitance (0.575 fF/μm^2), the unit area of 30 μm $\times$ 30 μm dimensions in the VCO design is chosen with 8 unit capacitors to make up 4-pF capacitance. In case of 15-pF MiM capacitor for the noise filter, the same approach is applied with 32 equal unit cells. The total capacitor area including the two top metals reaches 34,848 μm^2 (132 μm $\times$ 264 μm). Figure 5.10 shows the layout of the single LC VCO including the MiM bypass capacitor and the noise filter.

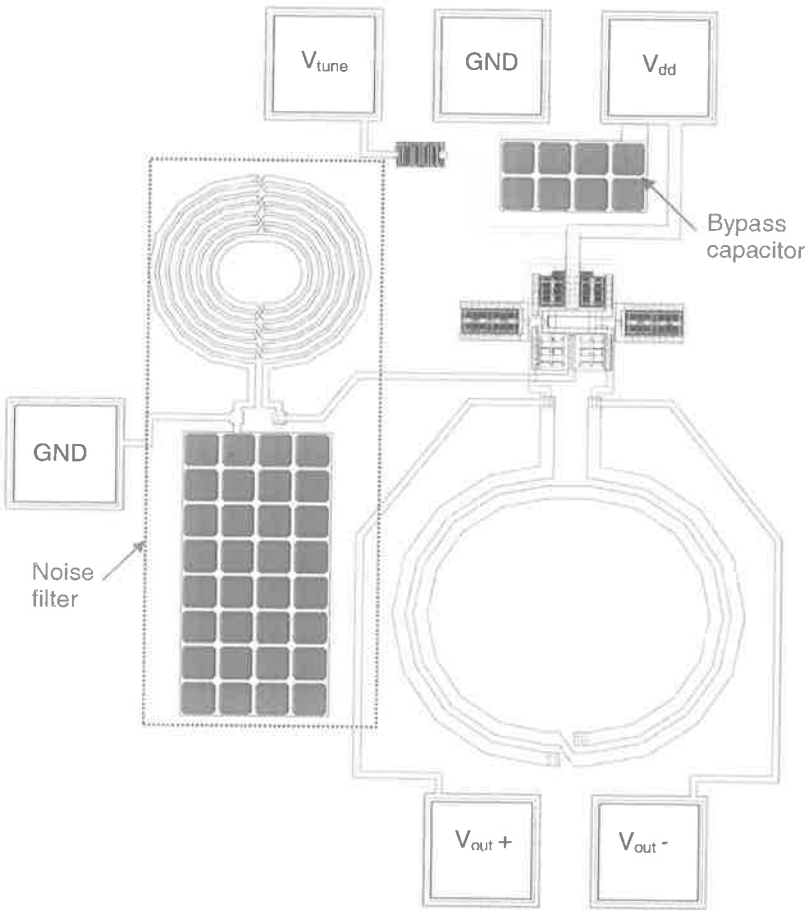


Figure 5.10: Single LC VCO layout.

The three pads on the top of the layout are for DC bias connection (V_{dd}), ground of the bypass capacitors (GND) and control input of the tank varactor (V_{tune}). The left pad is for connecting the noise filter composed of the 7-turn symmetric circular inductor and 15 pF MiM capacitor to the ground of the single LC VCO (GND). The bottom pads are for extracting the differential RF outputs ($V_{\text{out}+}$, $V_{\text{out}-}$) of the unbuffered VCO. The total oscillator area including the pads is 675 μm $\times$ 833.70 μm including all of the pads.

In the quadrature VCO, the majority of layout configuration of the single VCO has been used with minor changes. Although the two identical inductors of the noise filters

can be replaced with an equivalent one instead, they are used without modification for the symmetrical layout. The area efficiency to the total layout is also not much influenced by the two integrated inductors because the inductor is placed in the vacant area between the two signal paths for the differential outputs and the pads. Contrary to the 4-pF capacitor of the single VCO, the 4-pF MiM capacitor of the quadrature VCO is divided into two 2-pF MiM capacitors in parallel with regard to the power line (V_{dd}) for symmetry as shown in Figure 5.11.

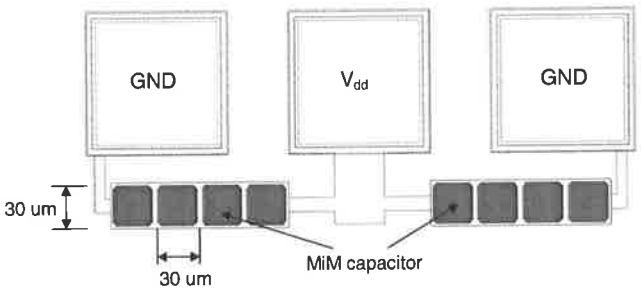


Figure 5.11: 4-pF MiM capacitor layout for the quadrature VCO.

The final quadrature VCO layout is shown in Figure 5.12.
For the quadrature outputs, both of the two top and bottom pads are assigned for extracting in-phase/quadrature output signals and the total area of the quadrature VCO is 1360 μm $\times$ 813 μm including all of the pads.

5.4 LC VCO EM Simulation

In spite of the great accuracy in 3D EM simulation, 2.5D EM simulator is preferable in case of analysis on plane-stacked structures such as a metalisation and a planar inductor. In particular, a metal strip modelling is effectively performed with relatively smaller memory and faster simulation on 2.5D EM environment.
Using quasi-3D modelling method introduced in Chapter 3, EM simulations for all designed LC VCOs are conducted. As previously mentioned, partial dielectric layers of integrated components such as MOSFETs or MiM capacitors are not modelled on 2.5D simulation environment. Consequently, the interconnecting metalisation of the

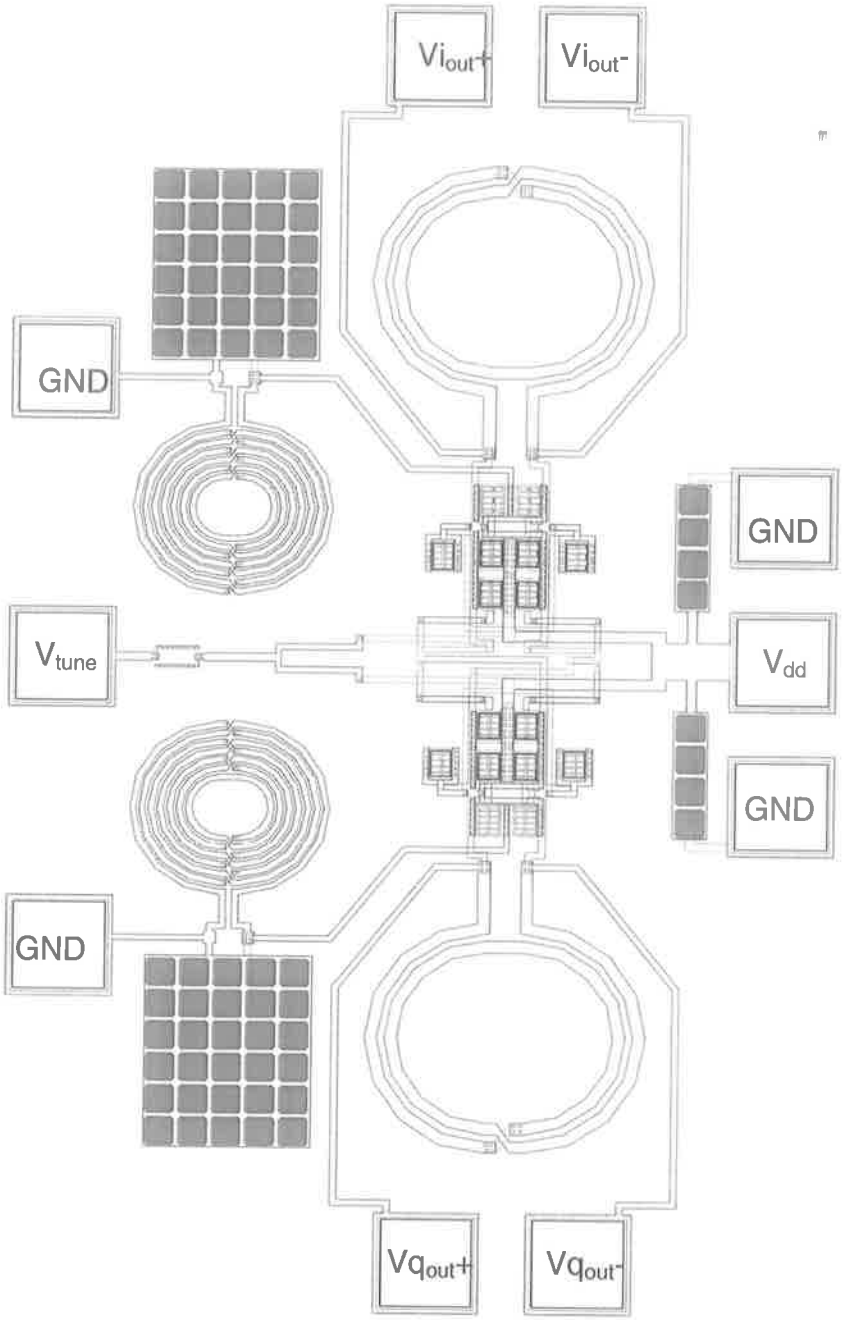


Figure 5.12: Quadrature LC VCO layout.

LC VCO layouts in this thesis is laid out for quasi-3D EM simulation and the active MOSFETs and MiM capacitors including the PS resistors are removed.

For an accurate reflection of the parasitic elements into the LC VCO operation, it is necessary to run the EM simulation on the whole layout structures including the integrated inductors. However, the layouts are divided into several subparts due to a limited physical memory available in the PC system and the swapping memory size [89]. This presents a bottleneck for the EM simulation in this thesis. These issues are caused from the quasi-3D modelling and numerously tiny structures meshed to calculate interaction between ports. In addition, they are dependant on the simulation setup of the mesh density, frequency bands swept and arc resolution.

To simulate with limited system resources (4 GB physical memory on a Solaris machine), the layout of the quadrature oscillator is split into subparts with a minimum effect on the net parasitic capacitance and resistance. In case of the single VCO, all the layouts except the noise filtering inductor could be simulated using the system resources as shown in Figures 5.13.

All pads are included to consider their effects (pad capacitance) on the oscillation frequency. In case of metal layers in parallel, they are simulated together if possible after cutting to the end of the parallel layers to take the capacitance between the layers into consideration. To prepare for the oscillation frequency deviation by the capacitance of the VCO layout metalisation, all of the monolithic inductors are separately simulated since it is not straightforward to calculate the capacitance of the metalisation. At the edge of each divided metalisation, all of the ports are assigned in the middle of the edge to ease the interconnection between the divided layout components for co-simulation. To connect MOSFET device models to metal layers for tuning bias voltage including power supply, the ports are allocated in the center of the interconnecting metalisation and the pads.

In case of the quadrature VCO, the whole layout is divided into three subparts as shown in Figures 5.14, 5.15 and 5.16.

Compared to the case of the single VCO, the signal lines connecting the two identical VCOs are divided to prevent the usage of excessive physical memory by the simulator. Besides, the inductors for the noise filter and tank circuit are separated from the layout

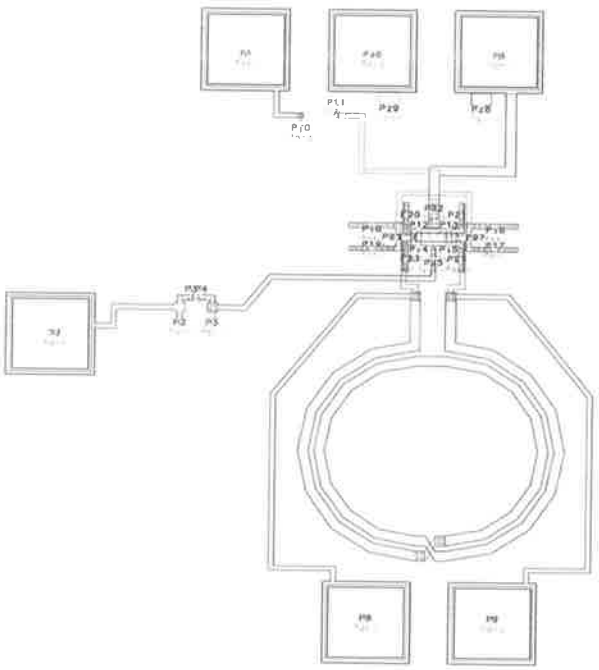


Figure 5.13: Layout of the single LC oscillator except the noise filtering inductor.

to tune the design parameters during the EM simulation phase.

5.5 Co-simulation Results

With the S-parameter simulation results, the subdivided layout components and symmetric inductors are co-simulated with the SOS FET device models including the MiM capacitor and PS resistor. Figures 5.17 and 5.18 illustrate the single and quadrature LC oscillator layout configurations for co-simulation, respectively.

As presented in Chapter 4, 1.4 Ω and 1.2 Ω resistors are connected to the gate port and drain/source ports of all active devices, individually to reflect the effect of the contact resistance for the single and quadrature LC VCOs in the co-simulations. The IP-6.8 μm model presented in Chapter 4 is utilised for the tank varactor of the single and quadrature LC VCOs.

Figures 5.19 5.20 and 5.21 5.22 illustrate the performances of the single and quadrature

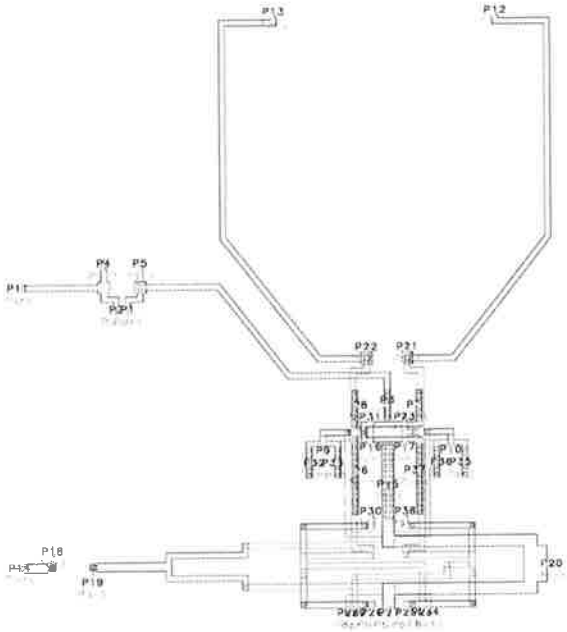


Figure 5.14: Subdivided quadrature LC oscillator layout: part I.

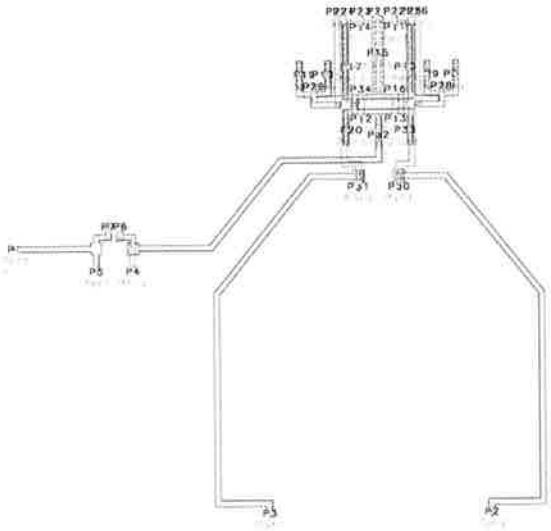


Figure 5.15: Subdivided quadrature LC oscillator layout: part II.

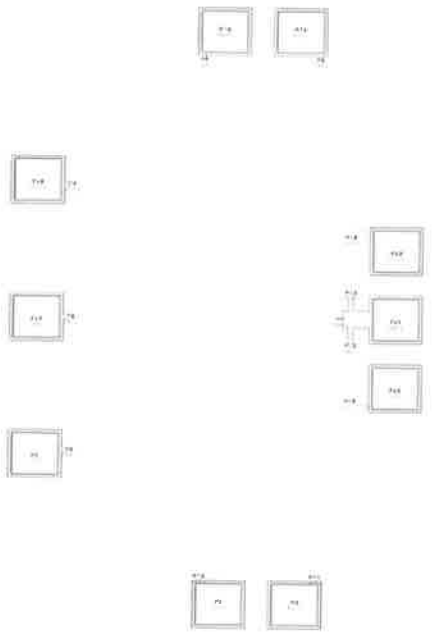


Figure 5.16: Subdivided quadrature LC oscillator layout: part III.

LC oscillators. Since the down-converted second harmonic affects phase noise performance of LC VCOs, it is desirable to diminish the harmonic power. As for suppression of the second harmonic, maximum -41.623 dB power at 12.03 GHz exhibits in 0.3 V_{tune} in case of the single LC VCO. At 11.06 GHz, the power is suppressed to minimum -49.904 dB for both of the differential outputs, $V_{\text{out}+}$ and $V_{\text{out}-}$. The differential outputs swing 0.450 V_{peak} to -0.447 V_{peak} at 6.268 GHz while the amplitudes are reduced to $\pm$ 0.343 V_{peak} at 5.532 GHz. The best phase noise performance of -119.352 dBc/Hz at 3 MHz offset frequency also exhibits in 0 V_{tune}. A wide tuning range of 736 MHz and the lowest power consumption of 0.42 mW ($I_{\text{bias}} \approx 0.52$ mA) are achieved within 0.0 - 0.8 V tuning bias range.

The quadrature VCO relatively has a better performance in terms of the harmonic suppression by around minimum -6 to maximum -28 dB than that of the single VCO for the both in-phase and quadrature differential outputs. The peak-to-peak voltage of the differential quadrature outputs ($V_{\text{qout}+}$, $V_{\text{qout}-}$) swings between 0.267 and -0.267 V at 5.927 GHz (0.167 and -0.167 V at 5.626 GHz) while inphase (I) signals expose

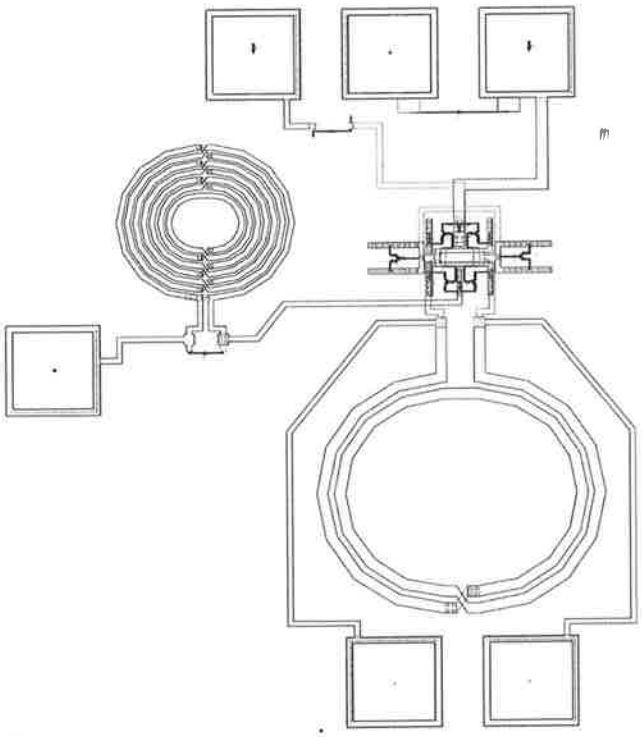


Figure 5.17: Single VCO layout configuration for the co-simulation.

the lower swing amplitude of 0.232 to -0.232 V (± 0.148 V at 5.626 GHz) at the same frequency (which is not shown for simplicity.). The harmonic suppression also shows a different power distribution. This difference is probably caused by the division of the signal lines between the two identical VCOs to reduce the usage of the physical memory[6].

In addition, capacitance distribution between metal layers for ground and differential output of each single VCO can cause the different output signal power[7]. Due to the coupling PMOS pair, the quadrature LC VCO has a narrower tuning range of 301 MHz

[6]The core layout of the quadrature VCO except the tank inductor and the noise filter requires more than 3.7 GB physical memory for initial startup memory and the memory usage gradually increases to more than 5 GB during the EM simulation. Since Solaris OS also has a problem in swapping a virtual memory like in Windows OS, the simulation has been failed for this reason.

[7]In this case, a dummy metal layer connecting to a pad for ground is advantageous to alleviate the difference of the output power.

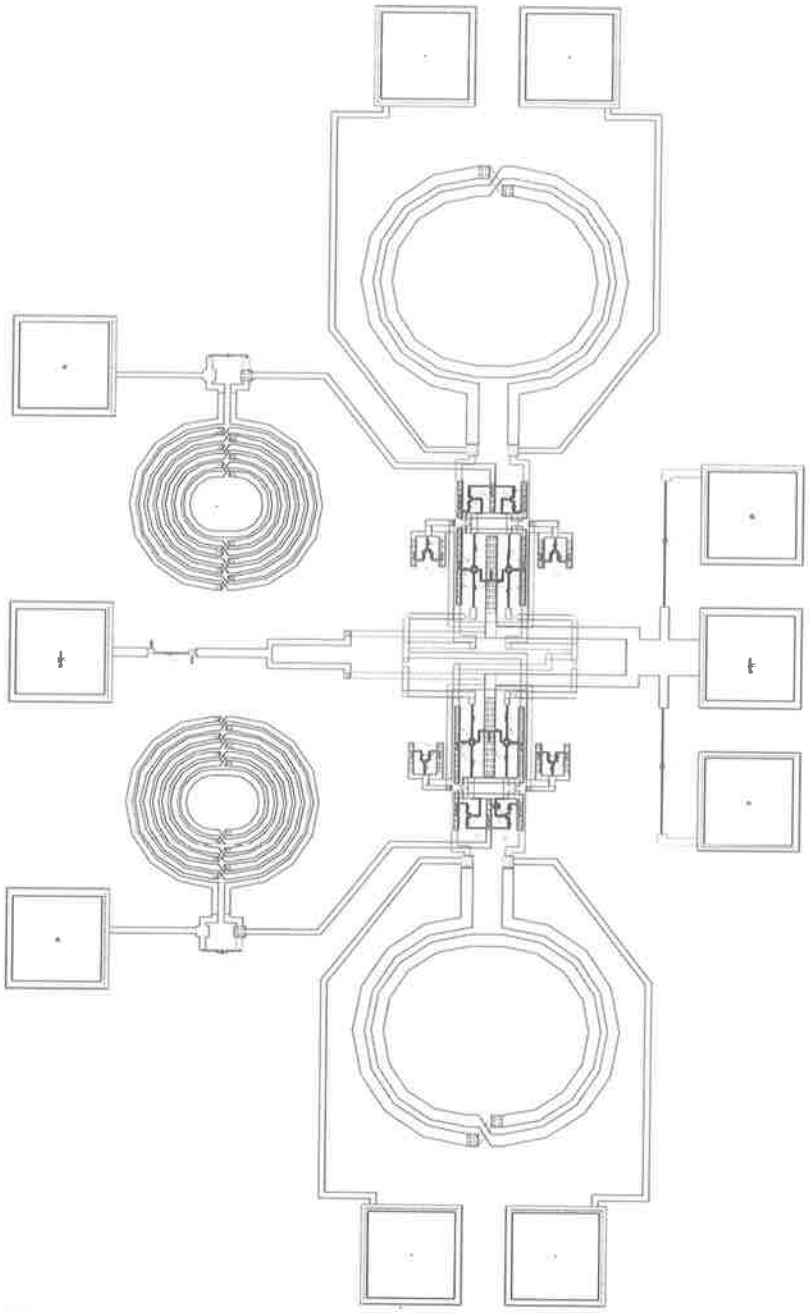
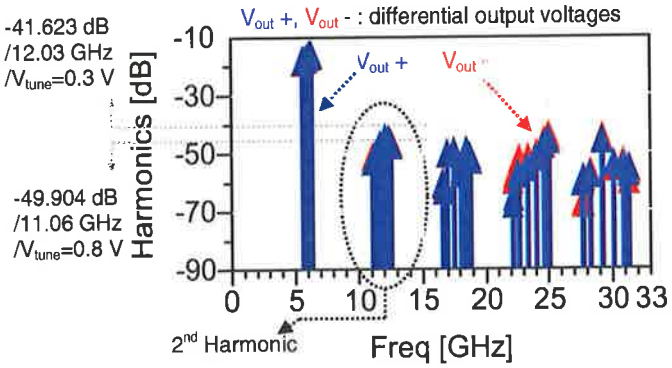
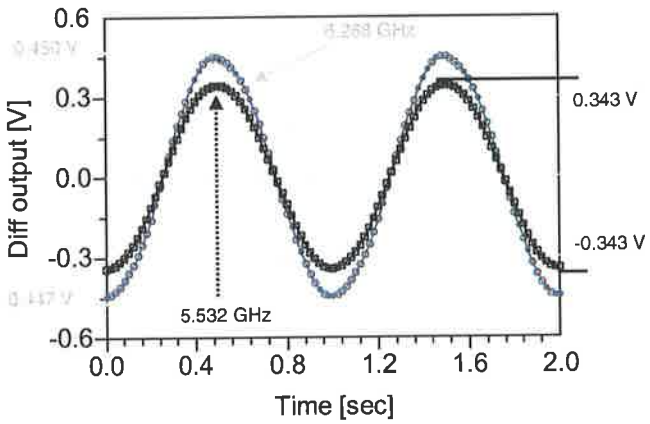


Figure 5.18: Quadrature VCO layout configuration for the co-simulation.



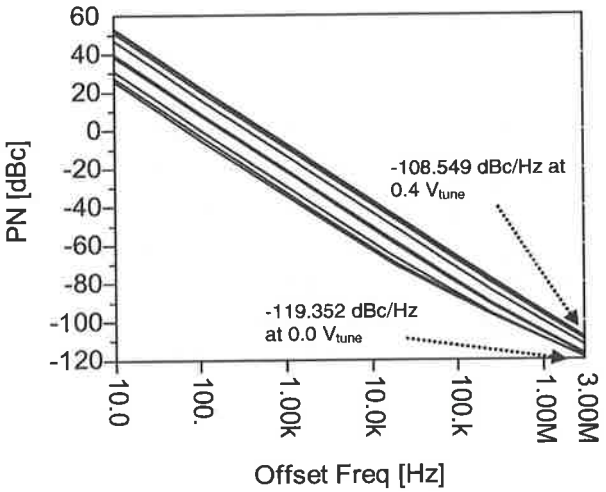
This figure illustrates harmonic suppression of differential output signals up to 5th harmonics. The blue and red arrows indicate the signal power of V_{out}+ and V_{out}-, respectively. In case of 2nd harmonic, the harmonic signal power has a maximum value of –41.623 dB at 12.03 GHz in 0.3 V tuning bias voltage (V_{tune}). Meanwhile, it is minimized to –49.904 dB at 11.06 GHz in 0.8 V_{tune}.

(a) Harmonic suppression (up to 5th order).



This figure shows differential output signals (i.e. (V_{out}+) – (V_{out}-)) at the highest (6.268 GHz) and lowest (5.532 GHz) tuning frequencies. At 6.268 GHz, the swing amplitude (grey curve) of V_{peak} to -V_{peak} is about 0.9 V. Meanwhile, the peak-to-peak differential signal amplitude (black curve) reaches around 0.69 V at 5.532 GHz.

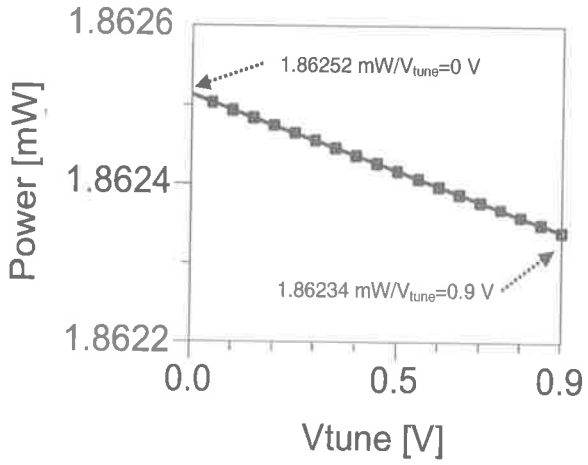
(b) Differential output signals.



This figure depicts the phase noise performance of the single LC VCO at 3 MHz offset frequency. A tuning bias voltage (V_{tune}) of 0.8 V is applied to the tank varactor with 0.1 sweeping mode. At 0.0 V_{tune}, the lowest phase noise of -119.352 dBc/Hz is obtained while the highest value of -108.549 dBc/Hz occurs at 0.4 V_{tune}.

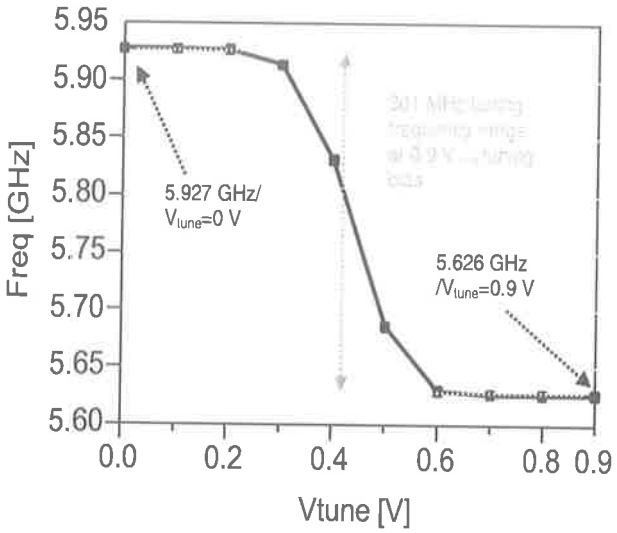
(c) Phase noise at 3 MHz offset.

Figure 5.19: Performance of the single LC oscillator (I).



This figure shows the power consumption of the quadrature LC VCO according to the tuning bias range. The highest power consumption of 1.86252 mW exhibits at 0 V_{tune} while the lowest power consumption of 1.86234 mW occurs at V_{tune}=0.9 V. By the coupling PMOS, the bias current is increased four times (~2.07 mA) compared to the single LC VCO. Similarly to the single LC VCO, the variation of the power dissipation (~0.18 uW) is negligible.

(a) VCO power consumption.



This figure shows the tuning frequency range of the quadrature LC VCO according to the same tuning bias range (0.9 V_{tune}). Due to the coupling PMOS, the available frequency range is reduced and the finger number of the tank varactor is set to 8 to satisfy the tuning requirement. This LC VCO has a narrower tuning range of 301 MHz (~5.2 %) with the same voltage range to the power supply.

(b) Tuning frequency range (0-0.9 V_{tune}).

Figure 5.22: Performance of the quadrature LC oscillator (II).

with an increased power supply voltage of 0.9 V. With the phase noise of -115.7 dBc/Hz at 3 MHz offset, a low power of 1.86 mW ($I_{\text{bias}} \approx 2.07$ mA) is achieved in the tuning range of 0.9 V. Note that the single and quadrature LC VCOs can be further optimised for a specific PVT (process/voltage/temperature) corner[8].

[8]This is because harmonic content can rise (or output power can fall) to unacceptable levels by the PVT corner. Also, it can make the circuit unstable for practical applications.

Chapter 6

Conclusions and Future Work

This chapter discusses the results of the voltage-controlled oscillator (VCO) designs. The ultimate purpose of this research is to develop an LC VCO IP core with low power and low phase noise for a high performance RF radio-on-chip (ROC). Compared to VCO performance published in the literature, the designed LC VCOs exhibits superior performance in terms of figure of merit (FOM) with phase noise and power consumption. Integrated in a phase-locked loop (PLL), the single and quadrature LC VCOs can be employed as a local oscillator for mobile applications operating at 5.8 GHz (IEEE 802.11 a).

6.1 Conclusions

The low phase noise of -119.35 dBc/Hz at 3 MHz offset frequency is achieved with the single LC oscillator with 736 MHz tuning frequency. The VCO core draws a low current of 0.52 mA at 0.8 V power supply voltage resulting in 0.42 mW of power consumption. The output power ranges from -2.833 dBm to -5.108 dBm in case of V_{out+} while V_{out-} has a output power from -3.091 dBm to -5.360 dBm depending on the tuning voltage (0.0 V to 0.8 V). From the definition of FOM presented in Chapter 2, the single LC oscillator performs:

$$\begin{aligned} \text{FOM}_{\text{single}} &= -|L\{\Delta f\}| + 10\log\left[\frac{P_{DC}}{P_{\text{ref}}} \times \left(\frac{\Delta f}{f_0}\right)^2\right] \\ &= -119.35 + 10\log\left[0.42 \times \left(\frac{3}{5.879 \times 10^3}\right)^2\right] \\ &\approx -189 \text{ dB}. \end{aligned} \tag{6.1}$$

The designed quadrature VCO has a 301 MHz tuning range, dissipates a low power of 1.86 mW at 0.9 V supply voltage and achieves -115.7 dBc/Hz phase noise performance at 3 MHz offset. The output power of the quadrature signal demonstrates -7.44 dBm to -11.54 dBm, while the in-phase output power exhibits -8.67 dBm to -12.55 dBm within the 0.9 V tuning range. The FOM of the quadrature LC oscillator becomes:

$$\begin{aligned} \text{FOM}_{\text{quad}} &= -115.7 + 10\log\left[1.86 \times \left(\frac{3}{5.78 \times 10^3}\right)^2\right] \\ &\approx -178.7 \text{ dB}. \end{aligned} \tag{6.2}$$

The FOM table presented in Chapter 1 is revised to compare the performance of the two VCOs with others presented in the literature.

From the revised FOM table, only the work by Hegazi *et al.* [24] which is the highest among the literature to date demonstrates a better performance by 6 dB. It is worth noting that the power consumptions of the single and quadrature LC VCOs presented in this work are recorded as the lowest values. Furthermore, the phase noise performance of the two oscillators is relatively exceptional compared to power consumption and fundamental frequencies. At the time of this writing, no competitive commercial product is available around the 5.8 GHz band. A discrete 5.2 GHz VCO module has recently been released by Vari-L [90]. It is characterized by 37.5 mW power consumption (7.5 mA bias current at 5 V power supply voltage) with -105 dBc/Hz at 100 kHz. The FOM is approximately -183.6 dB, which is lower than the single VCO by 5 dB.

6.2 Future Work

The work presented in this thesis is based on schematic and EM simulations. To consider the effects of actual operation, all possible parasitics are reflected into the

Table 6.1: Comparison of the revised FOM from Table 1.1.

	f_0 [GHz]	$L\{\Delta f\}$ [dBc/Hz]	Δf [kHz]	Type	P_{DC} [mW]	FOM
Hegazi [24]	1.2	-153	3000	LC/CMOS035	9.25	-195.4
Single[this work]	**5.879**	**-119.35**	**3000**	**LC/SOS-CMOS05**	**0.42**	**-189.0**
191-2750U [25]	2.75	-113	100	Module	21	-188.6
Wang [26]	9.8	-118	1000	LC/CMOS035	12	-187.0
Huang [27]	0.926	-112	100	LC/Ext/CMOS04	4.7	-184.6
Kinget [28]	2.45	-124	1000	LC/CMOS035	5.4	-184.5
Craninckx [29]	1.8	-113	200	LC/CMOS04	9.0	-182.5
Quad[this work]	**5.78**	**-115.7**	**3000**	**LC/SOS-CMOS05**	**1.86**	**-178.7**
Plouchart [30]	6.0	-116	1000	LC/SiGe	22	-178.1
Dauphinee [31]	1.5	-105	100	LC/Bip/BiCMOS08	28	-174.1
Rofougaran [32]	0.82	-100	100	LC/Etch/CMOS1	25	-164.3
Razavi [33]	1.8	-100	500	LC/Coup/CMOS06	7.6	-162.3
Kwasniewski [34]	0.74	-89.0	100	Ring/CMOS12	6.5	-158.3
Hajimiri [35]	2.810	-95.2	1000	Ring/CMOS025	10	-154.2

In Table 6.1, the figures used for comparing "this work" are the best-figures from Figures 5.19(c) and 5.21(c). Also, figures from other literature in the Table are measured values. Hence, the FOM figures of the single and quadrature LC VCOs obtained from simulations can be more optimistic when compared to the measured FOMs.

design procedure at a given circumstance. Generally as the extraction job of the parasitic components after laying out IC designs is performed in a low frequency band, measurements might be inaccurate compared to those of the post layout simulation. This is due to the fact that the parasitics are frequency dependant. This dependance becomes a critical factor in designing RF IC products. Therefore, designing RF oscillators at the real oscillation frequency band can be more effective through modelling the metalisation and passive devices.

Meanwhile, dividing the VCO layouts was inevitable to avoid overloading the limited system resources during the EM simulation. Such division can influence the simulation result and make it deviate from the expected outcome. The layout effect of the

Appendix A

Analysis on Q Enhancement of a Symmetric Inductor

A.1 Single-Ended Inductor

In a single-ended inductor, the small signal model can be derived using a 1-port network easily compared to a symmetric inductor. Since one port of the inductor is grounded, it can be simplified as shown in Figure A.1.

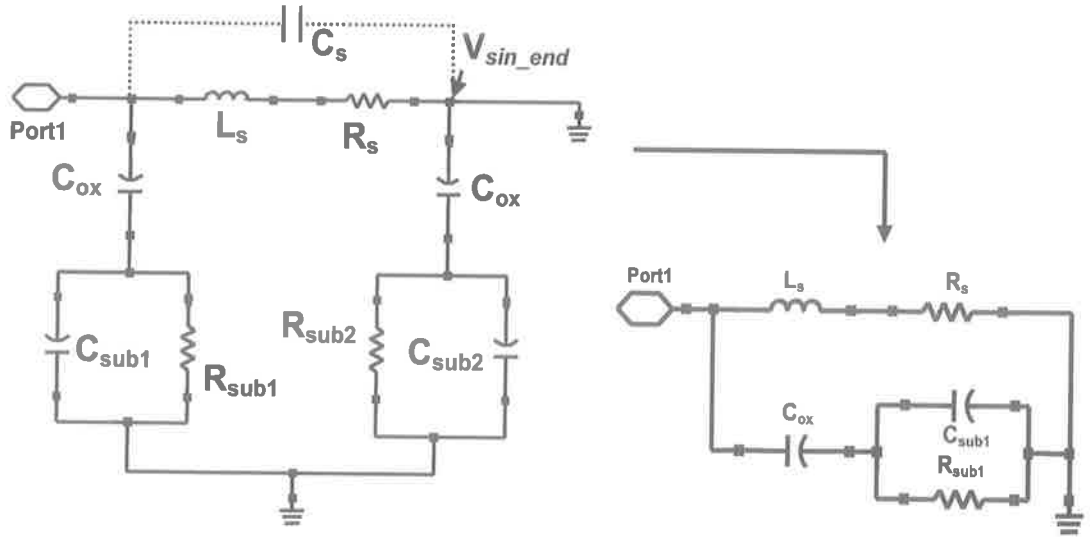
Generally, the series capacitance (C_s) parameter has a small value (several tens fF), which tends to be neglected in considering the composing components of lumped inductor models. For accuracy, C_s can be included in the small signal model, but it is omitted for simplicity here[1]. In Figure A.1, C_{ox} indicates silicon oxide film, and C_{sub} and R_{sub} represent substrate capacitance and substrate resistance.

Node $V_{\text{sin\_end}}$ is electrically zero, which causes C_{ox}, C_{sub2} and R_{sub2} to short. Looking into the passive network in terms of admittance, the series admittance ($Y_{\text{s\_sin\_end}}$) and the substrate admittance ($Y_{\text{sub\_sin\_end}}$) of a single-ended inductor can be derived by:

$$Y_{\text{s\_sin\_end}} = \frac{1}{R_s} // \frac{1}{j\omega L_s} = \frac{1}{R_s + j\omega L_s} \tag{A-1}$$

$$Y_{\text{sub1\_sin\_end}} = \frac{1}{R_{\text{sub1}}} + j\omega C_{\text{sub1}} \tag{A-2}$$

[1]For reference, C_s can be derived from an inductance (L_{srf}) at self resonant frequency (F_{srf}) and R_s from an impedance at low frequencies.



(a) (b)

Figure A.1: Simplified small signal model of a single-ended inductor.

$$Y_{\text{sub\_sin\_end}} = j\omega C_{ox} // Y_{\text{sub1\_sin\_end}} = \frac{j\omega C_{ox} - \omega^2 C_{ox} C_{\text{sub1}} R_{\text{sub1}}}{1 + j\omega R_{\text{sub1}}(C_{ox} + C_{\text{sub1}})}. \tag{A-3}$$

Accordingly, the total admittance ($Y_{\text{sin\_end}}$) is:

$$\begin{aligned} Y_{\text{sin\_end}} &= Y_{\text{s\_sin\_end}} + Y_{\text{sub\_sin\_end}} = \frac{1}{R_s + j\omega L_s} + \frac{j\omega C_{ox} - \omega^2 C_{ox} C_{\text{sub1}} R_{\text{sub1}}}{1 + j\omega R_{\text{sub1}}(C_{ox} + C_{\text{sub1}})} \\ &= \frac{R_s - j\omega L_s}{R_s^2 + \omega^2 L_s^2} + \frac{\omega^2 R_{\text{sub1}} C_{ox}^2 + j\omega C_{ox}(1 + \omega^2 R_{\text{sub1}}^2 C_{\text{sub1}}(C_{ox} + C_{\text{sub1}}))}{1 + \omega^2 R_{\text{sub1}}^2 (C_{ox} + C_{\text{sub1}})^2} \\ &= \frac{R_s}{R_s^2 + \omega^2 L_s^2} + \frac{\omega^2 R_{\text{sub1}} C_{ox}^2}{1 + \omega^2 R_{\text{sub1}}^2 (C_{ox} + C_{\text{sub1}})^2} + j\left[\frac{-\omega L_s}{R_s^2 + \omega^2 L_s^2} + \right. \\ &\left. \frac{\omega C_{ox}(1 + \omega^2 R_{\text{sub1}}^2 C_{\text{sub1}}(C_{ox} + C_{\text{sub1}}))}{1 + \omega^2 R_{\text{sub1}}^2 (C_{ox} + C_{\text{sub1}})^2}\right]. \end{aligned} \tag{A-4}$$

If the $Y_{\text{sin\_end}}$ is rearranged at low and high frequencies,

I. At low frequency

assuming the conditions that $R_s \gg \omega L_s$ and $1 \gg \omega R_{\text{sub1}}(C_{ox} + C_{\text{sub1}})^2$, $Y_{\text{sin\_end}}$ can be approximated as[3]:

$$Y_{\text{sin\_end}} \simeq \frac{1}{R_s} + \omega^2 R_{\text{sub1}} C_{ox}^2 + j\omega\left(C_{ox} - \frac{L_s}{R_s^2}\right). \tag{A-5}$$

II. At high frequency

assuming the conditions that $R_s \ll \omega L_s$ and $1 \ll \omega R_{\text{sub1}}(C_{ox} + C_{\text{sub1}})^4$, $Y_{\text{sin\_end}}$ can be approximated as:

$$Y_{\text{sin\_end}} \simeq \frac{R_s}{\omega^2 L_s^2} + \frac{1}{R_{\text{sub1}}}\left(\frac{C_{ox}}{C_{ox} + C_{\text{sub1}}}\right)^2 + j\left(\omega\frac{C_{ox}C_{\text{sub1}}}{C_{ox} + C_{\text{sub1}}} - \frac{1}{\omega L_s}\right). \tag{A-6}$$

At low frequency bands, the oxide capacitance (C_{ox}) works as an open circuit and the impedance of the single-ended inductor is dominated by the series resistance (R_s) and inductance (L_s). Meanwhile, the parasitic components such as C_{sub1} and R_{sub1} affect the impedance value at high frequency bands.

A.2 Symmetric Inductor

Contrary to the single-ended inductor, a symmetric inductor should consider both ports and the simplified model can be formed as in Figure A.2(a)[5].

Since the voltage phase at two ports is out of phase, a parallel network constituted of C_{sub1} and R_{sub1} is in series with the equivalent of C_{sub2} and R_{sub2}. For the purpose of analysis on the same environment and for simplicity, the simplified model is reformed as in Figure A.2(b).

[2]Such presumed conditions are used for comparison on the performance of single-ended and symmetric inductors in terms of admittance at low and high frequency bands. The relevance of the assumptions is determined by the component parameters depending on the operation frequencies of the inductors.

[3]Basically, the effect of C_{ox} and C_{sub1} are negligible (high impedance path) at low frequency. Therefore, the equivalent circuit can be simplified to a series L_s and R_s which could be easily derived from the real and imaginary part of the impedance.

[4]Refer to the footnote 2.

[5]To simplify the analysis of the two inductors, it is assumed that the parasitic components such as substrate capacitance and resistance have the same values.

I. At low frequency

$$\begin{aligned} Y_{\text{sin\_end}} - Y_{\text{sym}} &\simeq \frac{1}{R_s} + \omega^2 R_{\text{sub1}} C_{ox}^2 + j\omega\left(C_{ox} - \frac{L_s}{R_s^2}\right) - \left[\frac{1}{R_d} + \omega^2 R_1 C_1^2 + \right. \\ &\quad \left. j\omega\left(C_1 - \frac{L_d}{R_d^2}\right)\right] \\ &= \frac{1}{R_s} - \frac{1}{R_d} + \frac{1}{2}\omega^2 R_{\text{sub1}} C_{ox}^2 + j\omega\left(\frac{1}{2}C_{ox} + \frac{L_d}{R_d^2} - \frac{L_s}{R_s^2}\right). \end{aligned} \tag{A-12}$$

Assuming that $R_d = R_s$ and $L_d = L_s$ for simplicity in comparison, then:

$$Y_{\text{sin\_end}} - Y_{\text{sym}} \simeq \frac{1}{2}\omega^2 R_{\text{sub1}} C_{ox}^2 + j\frac{1}{2}\omega C_{ox}. \tag{A-13}$$

II. At high frequency

$$\begin{aligned} Y_{\text{sin\_end}} - Y_{\text{sym}} &\simeq \frac{R_s}{\omega^2 L_s^2} + \frac{1}{R_{\text{sub1}}}\left(\frac{C_{ox}}{C_{ox} + C_{\text{sub1}}}\right)^2 + j\left(\omega\frac{C_{ox}C_{\text{sub1}}}{C_{ox} + C_{\text{sub1}}} - \frac{1}{\omega L_s}\right) - \\ &\quad \left[\frac{R_d}{\omega^2 L_d^2} + \frac{1}{R_1}\left(\frac{C_1}{C_1 + C_2}\right)^2 + j\left(\omega\frac{C_1 C_2}{C_1 + C_2} - \frac{1}{\omega L_d}\right)\right] \\ &= \frac{1}{\omega^2}\left(\frac{R_s}{L_s^2} - \frac{R_d}{L_d^2}\right) + \frac{1}{2R_{\text{sub1}}}\left(\frac{C_{ox}}{C_{ox} + C_{\text{sub1}}}\right)^2 + \\ &\quad j\left[\frac{1}{\omega}\left(\frac{1}{L_d} - \frac{1}{L_s}\right) + \left(\frac{\omega}{2}\frac{C_{ox}C_{\text{sub1}}}{C_{ox} + C_{\text{sub1}}}\right)\right] \\ &\simeq \frac{1}{2R_{\text{sub1}}}\left(\frac{C_{ox}}{C_{ox} + C_{\text{sub1}}}\right)^2 + j\omega\left(\frac{1}{2}\frac{C_{ox}C_{\text{sub1}}}{C_{ox} + C_{\text{sub1}}}\right). \end{aligned} \tag{A-14}$$

At low frequency bands, the admittance difference can be neglected in Eq.(A-12) due to C_{ox} works as an open circuit. In other words, the impedances between the two inductors have a nearly similar value. In the meantime, Eq.(A-14) shows $Y_{\text{sin\_end}} - Y_{\text{sym}}$ has an increased value at high frequency bands due to the fact that a larger impedance path of the symmetric inductor is formed in the substrate layer. Consequently, induced energy loss by substrate current is diminished at high frequencies and the inductor Q is improved compared to the single-ended inductor.

A.4 Derivation of the Lumped Model Parameters

For extracting the lumped model parameters of the symmetric inductor, Z_d at low frequency can be written as:

$$Z_d = R_d + j\omega L_d$$

At high frequency,

$$\begin{cases} Z_2 = 1/(j\omega C_2) \\ Z_1 = R_1//C_2 = (G_1 + j\omega C_2)/(G_1^2 + \omega^2 C_2^2), \text{ where } G_1 = 1/R_1 \\ Z_c = Z_1 + Z_2 \\ Z = Z_d//Z_c = Z_d Z_c/(Z_d + Z_c) \end{cases}$$

Once Z_d is known, Z_c can be obtained as:

$$Z_c = ZZ_d/(Z_d - Z) \tag{A-15}$$

$$Z_c = \frac{G_1}{G_1^2 + (\omega C_2)^2} - j\left(\frac{\omega C_2}{G_1^2 + (\omega C_2)^2} + \frac{1}{\omega C_1}\right). \tag{A-16}$$

Taking the inverse of the real part of Z_c:

$$1/\mathrm{Re}(Z_c) = \omega^2 C_2^2/G_1 + G_1,$$

which is a linear equation. Plotting the above equation as a function of ω^2, the interception point with the y-axis defines G_1, which is the gradient of the curve provides C_2^2/G_1.

From C_2 and G_1, C_1 can easily be found from the imaginary part of Z_c.

Appendix B

ASITIC Technology File for Silicon-on-Sapphire On-Chip Inductors

ASITIC (analysis and simulation of inductors and transformers in integrated circuits) has been developed to simulate and analyze integrated planar inductors by Ali M. Niknejad of UC Berkeley [65]. ASITIC can be exploited to generate a variety of complicated inductor geometries, and used to estimate the inductance and quality factor of the planar inductors before simulation using a 2.5D EM simulator, i.e. Momentum of Agilent. However, EM simulation is less accurate because it is developed for 2D field structures. In addition, electromagnetic effects via upper and lower metals or eddy current in the substrate are not reflected into the simulation results. As a result, ASITIC is only used for inductance estimation.

```
< chip>

chipx = 1024                    ; dimensions of the chip in x direction
chipy = 1024                    ; dimensions of the chip in y direction
fftx = 256                      ; x-fft size (must be a power of 2)
ffty = 256                      ; y-fft size
TechFile = utsi05.tek           ; technology file name
TechPath = .                    ; technology file path
```

UTSi SOS 0.5 um technology file for ASITIC.

```
< layer> 0                  ; sapphire substrate layer
rho = 1· e^14               ; sapphire resistivity/Ω-cm
t = 650                     ; sapphire thickness/microns (μm)
eps = 9.39                  ; sapphire relative permittivity[1]

< layer> 1                  ; total oxide layer
rho = 1 · e^16              ; SiO2 resistivity
t = 9.35                    ; total thickness of the oxide layer (μm)
eps = 3.9                   ; SiO2 relative permittivity

< metal> 0                  ; poly silicon layer
layer = 1                   ; in the oxide layer
rsh = 9.9 · e^3             ; referred to MOSIS website (mΩ/square)
t = 0.37                    ; referred to Peregrine design manual
d = 0.0                     ; distance from the bottom of the oxide layer (μm)
name = poly1                ; assigned name for the poly silicon layer
color = green               ; color for the poly layer in ASITIC

< via> 0                    ; poly silicon layer to metal 1 layer
top = 1                     ; upper metal layer (metal 1)
bottom = 0                  ; lower metal layer (poly silicon layer)
r = 4                       ; *arbitrary resistance per via
width = 0.6                 ; square via width (μm)
space = 0.8                 ; minimum spacing between vias (μm)
overplot1 = .4              ; poly layer enclosure of via 0
overplot2 = .3              ; metal 1 layer enclosure of via 0
name = contact              ; assigned name for the via layer
color = blue                ; color for the via layer

< metal> 1                  ; metal 1 layer
layer = 1                   ; in the oxide layer
rsh = 48                    ; sheet resistance (mΩ/square)
t = 0.85                    ; metal 1 thickness (μm)
d = 1.22                    ; distance from the bottom of the oxide layer (μm)
name = metal1               ; assigned name for the metal 1 layer
color = yellow              ; color for the metal 1 layer in ASITIC

< via> 1                    ; metal 1 to metal 2 layer
top = 2                     ; upper metal layer (metal 2)
bottom = 1                  ; lower metal layer (metal 1)
r = 3                       ; *arbitrary resistance per via
width = 0.6                 ; square via width (μm)
```

```
space = 0.7                    ; minimum spacing between vias (μm)
overplot1 = .4                 ; metal 1 layer enclosure of via 0
overplot2 = .4                 ; metal 2 layer enclosure of via 0
name = via1                    ; assigned name for the via layer
color = brown                  ; color for the via layer

< metal> 2                     ; metal 2 layer
layer = 1                      ; in the oxide layer
rsh = 31                       ; sheet resistance (mΩ/square)
t = 1.08                       ; metal 2 thickness (μm)
d = 3.57                       ; distance from the bottom of the oxide layer (μm)
name = metal2                  ; assigned name for the metal 2 layer
color = gray                   ; color in ASITIC

< via> 2                       ; metal 2 to metalthick layer
top = 3                        ; upper metal layer (metalthick)
bottom = 2                     ; lower metal layer (metal 2)
r = 2                          ; *arbitrary resistance per via
width = 3.0                    ; square via width
space = 3.0                    ; minimum spacing between viathick layers
overplot1 = 0.1                ; metal 2 layer enclosure of via 1
overplot2 = 0.1                ; thick metal layer enclosure of via 1
name = viathick
color = white

< metal> 3                     ; metalthick layer
layer = 1                      ; in the oxide layer
rsh = 9                        ; sheet resistance (mΩ/square)
t = 3.1                        ; metalthick layer thickness (μm)
d = 5.70                       ; distance from the bottom of the oxide layer (μm)
name = metalthick              ; assigned name for the metalthick layer
color = purple                 ; color for the metalthick layer in ASITIC
```

*No effect by via layers to estimate inductor Q factor is considered in ASITIC.

Bibliography

[1] T. Weigandt, "Integrated VCO/Synthesizer Design for a Monolithic CMOS RF Receiver," *Qualifying Exam, EECS of UC at Berkeley*, October 1995 (`http://kabuki.eecs.berkeley.edu/%7Eweigandt/slides/quals_talk/`).

[2] T. I. Ahrens and T. H. Lee, "A 1.4 GHz 3 mW CMOS LC Low Phase Noise VCO Using Tapped Bond Wire Inductance," *International Symposium on Low Power Electronics and Design*, pp. 16–19, August 1998.

[3] S. H. Seok, C. Nam, W. S. Choi, and K. Chun, "A High Performance Solenoid-type MEMS Inductor," *Journal of Semiconductor Technology and Science*, vol. 1, no. 3, pp. 182–188, September 2001.

[4] C. T. C. Nguyen, "Vibrating RF MEMS for Low Power Wireless Applications," *Proceedings of 2000 International MEMS Workshop*, pp. 21–34, July 2001.

[5] `http://www.broadcom.com/cgi-bin/pr/prps.cgi?pr_id=PR020122A`, visited in March 2003.

[6] A. Matsuzawa, "RF-SOC–Expectations and Required Conditions," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 245–253, January 2002.

[7] A. Springer, L. Maurer, and R. Weigel, "RF System Concepts for Highly Integrated RFICs for W-CDMA Mobiile Radio Terminals," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 254–267, January 2002.

[8] M. S. J. Steyaert, B. D. Muer, P. Leroux, M. Borremans, and K. Mertens, "Low-Voltage Low-Power CMOS-RF Transceiver Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 281–287, January 2002.

[9] S. Martin, V. D. Archer-III, D. M. Boulin, M. R. Frei, K. K. Ng, and R. H. Yan, "Device Noise in Silicon RF Technologies," *Bell Labs Technical Journal*, pp. 30–45, summer 1997.

[10] K. H. Lim, C. H. Park, D. S. Kim, and B. S. Kim, "A Low-Noise Phase-Locked Loop Design by Loop Bandwidth Optimization," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 807–815, June 2000.

[11] G. Chien and P. R. Gray, "A 900-MHz Local Oscillator using a DLL-based Frequency Multiplier Technique for PCS Applications," *2000 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 1996–1999, February 2000.

[12] L. Lin, L. Tee, and P. R. Gray, "A 1.4 GHz Differential Low-Noise CMOS Frequency Synthesizer using a Wideband PLL Architecture," *2000 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 204–205, February 2000.

[13] C. H. Park and B. S. Kim, "A Low-Noise, 900-MHz VCO in 0.6-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 586–591, May 1999.

[14] J. Long, J. Y. Foo, and R. J. Weber, "A 2.4 GHz Low-Power Low-Phase-Noise CMOS LC VCO," *2004 IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design*, pp. 213–214, February 2004.

[15] L. Perraud, J.-L. Bonnot, N. Sornin, and C. Pinatel, "Fully-Integrated 10 GHz CMOS VCO for Multi-Band WLAN Applications," *2003 Sophia Antipolis Micro-Electronics forum*, pp. 1–6, October 2003.

[16] Y.-K. Chu and H.-R. Chuang, "A Fully Integrated 5.8 GHz U-NII Band 0.18-μm CMOS VCO," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 7, pp. 287–289, July 2003.

[17] J. T. Clemens, "Silicon Microelectronics Technology," *Bell Labs Technical Journal*, vol. 2, no. 4, pp. 76–102, Autumn 1997.

[18] P. McAdam and B. G. Goldberg, "Technical Future: CMOS SOS for Mixed-Signal ICs," *Applied Microwave & Wireless Magazine*, pp. 26–37, February 2002.

[19] Peregrine Semiconductor Corporation, (`http://www.peregrine-semi.com`).

[20] R. A. Johnson, C. E. Chang, P. M. Asbeck, P. R. de la Houssaye, G. A. Garcia, and I. Lagnado, "Microwave Characteristics of High Fmax Low Noise Thin Film Silicon-on-Sapphire MOSFETs," *1995 IEEE International SOI Conference*, pp. 18–19, October 1995.

[21] R. Reedy, J. Cable, D. Kelly, M. Stuber, F. Wright, and G. Wu, "UTSi CMOS: A Complete RF SOI Solution," *Analog Integrated Circuits and Signal Processing*, vol. 25, no. 2, pp. 171–179, November 2000.

[22] J. C. S. Woo, "High Performance Silicon on Sapphire Technology," *Final Report 1997-1998 for MICRO project 97-208.*

[23] V. D. T. Johan and K. Dieter, "Oscillator Design Efficiency: A New Figure of Merit for Oscillator Benchmarking," *2000 IEEE International Symposium on Circuits and Systems*, vol. II, pp. 533–536, May 2000.

[24] E. Hegazi, H. Sjoland, and A. A. Abidi, "A Filtering Technique to Lower LC Oscillator Phase Noise," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, December 2001.

[25] `http://www.vari-l.com/products/productdetail.asp?model=VCO191-2750U`, visited on 5 April 2003.

[26] H. Wang, "A 9.8 GHz Back-Gate Tuned VCO in 0.35 μm CMOS," *1999 IEEE International Solid-State Circuits Conference*, pp. 406–407, 1999.

[27] Q. Huang, "On the Exact Design of RF Oscillators," *Proceedings of the IEEE 1998 Custom Integrated Circuits Conference*, pp. 67–70, May 1998.

[28] P. Kinget and R. Frye, "A 2.4 GHz CMOS VCO with MCM-inductor," *1998 IEEE Proceedings of the 24th European Solid-State Circuits Conference*, pp. 364–367, September 1998.

[29] J. Craninckx, M. Steyaert, and H. Miyakawa, "A Fully Integrated Spiral-LC CMOS VCO Set with Prescaler for GSM and DCS-1800 Systems," *Proceedings of the IEEE 1997 Custom Integrated Circuits Conference*, pp. 403–406, May 1997.

[30] J. O. Plouchart, B. U. Klepser, H. Ainspan, and M. Soyuer, "Fully-monolithic 3 V SiGe Differential Voltage-Controlled Oscillators for 5 GHz and 17 GHz Wireless Applications," *1998 IEEE Proceedings of the 24th European Solid-State Circuits Conference*, pp. 332–335, September 1998.

[31] L. Dauphinee, M. Copeland, and P. Schvan, "A Balanced 1.5 GHz Voltage Controlled Oscillator with an Integrated LC Resonator," *1997 IEEE International Solid State Circuit Conference Digest of Technical Papers*, pp. 390–391, February 1997.

[32] A. Rofougaran, J. Rael, M. Rofougaran, and A. A. Abidi, "A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," *1996 IEEE International Solid State Circuit Conference Digest of Technical Papers*, pp. 392–393, February 1996.

[33] B. Razavi, "A 1.8 GHz CMOS Voltage-Controlled Oscillator," *1997 IEEE International Solids State Circuits Conference Digest of Technical Papers*, pp. 388–389, February 1997.

[34] T. Kwasniewski, M. A. Seido, A. Bouchet, F. Gaussorgues, and J. Zimmerman, "Inductorless Oscillator Design for Personal Communications Devices-a 1.2 μm CMOS Process Case Study," *Proceedings of the IEEE 1995 Custom Integrated Circuits Conference*, pp. 327–330, May 1995.

[35] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Phase Noise in Multi-Gigahertz CMOS Ring Oscillators," *Proceedings of the IEEE 1998 Custom Integrated Circuits Conference*, pp. 49–52, May 1998.

[36] Z. Skvor, S. R. Saunders, and C. S. Aitchison, "Novel Decade Electronically Tunable Microwave Oscillator Based on the Distributed Amplifier," *Electronics Letters*, vol. 28, no. 17, pp. 1647–1648, August 1992.

[37] L. Divina and Z. Skvor, "The Distributed Oscillator at 4 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2240–2243, December 1998.

[38] B. Kleveland, C. H. Diaz, D. Dieter, L. Madden, T. H. Lee, and S. S. Wong, "Monolithic CMOS Distributed Amplifier and Oscillator," *1999 IEEE International Solid State Circuit Conference Digest of Technical Papers*, pp. 70–71, February 1999.

[39] H. Wu and A. Hajimiri, "Silicon-Based Distributed Voltage-Controlled Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 493–501, March 2001.

[40] D. B. Leeson, "A Simple Model of Feedback Oscillator Noises Spectrum," *Proceedings of IEEE*, vol. 54, no. 2, pp. 329–330, February 1966.

[41] J. Craninckx and S. J. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 736–744, May 1997.

[42] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[43] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, and Y. H. Kwark, "Spiral Inductors and Transmission Lines in Silicon Technology using Copperdamascene Interconnects and Low-Loss Substrates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, pp. 1961–1968, October 1997.

[44] M. Danesh and J. R. Long, "Differentially Driven Symmetric Microstrip Inductors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 332–341, January 2002.

[45] J. Craninchkx and S. J. Steyaert, "Low-Noise Voltage-Controlled Oscillators using Enhanced LC-Tanks," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 794–804, December 1995.

[46] P. McAdam and B. G. Goldberg, "CMOS SOS for Mixed Signal ICs," *Peregrine Semiconductor Corporation Technical Paper*, June 2001.

[47] A. Hajimiri, "Recent Advances in RF CMOS," *RF IC Symposium*, May 2001 (`http://www.chic.caltech.edu/Publications/RFIC01_ali.pdf`).

[48] H. Wang, "A 50 GHz VCO in 0.25 μm CMOS," *2001 IEEE International Solid State Circuit Conference Digest of Technical Papers*, pp. 372–373, February 2001.

[49] W. D. Cock and M. Steyaert, "A CMOS 10 GHz Voltage Controlled LC-Oscillator with Integrated High-Q Inductor," *27th European Solid-State Circuits Conference*, pp. 496–499, September 2001.

[50] P. Andreani and S. Mattisson, "On the Use of MOS Varactors in RF VCO's," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 905–910, June 2000.

[51] T. H. Lee and A. Hajimiri, "Oscillator Phase Noise: A Tutorial," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 326–336, March 2000.

[52] D. B. Leeson, "A Simple Model of Feedback Oscillator Noises Spectrum," *Proceedings of IEEE*, vol. 54, no. 2, pp. 329–330, February 1966.

[53] A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, February 1998.

[54] J. J. Rael and A. A. Abidi, "Physical Processes of Phase Noise in Differential LC Oscillators," *IEEE 2000 Custom Integrated Circuits Conference*, pp. 569–572, May 2000.

[55] N. M. Nguyen and R. G. Meyer, "Si IC-Compatible Inductors and LC Passive Filters," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 1028–1030, August 1990.

[56] J. R. Long and M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 357–369, March 1997.

[57] G. F. Zhang and J. L. Gautier, "Broad-band, Lossless Monolithic Microwave Active Floating Inductor," *IEEE Microwave Guided Wave Letters*, vol. 3, no. 4, pp. 98–100, April 1993.

[58] M. McCorquodale, A. C. Wong, K. Nagarajan, H. Kulah, and C. T.-C. Nguyen, "An Integrated MEMS-BiCMOS SINCGARS Transceiver," *Design Automation Conference 2000*, June 2000 (`http://www.eecs.umich.edu/~mmccorq/research/mccorquodaleDAC00.pd%f`).

[59] M. W. Geen, G. J. Green, R. G. Arnold, J. A. Jenkins, and R. H. Jansen, "Miniature Mulilayer Spiral Inductors for GaAs MMICs," *Proceedings of GaAs IC Symposium Digests*, pp. 303–306, October 1989.

[60] W. B. Kuhn, A. E. Riad, and F. W. Stephenson, "Centre-Tapped Spiral Inductors for Monolithic Bandpass Filters," *Electronics Letters*, vol. 31, no. 8, pp. 625–626, April 1995.

[61] R. A. Johnson, C. E. Chang, P. M. Asbeck, M. E. Wood, G. A. Garcia, and I. Lagnado, "Comparison of Microwave Inductors Fabricated on Silicon-on-Sapphire and Bulk Silicon," *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 9, pp. 323–325, September 1996.

[62] R. A. Johnson, P. R. de la Houssaye, C. E. Chang, P. F. Chen, M. E. Wood, G. A. Garcia, I. Lagnado, and P. M. Asbeck, "Advanced Thin-Film Silicon-on-Sapphire Technology: Microwave Circuit Applications," *IEEE Electron Device Letters*, vol. 45, no. 5, pp. 1047–1054, May 1998.

[63] "Silicon On Sapphire (SOS) 0.5 μm CMOS DLP/TLM from Peregrine Semiconductor," *Presentation Material*, January 2001 (`http://cmp.imag.fr/Forms/Slides2003/05_SOS.pdf`).

[64] M. P. Wilson, "Modelling of Integrated VCO Resonators Using Momentum," *technical paper*, Tality, UK.

[65] `http://formosa.eecs.berkeley.edu/~niknejad/asitic.html`, visited on 21 November 2002.

[66] E. Pettenpaul, H. Kapusta, A. Weisgerber, H. Mampe, J. Luginsland, and I. Wolff, "CAD Models of Lumped Elements on GaAs up to 18 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 2, pp. 294–304, February 1988.

[67] H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. 10, no. 2, pp. 101–109, June 1974.

[68] G. Lihui, Y. Mingbin, C. Zhen, H. Han, and Z. Yi, "High Q Multilayer Spiral Inductor on Silicon Chip for 5 $\sim$ 6 GHz," *IEEE Electron Device Letters*, vol. 23, no. 8, pp. 470–472, August 2002.

[69] D. Eggert, P. Huebler, A. Huerrich, H. Kueck, W. Budde, and M. Vorwerk, "A SOI-RF-CMOS Technology on High Resistivity SIMOX Substrates for Microwave Applications to 5 GHz," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 1981–1989, November 1997.

[70] B. Piernas, K. Nishikawa, K. Kamogawa, T. Nakagawa, and K. Araki, "High-Q Factor Three-Dimensional Inductors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 8, pp. 1942–1949, August 2002.

[71] K. S. Kundert, "Modeling Varactors," *The Designer's Guide*, June 2002.

[72] Skyworks Solutions, Inc., "Varactor SPICE Models for RF VCO Applications," *Application note (APN1004)*.

[73] P. Andreani and S. Mattisson, "A 2.4-GHz CMOS Monolithic VCO Based on an MOS Varactor," *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, vol. II, pp. 557–560, May/June 1999.

[74] A. Kral, F. Behbahani, and A. A. Abidi, "RF CMOS Oscillators with Switched Tuning," *Proceedings of the Custom IC Conference*, pp. 555–558, May 1998.

[75] B. G. Streetman and S. Banerjee, *Solid State Electronic Devices - Chapter 6.* Prentice Hall, 2000.

[76] H. Ainspan and J. O. Plouchart, "A Comparison of MOS Varactors in Fully-Integrated CMOS LC VCO's at 5 and 7 GHz," *26th European Solid-State Circuits Conference*, pp. 448–451, September 2000.

[77] Peregrine Semiconductor Corp., p. 7, Peregrine UTSi 0.5 μm Design Manual.

[78] Peregrine Semiconductor Inc., p. 2, FC Rev. 1.3 UTSi 0.5 μm RF SPICE Models.

[79] J. P. Colinge, "Fully-Depleted SOI CMOS for Analog Applications," *IEEE Transactions on Electron Devices*, vol. 45, no. 5, pp. 1010–1016, May 1998.

[80] Peregrine Semiconductor Inc., pp. 31–32, FC Rev. 2.1 UTSi 0.5 μm DIGITAL SPICE Models.

[81] B. W. Offord and J. S. Ruthberg, "Radiation-Hardened Silicon-on-Insulator 0.8-μm Technology Design Rules," *TECHNICAL DOCUMENT 3065*, May 1999.

[82] B. D. Muer, M. Borrmans, M. Steyaert, and G. L. Puma, "A 2-GHz Low-phase-noise Integrated LC-VCO Set with Flicker Noise Upconversion Minimization," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1034–1038, July 2000.

[83] S. Levantino, C. Samori, A. Bonfanti, S. L. J. Gierkink, A. L. Lacaita, and V. Boccuzzi, "Frequency Dependence on Bias Current in 5-GHz CMOS VCOs: Impact on Tuning Range and Flicker Noise Upconversion," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1003–1011, August 2002.

[84] R. Aparicio and A. Hajimiri, "A Noise-Shifting Differential Colpitts VCO," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, December 2002.

[85] M. Tiebout, "Low-Power Low-Phase-Noise Differentially Tuned Quadrature VCO Design in Standard CMOS," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1018–1024, July 2001.

[86] M. R. A. Rofougaran, J. Rael and A. Abidi, "A 900 MHz CMOS LC Oscillator with Quadrature Outputs," *1996 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 392–393, February 1996.

[87] Agilent Technologies, Inc., (`http://eesof.tm.agilent.com`).

[88] Cadence Design Systems, Inc., (`http://www.cadence.com`).

[89] Microsoft Corporation, (`http://www.microsoft.com`).

[90] Vari-L Company, Inc., (`http://www.vari-l.com`).

[91] K. Kurokawa, "Injection Locking of Microwave Solid-State Oscillators," *Proceedings of the IEEE*, vol. 61, no. 10, pp. 1386–1410, October 1973.

[92] H. R. Rategh and T. H. Lee, "Superharmonic Injection-Locked Frequency Dividers," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, June 1999.

[93] J. B. Yoon and C. T. C. Nguyen, "A High-Q Tunable Micromechanical Capacitor with Movable Dielectric for RF Applications," *2000 IEEE International Electron Devices Meeting Technical Digest*, pp. 489–492, December 2000.

[94] C. T. C. Nguyen and R. T. Howe, "An Integrated CMOS Micromechanical Resonator High-Q Oscillator," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 4, pp. 440–445, April 1999.