Analysis, Modelling, Design, and Control of DC-DC Converter for Renewable Power Generation Systems

by

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Dedication: This work is dedicated to my loving parents and elder brother for their love, encouragement and endless support.

Abstract

Global energy demand is rapidly growing and therefore meeting the future energy demand is becoming a major concern worldwide. To meet the energy demand, fossil fuels are still used as the primary energy source. However, these hydrocarbon-based fuels produce greenhouse gases that adversely affect environment and human health. Therefore, alternative renewable energy sources such as solar, wind, hydro, biomass and geothermal are getting very popular. Currently, development of power converters for these renewable energy sources is becoming more and more essential for converting this energy to appropriate voltage levels or feeding it to electrical power distribution networks. This research study is focused on the DC-DC boost converter analysis, design, modelling, and using current control techniques for single-phase uninterruptible power supply (UPS) inverter systems.

The major contributions of the presented work can be categorized into two parts: Firstly, a comprehensive analysis of classical and advanced DC-DC converter topologies for renewable power applications. DC-DC power converters have attracted significant attention due to their increased use in a number of applications from aerospace to biomedical devices. The interest in wide bandgap (WBG) power semiconductor devices stems from outstanding features of WBG materials and power device operation at higher temperatures, larger breakdown voltages and sustaining larger switching transients than silicon (Si) devices. As a result, recent progress and development of WBG power devices based converter topologies are well-established for power conversion applications in which classical Si based power devices show limited performance. Currently, WBG devices such as silicon carbide (SiC) and gallium nitride (GaN) are the most promising semiconductor materials that are being considered for new generation of power devices because of their high voltage operation, high current switching capabilities, very low ON resistance, good thermal conductivity, etc.

Secondly, a cost effective design of Gallium nitride (GaN)-based high-frequency, high efficiency DC-DC boost converter owing to preferred soft-switching features. The

use of new power semiconductor devices such as GaN high electron mobility transistors (GaN HEMTs) are able to minimize switching losses, allowing high switching frequencies (from kHz to MHz) for realizing compact and fully integrated power converters.

Finally, PI and PR control parameters are optimally tuned, and experimentally tested for single-phase UPS inverters to obtain very low total harmonic distortion (THD), zero steady-state error, and fast response. This research presents detailed analysis and mathematical models of PI and PR controllers in single-phase UPS inverter applications. In order to realize the importance of PR control features over conventional PI controllers, a PI controller is implemented in the same UPS inverter and mathematically analyzed. The performance of these controllers is analyzed in terms of steady-state is and transient responses and current harmonics level. The experimental result shows that the PR controller achieves zero steady-state error, improved transient response and reduced low-order harmonics distortion of the output current compared to PI controller. The performances of the implemented controllers are simulated and compared using the MATLAB/Simulink modeling environment.

The main significance of this work is the design and development of a DC-DC boost converter, and optimization of controller parameters for high power application such as Electric Vehicle (EV) charging, aerospace, renewable power generation, etc.

Statement of Originality

I certify that this work contains no material which has been accepted for the award of any other degree or diploma in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text. In addition, I certify that no part of this work will, in the future, be used in a submission in my name, for any other degree or diploma in any university or other tertiary institution without the prior approval of the University of Adelaide and where applicable, any partner institution responsible for the joint-award of this degree. I give consent to this copy of the thesis, when deposited in the University Library, being available for loan, and photocopying, subject to the provisions of the Copyright Act 1968. I also give permission for the digital version of my thesis to be made available on the web, via the University's digital research repository, the Library Search and also through web search engines, unless permission has been granted by the University to restrict access for a period of time. I acknowledge the support I have received for my research through the provision of an Australian Government Research Training Program (RTP) Scholarship.

	07/06/2022
Signed	Date

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Thesis Conventions

The following conventions have been adopted in this Thesis:

1. **Spelling.** Australian English spelling conventions have been used, as defined in the Macquarie English Dictionary, A. Delbridge (Ed.), Macquarie Library, North Ryde, NSW, Australia, 2001.

2. **Typesetting.** This document was compiled using the MikTex 2.9 software. TeXnicCentre was used as text editor interfaced to MikTex. XCircuit and GSview 5.0 were used to produce circuit diagrams and other drawings.

3. **Mathematics.** MATLAB/Simulink tools (MATLAB Version R2018a) were used to simulate the proposed converter and control technique. MATLAB code was written to generate the Bode diagrams.

4. **TMS320F28335 eZdsp™.** For hardware implementation of both controllers' algorithms, a 32-bit floating-point TMS320F28335 eZdsp development board was used. The C program for both controllers was developed by using Texas Instrument Code Composer Studio 6.1.0 (CCS) software.

5. **Referencing.** The Harvard style has been used for referencing.

Publications

1. **M. Parvez,** A. T. Pereira, N. Ertugrul, N. H. E. Weste, D. Abbott, and S. F. Al-Sarawi. Wide bandgap power DC-DC converter topologies for power applications. In *Proceedings of the IEEE*, Published – 29 April 2021, *ISI-Indexed*, Q1, Impact factor: 10.694. DOI: 10.1109/JPROC.2021.3072170

2. **M. Parvez,** M. F. M. Elias, N.A. Rahim, F. Blaabjerg, D. Abbott, and S. F. Al-Sarawi. Comparative study of discrete PI and PR control for single-phase UPS Inverter. In *IEEE Access*, Published – 07 January 2020, *ISI-Indexed*, Q1, Impact factor: 4.098. DOI: 10.1109/ACCESS.2020.2964603

3. **M. Parvez,** A. T. Pereira, N. H. E. Weste, D. Abbott, and S. F. Al-Sarawi. GaN-based high-frequency high-voltage gain non-isolated transformerless DC-DC boost converter with voltage-lift switched-inductor circuit. In *IEEE Access*, Submitted.

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List of Abbreviations

2DEG	two dimensional electron gas
AC	alternating current
ADC	analog-to-digital converter
AlGaN/GaN	aluminium mole fraction in AlGaN layers of GaN-capped
APFs	active power filters
BB	buck-boost
CC	capacitor clamp
CCM	continuous current mode
CCS	Code Composer Studio 6.0
CHB	cascade H-bridge
CMOS	complementary metal oxide semiconductor
CRM	critical current mode
CW	Cockcroft-Walton
D-Mode	depletion mode
DC	direct current
DiC	diode-clamped
DSP	digital signal processor
E-mode	Enhancement-mode
ESR	equivalent series resistance
EVs	electrical vehicles
F-C	flying-capacitor
FB	full-bridge

FC	fuel cell
FFT	fast fourier transform
GaAs	gallium arsenide
GaN	gallium nitride
GTOs	gate turn-off thyristors
HB	half-bridge
HEMTs	high electron mobility transistors
HEV	hybrid electric vehicle
HF	high frequency
HP	high-power
HV	high-voltage
HVDC	high-voltage direct current
IGBTs	insulated-gate bipolar transistors
IMP	internal model principle
JBS	Junction Barrier Schottky
kV	kilovolts
kW	kilowatt
L-C	inductor-capacitor
LV	low voltage
MC	multilevel converter
MF	medium frequency
MHz	megahertz
MMC	modular multilevel converter
MOSFETs	metal oxide semiconductor field effect transistors
MP	medium power

MVDC	medium-voltage direct current
NPC	neutral point clamping
PCB	printed circuit board
PDDC	power DC-DC converter
PI	proportional integral
PR	proportional resonant
PV	photovoltaic
PWM	pulse width modulation
RC	repetitive control
SEPICs	single-ended primary-inductor converters
Si	silicon
SiC	silicon carbide
SM	sliding mode
SS	soft switching
SS-PWM	soft switchinh pulse width modulated
THD	total harmonic distortion
THDi	current total harmonic distortion
TSBB	two-switch buck-boost
UPS	uninterruptible power supply
VHF	very high frequency
WBG	wide band gap
ZCS	zero current switching
ZVS	zero voltage switching

List of Symbols

δV_{C_i}	denotes voltage ripple of i_{th} capacitor.
δ_i	denotes current ripple.
δ_v	denotes voltage ripple.
η	eta denotes converter efficiency.
μF	the microfarad.
μH	microhenry.
μm	micrometre.
μs	microsecond.
Ω	ohm.
$\Omega{\cdot}\text{cm}^2$	ohm square centimetre.
ω_c	the cut-off frequency.
ω_o	the resonance frequency.
π	pi.
nC	nanocoulomb.
nF	the nanofarad.
$\{i = 1, 2, 3, \cdots, N\}$	N-stage cascade CW voltage multiplier.
°C	degree celsius.
e	error signal.
eV	electron volt.
$e(n)$	controller error.
K_i	the integral gain constant.
K_p	the proportional gain constant.
s	the Laplace variable.
T	sampling time.
$u(n)$	controller output.

Chapter 1

Introduction

This chapter introduces the area of converters, current controllers, and the motivations to carry out the research described in this thesis. The main aims and contributions of the thesis are outlined, and the contents of each chapter are briefly described.

1.1 Converters and Current Controllers

The most significant task in power converter design is to decrease power losses to improve the conversion efficiency—this impacts on a wide range of applications, more specifically when these converters are used renewable energy. By decreasing the power loss, the size of the converter components can be reduced, which leads to a compact size for the whole converter (Ertugrul & Abbott 2020, Bertoni et al. 2016).

Therefore, the converter size and cost fully depends on the design requirements and applications, where power density of the converter is inversely proportional to the size of converter passive components. Due to increased switching frequency result in increasing both the power density and switching loss increase, leading to decreasing the converter's efficiency. Moreover, these switching losses can be reduced by using several soft switching techniques, which further increase the complexity of the converter design and circuitry.

In the last decade, crucial research has been focused on isolated DC-DC converters to improve their conversion efficiency and voltage gain, as well as reducing the switching losses (Ertugrul & Abbott 2020, Pareschi et al. 2014, Tan et al. 2012, 2013, Yu et al. 2013, Saha et al. 2020). The majority of power converters can be unidirectional to deliver power to loads such as, motor drives, uninterruptable power supplies, and

battery chargers. Recently, due to the increased demand for battery storage applications, bidirectional converters are attracting more interest. Historically, silicon (Si) MOSFET technology is well established in power semiconductor devices (Kahng 1976). Recently, wide band gap (WBG) semiconductor materials have been introduced in the power semiconductor market. Among the various WBG devices, silicon carbide (SiC) and gallium nitride (GaN) devices deliver superior power converter performance due to their outstanding material properties in comparison to with silicon based devices (Kaminski & Hilt 2014, Millan et al. 2014, Ramachandran & Nymand 2015). Extensive studies of SiC power devices have demonstrated their effectiveness in the recent literature (Boutros et al. 2009, Inoue & Akagi 2007). On the other hand, there are only a few studies on GaN devices for high power converters (up to few kW) (Das et al. 2011, Huang et al. 2016).

A basic classification of power conversion systems can be performed based on either their input and output signals, direct current (DC) or alternating current (AC), as follows:

- DC-DC Converter.
- DC-AC Inverter.
- AC-DC Rectifier.
- AC-AC Transformer.

This research work is focused on the DC-DC boost converter analysis, design, and development with the optimisation of filter and current controller parameters for single-phase uninterruptible power supply (UPS) inverter systems. The current controllers are divided into several control techniques. There are a number of control techniques that can be used in DC-DC converters, two of the most common techniques are proportional integral (PI) and proportional resonant (PR). In general, PI controller has been employed in many power converters applications, such as active power filters (APFs), wind turbines, water turbines, photovoltaic inverters, uninterruptable power supplies, dynamic voltage restorer, active rectifiers, boost converters, induction drives, fuel-cell inverters and micro grids (Rocabert et al. 2012, Hasan et al. 2008, Mahmud et al. 2017).

Recently, PR controller is gaining popularity because of its capability in tracking a sinusoidal reference with zero steady-state error especially for single-phase system (Rocabert et al. 2012, Parvez et al. 2020). It can also be applied in three-phase standalone and grid-connected micro inverter system.

1.2 Research Motivation

Recently, a lot of research has been focused on converters due to growing interest in power electronics, and renewable power generation. Their broad range of applications in renewable power generation such as- fuel cell (FC), photovoltaic (PV), wind turbine, biomass, tidal, and industrial electronics, electrical vehicles (EVs), battery-operating portable equipment, uninterruptible power supply (UPS), and telecommunication systems and many more. This research specially focuses on high-frequency, high-voltage gain converter topology for renewable power application, and associated control techniques. In this way, two control techniques are modelled, designed and implemented for UPS inverter application. This thesis is focused on: (i) wide bandgap DC-DC converter topology analysis, (ii) high frequency, high-efficiency novel DC-DC boost converter design for power applications, and current control techniques for single-phase UPS inverter application.

1.3 Project Aims and Significance

The main objective for this research project is to design and develop a DC-DC boost converter and associated controller parameters. The objectives of this study are as follow:

1. Design and development of a high-frequency, high efficiency GaN-based full-bridge DC-DC boost converter with a voltage-lift switched-inductor circuit, which provides high voltage-gain and high efficiency without operating at high duty cycle.
2. Development of a mathematical model for proposed converter.
3. Development of mathematical model of PI and PR current controller.

4. Optimisation of the PI and PR controller parameters for single-phase UPS inverter.

5. Design, development, implementation and verification of an inverter prototype using PI and PR controllers.

1.4 Thesis Outline

Chapter 1– presents the area of converters, current controllers, research motivation, project aims, and thesis outline.

Chapter 2 – provides a historical overview of classical and recent progress development in wide band gap power DC-DC converter topologies for power applications and major challenges in material, design, architecture, devices are described. This leads into the high efficiency, high voltage gain converter design for renewable power generation systems. Finally, design recommendation and future trends are explored.

Chapter 3 – presents the operating principle of the proposed high step-up DC-DC converters. Also associated circuit diagram for the different operation stage each of the converter and their ideal key waveforms are presented and discussed. Using the developed steady-state mathematical analysis, design and selection procedure of different passive and active parameters used in the developed converter topologies are also discussed. In addition, the analysis of voltage and current stresses on different devices, voltage gain, voltage and current ripple are presented.

Chapter 4 – optimisation technique for both the PI and PR controller parameters included in the UPS inverter are presented and discussed. This chapter discussed the open-loop, and closed-loop responses of both PI and PR controller using selected and optimisated parameters values used to conduct the simulation and experimental varification. In addition, the simulation and test results for both controllers are also described in this chapter.

Chapter 5 – provides a summary of the presented work and provides concluding remarks, summary of contributions and future research directions.

1.5 Thesis Contributions

With a focus on the development of high-frequency, high-voltage gain DC-DC step-up converter, and optimisation of current controller parameters for renewable power generation systems. The main contributions of this research are outline as follows:

1. The design and development of a high-frequency, high-efficiency full-bridge GaN-based transformerless DC-DC step-up converter. The proposed design provides high voltage-gain using only two cascaded voltage multiplier stages and operate at lower duty cycle with variable input voltage.

2. Design, development and implementation of a PWM control strategy of inverter using two independent switching frequencies along with variable duty cycle.

3. Mathematical modeling of PI and PR controllers and comparative performance analysis of proposed PI and PR controller.

4. Optimally tuned controller parameters to achieve very low THD.

Chapter 2

Wide Bandgap DC-DC Converter for Power Applications

This chapter is organized into five sections. Section 2.2 presents and describes classical power DC-DC converter topologies. Then, in Section 2.3, recent progress and development in wide band gap power devices and major challenges are described. In Section 2.4, WBG-based power DC-DC power converters topologies are presented. Design recommendations, followed by future research trends are discussed in Section 2.5. This is then followed by a summary.

Most of this chapter contents have been published in Proceedings of the IEEE.

1. **M. Parvez,** A. T. Pereira, N. Ertugrul, N. H. E. Weste, D. Abbott, and S. F. Al-Sarawi. Wide bandgap power DC-DC converter topologies for power applications. In *Proceedings of the IEEE*, Published – 29 April 2021, *ISI-Indexed*, Q1, Impact factor: 10.694. DOI: 10.1109/JPROC.2021.3072170

2.1 Introduction

Today's silicon power MOSFET and silicon insulated gate bipolar transistor (IGBT) are the main building blocks of power electronics switching circuits (Shenai 2019). Advanced silicon IGBTs with blocking voltage capability ranging from 600 to 6,500 V are emerging due to the large variety of high volume applications (Baliga 2015). In the last 5 years, SiC devices have become commercially available with potential to replace silicon IGBTs in a number of applications. However, penetration into the

IGBT market is still constrained by the high manufacturing cost of SiC devices. The on-state characteristic curve of IGBT devices is shown in Figure 2.1 as a function of the blocking voltage rating. It can be seen from the figure that, the reduction in the on-state current density for IGBTs results in an increase in blocking voltage. The on-state current density is determined by thermal consideration such as maximum junction temperature of the package (Rahimo 2014). However, silicon power semiconductor devices suffer from several issues (Briere 2010):

- High losses: The relatively low silicon bandgap (1.1 eV) and low critical electric field (30 V/μm) result in high voltage devices with substantial thickness; leading to higher conduction losses.
- Low switching frequency: Silicon power MOSFETs incur high conduction losses due to majority carriers and hard switching operation. The gate charge capacitance produces high spike current, which leads to increased conduction losses and switching losses at high switching frequencies. On the other hand, Si IGBTs have higher current density compared to Si MOSFETs due to minority carriers and conductivity modulation. The minority carriers reduce the switching frequency range of IGBTs, resulting in low switching losses. Low switching frequency also leads to larger inductors and capacitors, resulting in bulkier systems.
- High leakage current & high-temperature: Typically, the junction temperature and leakage current depends on the high intrinsic carrier density, resulting in the high intrinsic carrier density of silicon power devices leading to an increase in junction temperature and leakage current. The maximum operating junction temperature of IGBTs is typically 125°C.

In the recent development of power semiconductor devices, several researchers have tried to alleviate these problems by using WBG semiconductors. These WBG devices are capable of low-loss operation at high voltages (>1 kV to tens of kV), can operate at high frequencies (tens of kHz to tens of GHz), and high temperatures (>150°C) (Shinohara et al. 2018, Mishra et al. 2008). Power converters based on WBG devices can achieve higher efficiency, higher the term gravimetric is used for energy storage devices like batteries, and volumetric power conversion densities (Hughes et al.

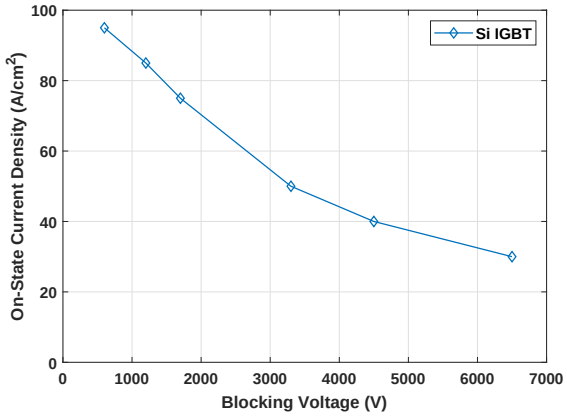


Figure 2.1: ON-state characteristics curve of IGBT devices (Baliga 2015).

2012) in comparison to complementary metal oxide semiconductor (CMOS) based devices. Hence, GaN on Si delivers superior performance to bulk Si technologies, while being more cost effective than GaN on SiC, GaN on GaN or GaN on diamond (Pittini et al. 2014).

Typically, DC–DC converters are classified into isolated and non-isolated converters as shown in Figure 2.2. The isolation mention that the electrical barrier in between the inputs and outputs of the converter. A high-frequency transformer can be used as an electrical barrier in the converter. The benefits of the barrier are in facilitating high voltage applications with different output voltage polarity (Raghavendra et al. 2020). Several converter topologies and applications are proposed to increase the efficiency of isolated DC-DC converters (Tan et al. 2013, Yu et al. 2013, Pittini et al. 2014). Most isolated DC-DC converters utilize zero voltage switching (ZVS) to improve the efficiency up to 97% for high power converters ranging from 1 to 5 kW (Nymand & Andersen 2010, Xue et al. 2015). However, it is quite challenging to further improve the efficiency of non-isolated converters.

In contrast to Si technology, GaN is a promising semiconductor for high power converters to further improve switching losses resulting in increased efficiency (Kaminski & Hilt 2014). There are still some limitations in the manufacturability of GaN devices, and the cost of GaN device is higher than Si. Recently, manufacturers have been continually addressing these limitations, reducing GaN development cost aiming for GaN devices with cost equivalence to Si (Kaminski & Hilt 2014). Another limitation in WBG devices is the packaging due to the parasitic inductances in device

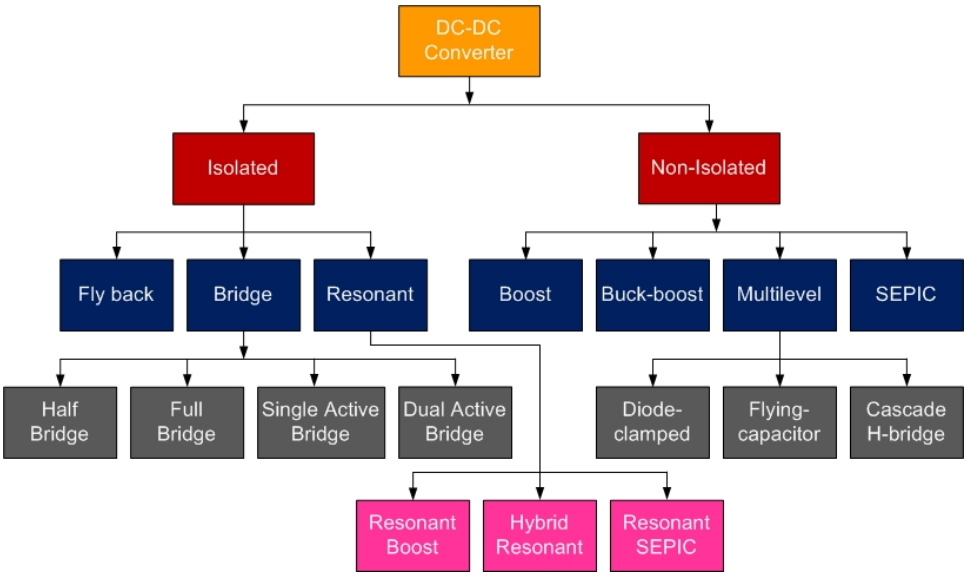


Figure 2.2: Classification of DC–DC converters.

and printed circuit board (PCB) traces (Jones et al. 2016). These devices are more popular due to low switching loss and frequency operation, but with high junction temperature (Kaminski & Hilt 2014). To enable miniaturisation and full utilisation of the GaN devices, high frequency operation is needed, so parasitic associated with on-chip interconnect and load ought to be as small as possible. For the load, such reduction can be achieved either using point-of-load (PoL) approach or utilizing an integrated voltage-regulator (IVR) (Aklimi et al. 2017, Li et al. 2010).

This chapter is organized into five sections. Section 2.2 presents and describes classical power DC-DC converter topologies. Then, in Section 2.3, recent progress and development in wide band gap (WBG) power devices and major challenges are described. In Section 2.4, WBG-based power DC-DC power converters topologies are presented. Design recommendations, followed by future research trends are discussed in Section 2.5. This is then followed by a summary.

2.2 Classical Power DC-DC Converter Topologies

To understand recent development and implementation of WBG power DC-DC converter topologies, it is important to first provide a brief summary of classical power DC-DC converters and their applications in the last decade. In the 1970s, thyristor based high-power (HP) DC-DC buck-boost converters were established for high

power applications (Morman et al. 1972). A few years later, a three level high power DC-DC converter was proposed (Nakaoka et al. 1979), which is currently known as a multilevel converter (MC) topology. This type of converter was controlled by using a time-sharing high frequency thyristor to provide large scale DC power supplies, which can operate over an ultrasonic chopping frequency region in the extent of 20 kHz or more than 20 kHz.

At the beginning of 1990s, a (HP) dual bridge DC-DC MC was established for HP applications (De Doncker et al. 1991). This topology involves a high frequency (HF) and soft switching (SS) technique with a three-phase symmetric AC link transformer. Generally, these converter topologies (such as resonant converters, multilevel converters and bridge/multi-phase bridge converters) may be considered as classical power DC-DC converter (PDDC) topologies and are used in various power applications. Different types of classical converters are used in a MC topologies for HP or medium power (MP) applications only.

2.2.1 Classical silicon (Si) based power devices

Silicon (Si) based power devices can be classified into buck converters, HF resonant boost converters, HF resonant converters and resonant single-ended primary-inductor converters (SEPICs). Several traditional circuit configurations are described based on the MOSFET/IGBT in this section. Although, both IGBT and MOSFET are voltage-controlled semiconductor devices that operate well in switch mode power supply (SMPS) applications, IGBTs possess improved power handling capability (März et al. 2018). IGBT has a lower forward voltage drop compare to MOSFET. With the increase of selections between the two devices, it's becoming more problematic to select the best device based on their applications alone. Typically, MOSFET operates at higher switching frequency around 200 kHz, where IGBT operates at low switching frequency around 10-20 kHz. The two-switch buck-boost (TSBB) converter shown in Figure 2.3 (Hossain et al. 2018), can be galvanically isolated by introducing an HF or medium frequency (MF) transformer, either in the buck cell or boost cell.

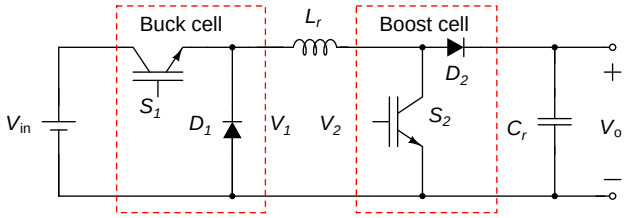


Figure 2.3: Two-switch buck-boost (TSBB) converter. The TSBB converter can be galvanically isolated by introducing an high frequency (HF) or medium-frequency (MF) transformer, either in the buck cell or boost cell, leading to the buck-derived isolated modules, as forward, push-pull, half-bridge (HB) and full-bridge (FB) modules, or boost-derived isolated modules, i.e., push-pull, HB and FB modules respectively.

A well-known classical high frequency isolated buck DC-DC converter can be obtained as shown in Figure 2.4 (a)-(b) by substituting the buck cell in Figure 2.3. Similarly, the isolated boost converter can be constructed as shown in Figure 2.4 (c)-(d) by substituting the boost cell in Figure 2.3. Moreover, a resonant tank circuit can be described to the boost converter, buck-boost converter, SEPIC converter or hybrid bridge converter to obtain SS resonance. The voltage across the switching elements may be made by putting one or more components of the inductor-capacitor (L-C) network in series or parallel with the converter switches so they can turn on-off with ZVS (Mendonça et al. 2018, Kirubakaran et al. 2009, Safaee et al. 2016). In addition to the zero switching voltage and current of the active switches, this topology also has a zero switching current for the output diodes.

Nevertheless, normally the switching frequency has to be higher than the preferred resonant frequency in order to guarantee SS operation and to obtain output voltage or current over a wide range. This tends to result in a bulky resonant tank, low power density, and poor efficiency. An example of a various types of resonant converter topologies are shown in Figure 2.5 (a)-(c). Traditionally DC-DC resonant converters are built for low frequency and low power applications, such as in telecommunications, fuel cell based power systems, renewable power supplies, etc. These topologies are limited by the use of semiconductor device switches. To overcome these problems, recently several type of HF or very high frequency (VHF) resonant converters

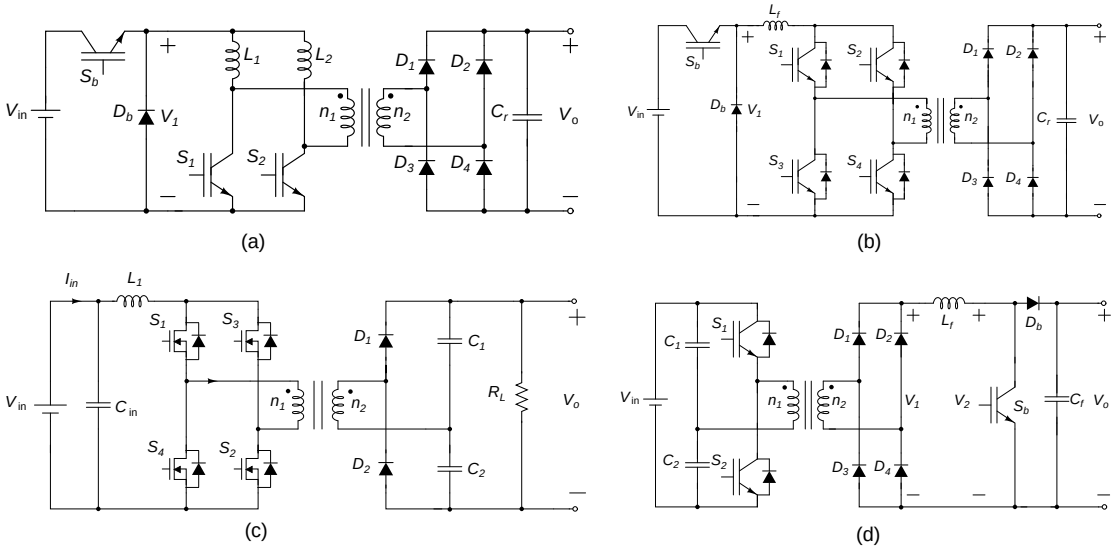


Figure 2.4: Classical high frequency isolated buck-boost (BB) DC-DC converter (Hossain et al. 2018, Yao et al. 2011) by substituting the buck cell in Figure 2.3 with (a) HB buck DC-DC converter, (b) FB buck DC-DC converter, (c) FB-boost DC-DC converter, and (d) HB-boost DC-DC converter.

were built for medium output power applications (Yu et al. 2013, Mendonça et al. 2018, Kirubakaran et al. 2009, Safaee et al. 2016).

However, bridge DC-DC power converters have been significantly developed and implemented in recent years (Zhu 2006, Zhang et al. 2013, Kim, Ehsani & Kim 2015, Pahlevani et al. 2016, Hossain et al. 2019). Figure 2.6 (a)-(d) shows existing implementation of isolated full-bridge (FB) converter topologies for HP applications. Due to SS techniques such as ZVS or zero current switching (ZCS) techniques, a possible decrease in system switching losses and an improvement in switching frequency is possible. In the same way a soft switching pulse width modulated (SS-PWM) FB bidirectional isolated converter is used for step-up function as shown in Figure 2.6 (a), where its communication process is developed to reduce mismatch between the leakage inductor and boost inductor current when communication occurs.

In (Zhang et al. 2013), the dual-input based DC-DC converter is reported where it consists of a HB-boost cell and FB boost cell combination as shown in Figure 2.6 (b). Though, this strategy has some benefits, the major limitation is the

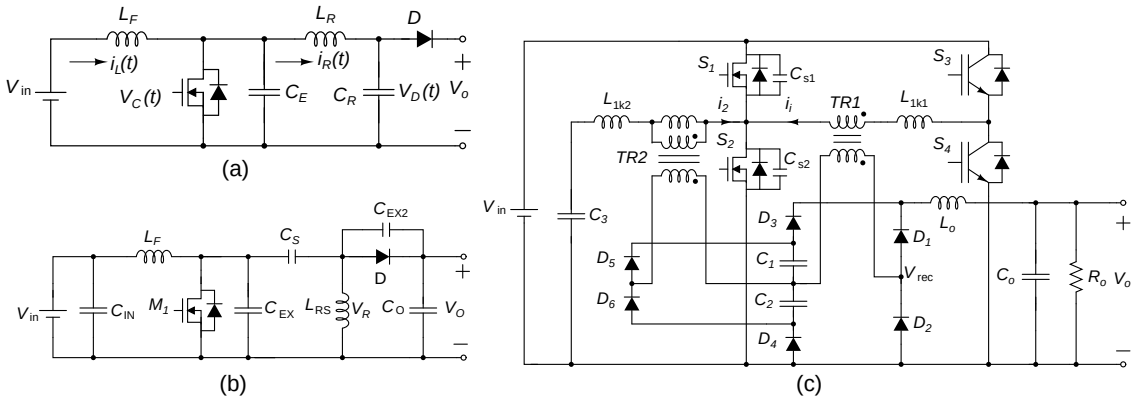


Figure 2.5: Several types of resonant converter topologies: (a) Resonant boost converter topology that is suitable for operation at very high frequencies (Burkhart et al. 2013); (b) Hybrid resonant and phase-shift converter (Yu et al. 2013), and (c) Resonant SEPIC converter and control method suitable for HF and VHF DC-DC power conversion. The topology provides high efficiency over a wide input and output voltage range (Hu et al. 2012).

current stress of converter active and passive components that raises the design complexity. In addition, due to the dead-time effect, where a capacitor charging based high-voltage (HV) DC-DC converter is implemented for power application as shown in Figure 2.6 (c) (Kim, Ehsani & Kim 2015), where it contains a FB converter and three HV-HF transformers. A series-parallel current-driven (SPCD) based FB converter as represented in Figure 2.6 (d) (Pahlevani et al. 2015), while the branch combinations of L_s, L_p, and C_p are used to offer ZVS, resulting in an improvement in the converter efficiency (Tsang et al. 2014).

2.2.2 Multilevel converter

In the last three decades, multilevel converters (MCs) are being designed and developed for medium power (MP) to HP applications (Rodríguez et al. 2007, Franquelo et al. 2008, Rodriguez et al. 2009, Kouro et al. 2010, Debnath et al. 2015). The classical and recent advances MCs can be divided into three groups such as capacitor clamped (CC) converter or diode-clamped (DiC) converter, cascade H-bridge (CHB) converter and flying-capacitor (F-C) converter (Zhang, Peng & Qian 2004, Dey & Bhattacharya 2020, Barbosa et al. 2005). In this section, modular multilevel converter (MMC) are also discussed. The basic idea of MCs is to operate at higher operating voltage and reduce the voltage stress across diodes and switches. Note

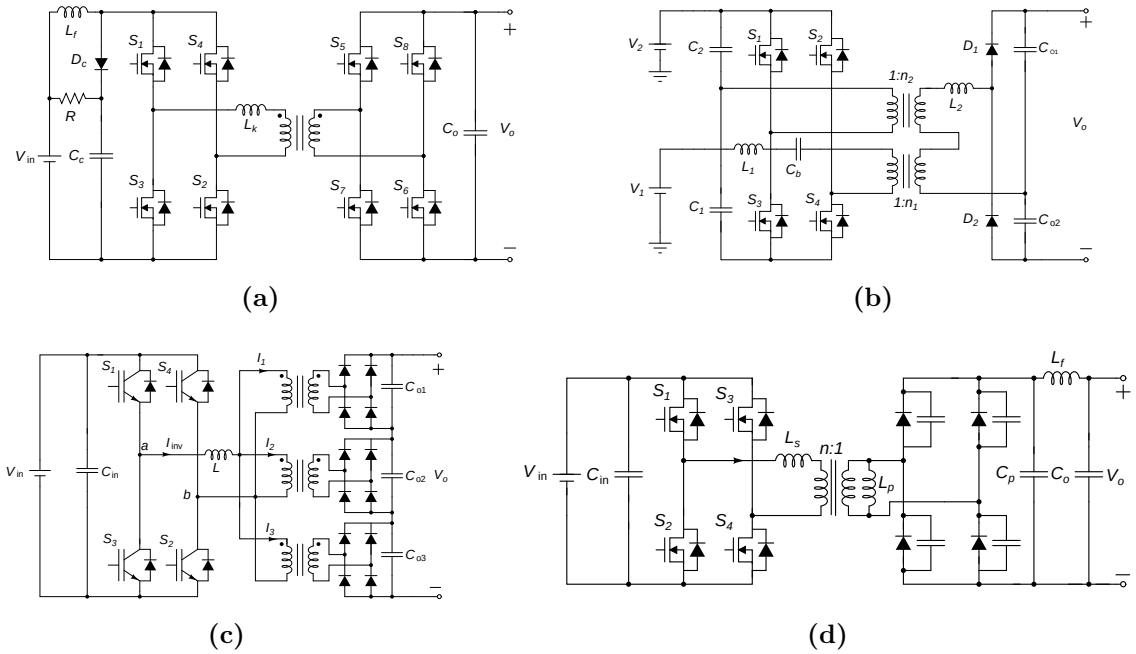


Figure 2.6: Bridge DC-DC power converter topologies: (a) Soft switching pulse width modulated (SS-PWM) bidirectional isolated FB-boost converter is used for step-up function (Hossain et al. 2018, Zhu 2006); (b) Dual-input based DC-DC converter with HB boost cell and FB boost cell combination (Hossain et al. 2018, Zhang et al. 2013); (c) HV DC-DC FB converter is implemented for pulse-power application (Hossain et al. 2018, Kim, Ehsani & Kim 2015); and (d) SPCD converter topology (Hossain et al. 2018, Pahlevani et al. 2015).

that DC-DC MCs with an transitional AC link is based on the well-known DC-AC MC.

Recently the three-level (3L) DC-DC converter topologies with an LLC resonant circuit have been proposed in HP and MP applications as shown in Figure 2.7 (Coccia et al. 2007), where the neutral point clamping (NPC) structure is used by neglecting neutral point clamping diodes (Coccia et al. 2007). The LLC resonant circuit is presented to obtain SS operation, which provides a stable DC output voltage (Rosas-Caro et al. 2015).

A three-phase three-level DC-DC converter topology is shown in Figure 2.8. This converter topology commonly used for high input and high power application, uses a combination of a FB converter and a three-level HB converter that uses symmetrical duty cycle for control (Liu et al. 2014). As a result, the voltage stress is halved and the output current ripple is further improved, which can be further utilised to

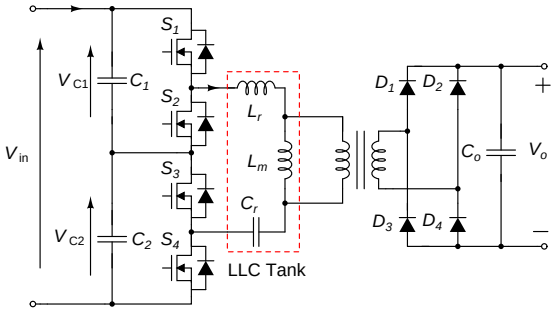


Figure 2.7: Three-level DC-DC converter with LLC resonant tank. This topology is used for HP and MP applications. The LLC resonant tank added to achieve soft switching operation and constant DC output voltage (Hossain et al. 2018, Coccia et al. 2007).

minimize the filtering requirement. Increasing the switching frequency decreases the overall performance of the converter due to a hard switching method, therefore the SS (ZVS/ZCS) strategy may address this limitation. Figure 2.9 shows a bidirectional DC-DC converter with a hybrid switching circuit (Yoo & Lee 2013). Moreover, several types of DiC converter and NPC based MC topologies have been studied (Yoo & Lee 2013, Adhikari et al. 2014). In the literature, more research has also focused shows on F-C based DC-DC converter topologies in literature (Parastar et al. 2015, Jin et al. 2014, Pan et al. 2005, Peng et al. 2002).

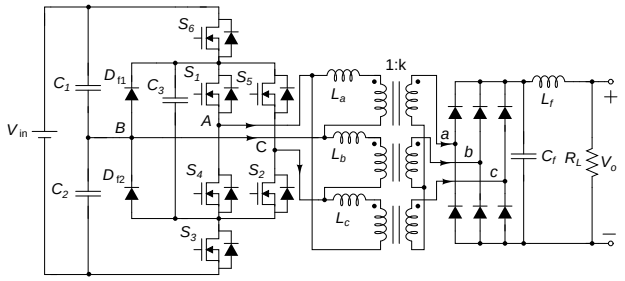


Figure 2.8: Three-phase three-level DC-DC converter topology. In this topology, the switching devices reduce to half of the input voltage and in the meantime, the output current ripple frequency significantly enhances. This topology suffers from higher switching losses due to hard switching technique, which degrade the overall performance of the converter (Hossain et al. 2018, Liu et al. 2014).

Figure 2.10 shows a four level (4L) F-C based bidirectional non-isolated DC-DC converter that contains of six switching operating cells creating three switching poles (Peng et al. 2002). Note that the converter (Figure 2.10) does not use any

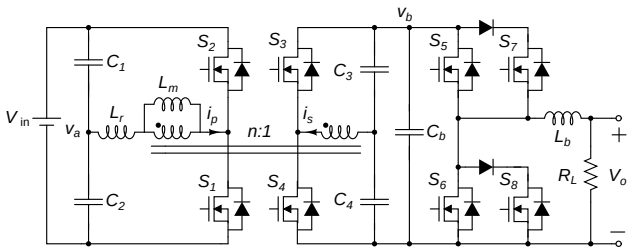


Figure 2.9: Two-stage isolated bidirectional DC-DC converter with hybrid switching circuit. The hybrid switching allow the continuous and parallel operation of various alternative sources (Hossain et al. 2018, Yoo & Lee 2013).

magnetic components with a pulse width modulation (PWM) technique to produce a fixed duty cycle. Further, the structure is usually used as a voltage multiplier (Peng et al. 2002). Therefore, these type of topologies have some limitations such as: complexity, high switching frequency, over voltage drop, non-modular layout, complicated switching method and bidirectional power flow limitation.

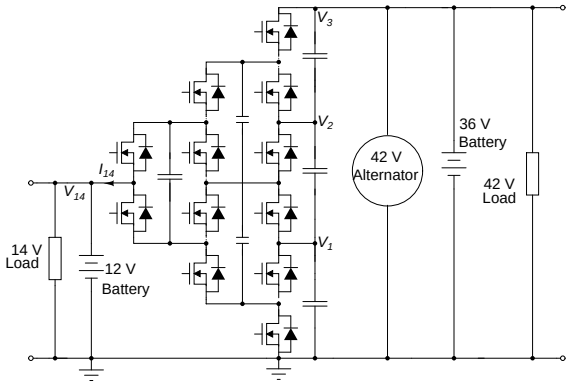


Figure 2.10: Multilevel (4 L) flying-capacitor (F-C) based bidirectional non-isolated DC-DC converter which consists of six switching cells. The switching cells are forming three switching poles. This type of topology operates at higher switching frequency to reduce the switching losses (Hossain et al. 2018, Peng et al. 2002).

Currently, the multi-level cascade DC-DC converter is gaining increased interest in photovoltaic (PV) applications (Hafez 2015, Morales-Saldana et al. 2002, Cai et al. 2014, Kashani et al. 2014, Khan & Tolbert 2007). Such a topology can be designed using either buck or boost converter for PV applications. A comparison between the three multi-level topologies is given in Table 2.1. As an example, a buck type multilevel cascade DC-DC converter topology proposed for PV applications is shown

in Figure 2.11 (Hafez 2015). The freewheeling diodes in this converter allows current bypassing in case of PV module failure. On the other hand, some active device components can have continuous operation during a fault condition. Performance comparison of Si based converter topologies is shown in Table 2.2. From the table, it can be seen that the bridge/multiphase converter is capable of delivering both high power at high output voltage in comparison to resonant and multilevel converters, although the resonant converter has the advantage that it can operate at high switching frequency. It worth mentioning that bridge, multiphase and multilevel converters can be based on BJT, MOSFET, or IGBT devices. Modulation control techniques, such as: PWM, phase shift pulse width modulation (PS-PWM), and dual-phase-shift pulse width modulation (DPS-PWM) can be used in the bridge/multilevel converter, whereas both resonant and multilevel converters are limited to PWM.

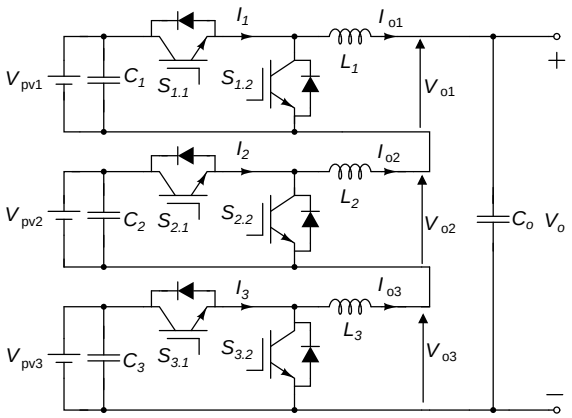


Figure 2.11: Multilevel cascaded DC-DC half-bridge (HB) buck converter topology for PV application. When PV module failure, the freewheeling diode of buck converter allows a current bypass path. The capacitor of cascade HB buck converter discharge is higher and voltage stress is lower (Hossain et al. 2018, Hafez 2015).

As can be noted from Table 2.1, cascade half bridge (CHB) MC is favourable for PV applications compare to diode-clamped (DiC), and flying-capacitor (F-C) based multilevel converters (MCs) because it uses fewer switches, has lower voltage stress, easier switching signal control, fault tolerance capability, lower harmonic distortion for higher switching frequencies, reduced circuit complexity, low cost, and smaller size.

Table 2.1: Performance comparisons of Si based three multilevel converter topologies (Zhang, Peng & Qian 2004, Pan et al. 2005, Peng et al. 2002, Hafez 2015, Morales-Saldana et al. 2002, Cai et al. 2014, Kashani et al. 2014, Khan & Tolbert 2007).

Parameters	Diode-clamped (DiC)	Flying-capacitor (F-C)	Cascaded H-bridge (CHB)
Discharge	Less	Higher	Higher
Filter component (s)	Reasonable	Bulk	Light
Modular structure	No	No	Yes
Voltage stress	N/A	Higher	Lower
Tolerate in fault	N/A	Unable	Capable
Necessity of switching devices	Higher	Less	Lower
Switching system	N/A	Difficult	Easier
Gate signal	N/A	N-phase signal	Two-phase signal
Voltage drop on active devices	Reasonable	Higher	Lower
Capacitors used	N/A	Higher and different values	Lower and same values

Table 2.2: Performance comparison of Si based several power DC-DC converter topologies (Hossain et al. 2018).

Parameters	Resonant Converter	Multilevel Converter	Bridge/Multiphase Converter
Power rating (kW)	2.74, 5, 24, 50	2.75, 3, 12.6	2, 2.8, 3, 6, 40, 50
Output voltage (V)	400, 600	43, 700	60, 220, 280, 300, 350, 400,600, 2000
Switching frequency (kHz)	100, 120, 250, 750	33.3	10, 20, 25, 50, 100, 200, 256
Semiconductor devices	SCR, MOSFET	MOSFET	BJT, MOSFET, IGBT
Modulation and control	PWM	PWM, PS-PWM	PWM, PS-PWM, DPS-PWM
Control variable	Voltage control	Voltage Control/Current Control	Voltage Control/Current Control
Switching loss	High	Comparatively low	Low
Converter efficiency	Low	Comparatively high	High
References	Morman et al. (1972), Eno et al. (2005), Canales et al. (2002), Jacobs et al. (2004).	Kolar & Zach (1997), Liu et al. (2006).	Cho et al. (2000), Walter & De Doncker (2003), Zhang, Zhang, Xie, Jiao & Qian (2004), Mason & Jain (2005),. Pavlovsky et al. (2005), Liu et al. (2005).

2.3 Recent Progress and Development in Wide Bandgap Power Devices

New development of high efficiency power converters have emerged with the advancement of WBG power semiconductor materials (Ertugrul & Abbott 2020). In a majority of power converters, magnetic components (inductors and transformers) and capacitors contribute significantly to the overall converter size and cost. Therefore, to miniaturize and reduce the cost of an electrical energy processor, its switching frequency, f_{SW} must be increased (Shenai 2019). Emerging low-loss circuit components are required for high power applications. This is the basic reason for promising WBG

power devices; they also led to increased energy efficiency in traditional Si-based power converters and open new HV high-power conversion applications. Figure 2.12 shows an ON-state characteristic curve of a WBG power device as compared to a Si IGBT power device as a function of blocking voltage rating. It may be noted from the figure that the current density reduces for both Si IGBT and SiC MOSFET devices when increasing the blocking voltage rating.

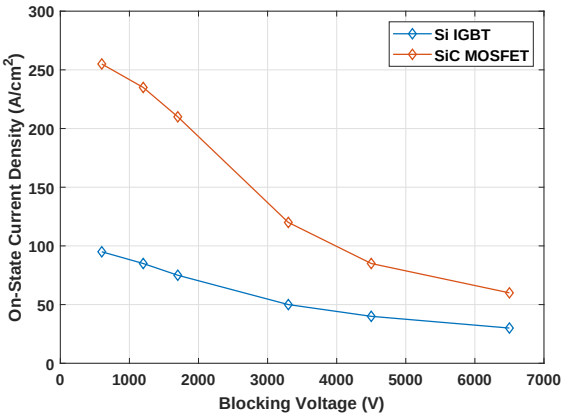


Figure 2.12: ON-state characteristics curve of WBG power device is compared with Si IGBT (Baliga 2015).

In the last few years, a large number of high frequency, high efficiency, integrated power electronics based on WBG devices using gallium arsenide (GaAs), SiC and GaN technologies have been reported (Bentini et al. 2011, Millan et al. 2014, Micovic et al. 2005), some converters are combined with Si or GaAs-based logic circuits for control (Pala et al. 2012, Pereira et al. 2015). The underlying logic functions in such control circuits can be integrated on the same die as the converter to develop a highly integrated, power efficient, and small area modules for a wide range of applications, such as electric vehicles (EVs), switched mode power supplies, DC motor drivers, etc. Such an approach, results in superior performance compared to existing GaN modules interfaced with Si- or GaAs-based technologies, while maintaining low cost (Ertugrul & Abbott 2020). Figure 2.13 shows performance of both GaN and SiC technologies in comparison with Si-based and demonstrate that GaN performance exceeds other technology in all aspects except for thermal conductivity, which is higher in the case of SiC technology (Boles 2018).

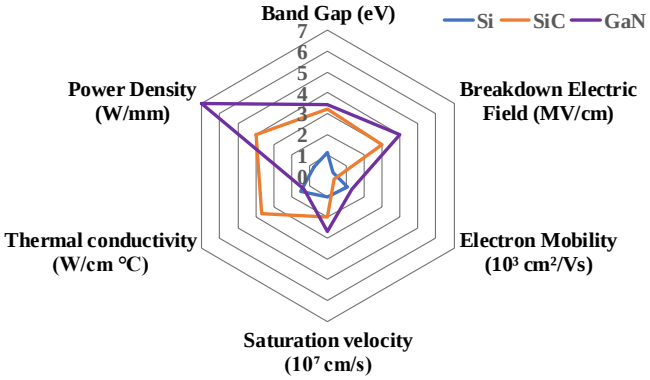


Figure 2.13: Summary of material properties for Si, SiC and GaN devices. The WBG semiconductor devices such as SiC and GaN represents high power density and high band gap compare to Si devices (Boles 2018).

2.3.1 SiC-devices

It may be noted that SiC power devices are the most developed WBG semiconductors. These devices have progressed significantly since 1987 by CREE Inc., which is the main provider of SiC wafers. Note that SiC Schottky diodes have higher blocking voltage capability compare to Si Schottky diodes. Apart from commercial devices, many other SiC devices are operated in the kilovolts (kV) range with minimized on-resistances such as 4H-SiC and 6H-SiC p-n diodes, Schottky diodes, insulated-gate bipolar transistors (IGBTs), thyristors, BJTs, several metal oxide semiconductor field effect transistors (MOSFETs), and gate turn-off thyristors (GTOs). Although there are MOSFETs rated at 600 V and 1000 V, the current is usually less than in a GaN HEMT, and the R_{DS} is at least two times or more than that of a GaN HEMT (Wang, Dong, Jiang, He, Hu, Ye & Ding 2019).

The use of SiC power devices can improve system level gains such as: minimization of switching losses, size, volume and increased efficiency. When SiC power devices are implemented in a hybrid electric vehicle (HEV) instead of Si power devices, the efficiency increases by 10%, and the heatsink size requirement is reduced to 1/3 of the original size (Ozpineci et al. 2001, Zhang et al. 2011). Currently, two SiC polytypes such as 6H-SiC and 4H-SiC are well studied in the research domain, but 4H-SiC is presently more dominant for power applications. Although both of these polytypes possess similar properties, however 4H-SiC is more popular than 6H-SiC because the

Table 2.3: Comparison Figure-Of-Merit for WBG semiconductors materials with respect to Si (Jain et al. 2008, Qian et al. 2017).

Parameters	Si	6H-SiC	4H-SiC	GaN
Johnson's figure of merit JFM	1.0	277.8	215.1	215.1
Baliga's figure of merit (BFM)	1.0	125.3	223.1	186.7
FET switching speed figure of merit (FSFM)	1.0	30.5	61.2	65.0
Bipolar switching speed figure of merit (BSFM)	1.0	13.1	12.9	52.5
FET power-handling-capacity figure of merit (FPFM)	1.0	48.3	56.0	30.4
FET power switching product (FTFM)	1.0	1470.5	3424.8	1973.6
Bipolar power handling capacity figure of merit (BPFM)	1.0	57.3	35.4	10.7
Bipolar power switching product (BTFM)	1.0	748.9	458.1	560.5

6H-SiC has a significantly higher anisotropic properties in terms of carrier mobility and thermal conductivity than the 4H-SiC counterpart (Qian et al. 2017).

Further, a performance comparison of promising power electronics technologies, using well-known figures of merit, normalised relative to Si-based transistors, are shown in Table 2.3. As can be seen, Si transistors present the poorest performance among the semiconductor materials, whereas SiC and GaN have almost the same figures of merit, except when it comes to thermal conductivity for SiC technology (Boles 2018). Hence, current research activities are directed toward creating GaN on different substrates to improve the thermal conductivity performance (Zhang et al. 2001, Li et al. 2016).

Recently, Infineon has released their CoolSiC^{TM} generation 6 (G6) for SiC Schottky barrier diodes with breakdown voltage 650 V [Infineon- IDH04G65C6, PG-T0220-2 data sheet]. This represents an enhancement over the CoolSiC^{TM} G5 via advancements such as a novel Schottky metal system. The implementation of highly efficient, compact and simple 3-phase inverter systems is currently limited by high dynamic losses operating at 1,200 V in silicon devices. Alternative designs using 600 V/650 V devices can result in partially improved efficiency. However, such designs result in higher cost and module complexity when integrated in multilevel topologies, resulting in more complex control systems. In addition, Infineon TRENCHSTOP^{TM} technology has provided high power IGBT modules from 1,200 V to 3,300 V with

Table 2.4: The static characteristics of SiC MOSFET for the model (Model IDH04G65C6-Infineon), (LSIC1MO170E1000 1700 V N-channel-Littelfuse), (GR350MT33J-3300 V), and Infineon IGBT4 for the model (FZ2000R33HE4-IGBT4) that are commercially available and in engineering samples.

Parameters	SiC MOSFET Infineon (IDH04G65C6)	SiC MOSFET Littelfuse (LSIC1MO170E1000 1700 V)	SiC MOSFET GenSiC (GR350MT33J-3300 V)	IGBT4 Infineon (FZ2000R33HE4 IGBT4)
Drain-source voltage (V_{DS})	650 V	1,700 V	3,300 V	3,300 V
Drain current (I_D)	4 A	3.5 A	400 A	2,000 A
Drain-source on-resistance, $R_{DS(on)}$	0.315 Ω	750 mΩ	350 mΩ	N/A
Maximum junction temperature (T_j)	150°C	150°C	150°C	150°C

a current rating from 200 A to 1,500 A, especially for motor control drives, wind energy systems, solar energy systems, uninterruptible power supply (UPS), and agricultural vehicles, which means much lower static losses, higher power density and softer switching (Mueller et al. 2018).

Furthermore, Littelfuse, Wolfspeed, and Microsemi provide advanced SiC devices that use Schottky barrier diodes with high breakdown voltage in the order of 1,700 V, while GeneSiC^{TM} has a newly developed 3,300 V, 400 A SiC power module. The static characteristics of SiC MOSFET for Infineon's IDH04G65C6, Littlefuse's 1,700 V N-channel LSIC1MO170E1000, the 3,330 V GR350MT33J, and Infineon's IGBT4 for the FZ2000R33HE4-IGBT4 module are listed in Table 2.4.

2.3.2 GaN-devices

At the heart of a high efficiency converter is a low loss, high voltage, high current power switch that can deliver variable output power. The high efficiency within a switching power converter is obtained by the choice of semiconductor technology used as well as the peripheral drive and control topology of the system. High-quality lateral heterostructures (e.g. aluminium mole fraction in AlGaN layers of GaN-capped AlGaN/GaN) with high electron mobility transistors (HEMTs) and high two dimensional electron gas (2DEG) density make GaN an ideal semiconductor of choice for power devices. One of the key benefits of a lateral device technology is its high integration density, which can be exploited for the development of on-chip peripheral control circuits (Wong et al. 2010).

In contrast to silicon design methodology developments, which have been in practice for almost 40 years, only the power devices themselves are integrated onto GaN chips. However, to enable low-cost, high efficiency circuits there is a need to integrate the control logic circuitry onto the GaN chips. This requires the development of new circuit, logic and design strategies to deal with this requirement. This arises because for the last 70 years the focus has been on silicon technology and billions of dollars have been invested into the development of that technology.

- GaN-rectifiers: Currently, most of GaN Schottky-diodes can be stated by using lateral configuration to overcome the conduction losses in GaN substrates (Zhan et al. 2001). Although both the forward and breakdown voltage in lateral GaN rectifiers are still high, where 9.7 kV breakdown voltage has been found on sapphire substrates (Zhang et al. 2001). Note that GaN rectifiers on Si substrates demand a significant attention because of their lower cost. Furthermore, currently, high-junction temperature GaN substrates, and 600 V GaN Schottky diodes are commercially available. Recently, a 1,500 V lateral GaN Schottky diode structure has been reported (Boles et al. 2013). Note that GaN Junction Barrier Schottky (JBS) diodes can further increase the operating voltage of these rectifiers from a 1,500 V to 3,000 V voltage range.

- HEMTs and power MOSFETs: One of the important features of GaN is the presence of a 2DEG formed in AlGaN/GaN lateral heterostructures due to a large conduction band. The existence polarization fields in AlGaN/GaN allows a large 2DEG carriers concentration with high electron mobility values between 1,200 and 2,000 cm^2/Vs. Figure 2.14 shows a normally-on GaN HEMT, where a negative bias is applied between gate and source to modulate the drain to source current. Nowadays, these devices are becoming more and more popular due to their high power switching frequency with outstanding performance trade-off between explicit on-resistance and breakdown voltage. In addition, they are well suited for power switching applications with ultrahigh bandwidth and as microwave power devices for cellular phone base stations.

  GaN-based HEMTs or GaN heterostructure FET (HFET) devices have been designed and developed on both sapphire and SiC substrates to demonstrate their output power ability from 1.1 W/mm initially in 1996 up to 40 W/mm

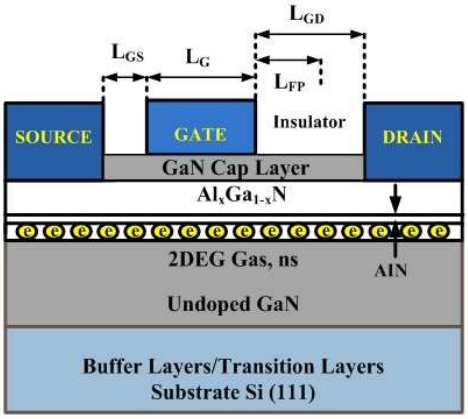


Figure 2.14: Cross section of a typically-on GaN HEMT. The negative bias is applied between gate and source to modulate the drain to source current. The GaN-based HEMTs devices have been designed and developed on both sapphire and SiC substrates to demonstrate their output power ability from 1.1 W/mm initially up to 40 W/mm recently (Millan et al. 2014, Wu et al. 2006).

recently (Asif Khan et al. 1994, Wu et al. 2006). Furthermore, GaN HEMTs are emerging with capability up to 10 kV, while GaN-based converters have already been established. One of the limitation due to the collapse current in these devices, which can lead to a reliability issue over long time (Ikeda et al. 2008). In this case, various fabrication approaches have been considered to improve the collapse current, of these the use of a superficial-charged-controlled n-GaN cap configuration in the device structure (Oku et al. 2008).

Note that the blocking voltage of AlGaN/GaN lateral heterostructures are higher than 1 kV (Yoshida et al. 2006), when mounted on Si substrates. Moreover, high blocking voltage capability and low on-resistance GaN HEMTs on semi-insulating SiC substrates have been realized, giving rise to a record figure-of-merit ($\sim 2,3 \times 10^9$ $V^2/\Omega{\cdot}cm^2$) beyond the 6H-SiC theoretical limit (Bahat-Treidel et al. 2010). Recently, a 2.2 kV GaN HEMTs has been fabricated on Si that attains a significant advancement over HEMT configurations on bulk Si (Srivastava et al. 2011). On the other hand, GaN HEMTs have also been established on semi-insulating SiC for high power generation using field-plated gates (Boutros et al. 2006).

Note that, for power applications, normally-on GaN HEMTs are problematic and that normally-off GaN HEMTs offer much higher performance. For this reason, normally-off GaN HEMT switches, shown in Figure 2.15 (Saito et al. 2006), are readily finding applications in power systems, where the AlGaN layer under the very narrow gate region produces a positive threshold voltage. Normally-off GaN HEMTs structures can be produced using a fluorine-based plasma treatment of the gate region instead of the narrow gate region of AlGaN configuration (Cai et al. 2006). As a result, the threshold voltage is achieved via plasma treatment that incorporates fluorine ions in the AlGaN barrier. It has been shown, using a gate recess structure combined with a fluorine-based surface treatment of normally-off AlGaN/GaN HEMTs has been as excellent solution for obtaining high performance (Palacios et al. 2006). In addition, a normally-off p-n gate HEMTs can also be utilised in a 2DEG depletion layer for observation as shown in Figure 2.16.

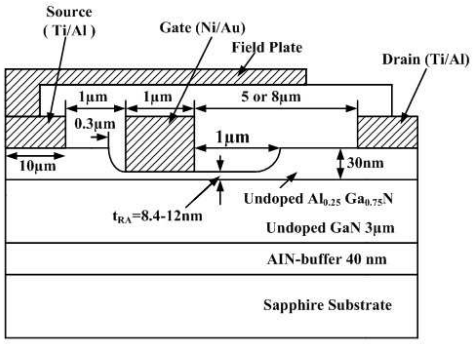


Figure 2.15: Recessed-gate of a typically-off GaN HEMT structure. The off-GaN HEMT provide much higher performance in power applications, where the AlGaN layer under the very narrow gate region produces a positive threshold voltage. The threshold voltage is obtained via plasma treatment that incorporates fluorine ions in the AlGaN barrier (Millan et al. 2014, Saito et al. 2006).

Generally, lateral GaN MOSFETs show outstanding performance in normally-off operation and large conduction band offset for high power applications. In this case, a large conduction band offset has some reliability problems and less susceptibility for injection of hot electrons, in particular those related to surface and current collapse—this makes them an alternative to SiC MOSFET and GaN HEMTs (Millan et al. 2014, Huang et al. 2008). In the case of SiC

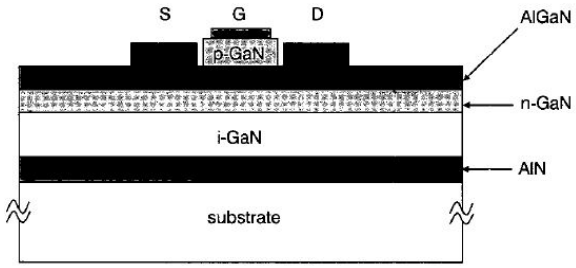


Figure 2.16: Schematic diagram of a typically-off p-n gate GaN HEMT. The normally off p-n Schottky gate is to utilised isolate the gate (Hu et al. 2000).

MOSFETs, the presence of interface states limits performance. To overcome these limitations, GaN MOSFETs can be designed by incorporating the AlGaN/GaN heterostucture into the reduced surface field (RESURF) region as shown in Figure 2.17.

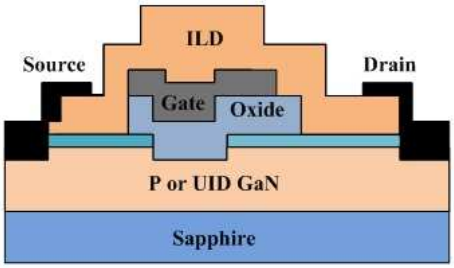


Figure 2.17: Schematic diagram of a lateral GaN hybrid MOS-HEMT. The GaN MOSFETs is designed by incorporating the AlGaN/GaN hetorostucture into the reduced surface field region (Huang et al. 2008).

2.3.3 GaN cascode configurations

The basic GaN HEMT structure is typically an ON-state device (Mitova et al. 2013, Green et al. 2000, Shinohara et al. 2018). In order to increase its performance and applicability, manufactures are using the cascode configuration to obtain normally OFF-state behavior.The commercially available cascode configuration typically has a voltage rating of around 600 V and is constructed using a conventional MOSFET and a high-voltage depletion GaN. As an example, the depletion mode (D-Mode) GaN HEMT device is connected in series with low voltage (LV) Si MOSFET (normally 30 V and low ON-state resistance) as shown in Figure 2.18. The cascode

structure results in an enhancement switch by applying the voltage pulse on the LV Si MOSFET gate in order to regulate the high voltage D-Mode GaN HEMT to turn ON or OFF (Ramachandran & Nymand 2017, Li et al. 2016, Elrajoubi et al. 2018).

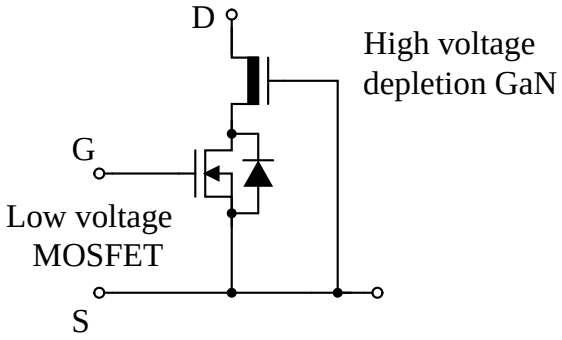


Figure 2.18: GaN cascode configuration. The depletion mode (D-Mode) GaN HEMT device is connected in series with low voltage (LV) Si MOSFET (normally 30 V and low ON-state resistance). When apply the voltage pulse on the low voltage Si MOSFET gate, the depletion mode (D-Mode) GaN HEMT regulate the high output voltage to turn ON and OFF.

When the gate is in the ON state, the GaN HEMT channel path can permit current in both directions, because it does not have any internal body diode. The conduction loss only occurs in the GaN HEMT due to low ON-state resistance of the low voltage Si MOSFET. In most cases, the MOSFET body diode in a boost (Kim & Kim 2013, Gu & Zhang 2013), buck, or buck-boost converter (Wei et al. 2012, Alonso et al. 2013) does not conduct current. In the case of a MOSFET body diode in a HB inverter, the diode conducts current with complementary gating pulses. The MOSFET body diode results in high conduction losses during large dead-band time. The short dead-band time in GaN switches produces low conduction losses, which may be negligible. In addition, the reverse recovery of the MOSFET body diodes has a negative effect on the performance of the converter, CoolMOS^{TM} CFD from Infineon may recover in resonant switching topologies in high power Switch Mode Power Supply (SMPS) applications like telecom, server and EV charging (Liu & Ruan 2007).

- Gate resistor: The GaN switch can be turned ON or OFF by controlling the gate of the low voltage MOSFET. Generally, the gate resistor is used to control the switching time-interval to turn ON and OFF the MOSFET. A low

switching losses is obtained due to low voltage MOSFET. Therefore, unlike the Si-MOSFETs, the gate resistance of GaN switch plays a negligible role in the switching performance. In addition, manufacturers of these devices recommend driving GaN switch without connecting any gate resistor (Mitova et al. 2013).

- GaN switch characterization: The important datasheet specifications of the GaN switch used in this chapter are tabulated in Table 2.5. The GaN switch is in a TO-220 package. The GaN device characterization is vital for predicting its switching and conduction loss. This is essential of when designing and analysing the thermal characteristics of a power converter to calculate its efficiency. Usually, device manufacturers provide several loss curves that are either theoretical or experimental, under different operating conditions (Mohan et al. 2003).

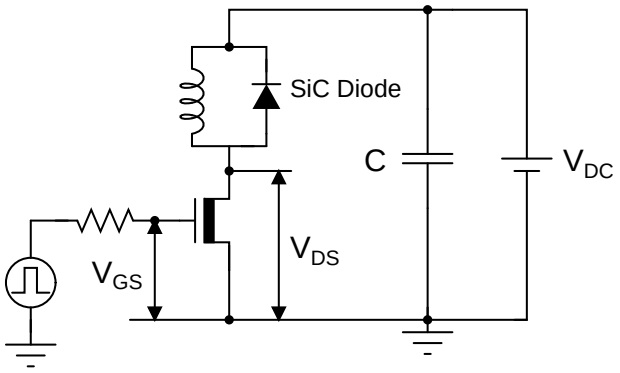


Figure 2.19: GaN characterization setup.

The basic GaN switch schematic circuit diagram of ON-state device characterization is shown in Figure 2.19. To turn ON a GaN switch, a small duration of gate pulse can be applied. The conduction voltage drop ($V_{\mathrm{DS(on)}}$), and drain current (I_{D}) can be measured. The experimental results can be presented at several junction temperature (T_j), where GaN switch will be heated up to the desired temperature using a heating resistor. The on-state resistance ($R_{\mathrm{DS(on)}}$) at operating temperature (T_c) and drain current (I_{D}) can be expressed by:

$$R_{\mathrm{DS(on)}} = \frac{V_{\mathrm{DS(on)}}}{I_{\mathrm{D}}} \ . \tag{2.1}$$

Table 2.5: Ratings of GaN switch in TO-220 package (TPH3006PS).

Parameters	Min	Typical	Max	Test Conditions
Maximum drain-source volt-age ($V_{\mathrm{DSS-MAX}}$)	600 V	-	-	$V_{\mathrm{GS}} = 0$ V
Gate threshold voltage ($V_{\mathrm{GS(th)}}$)	1.35 V	1.8 V	2.35 V	$V_{\mathrm{DS}} = V_{\mathrm{GS}}$, $I_{\mathrm{D}} = 1$ mA
Drain-source on-resistance, $R_{\mathrm{DS(on)}}$ at $T_j = 25°\mathrm{C}$	-	0.15 Ω	0.18 Ω	$V_{\mathrm{GS}} = 8$ V, $I_{\mathrm{D}} = 11$ A, $T_j = 25°\mathrm{C}$
Drain-source on-resistance, $R_{\mathrm{DS(on)}}$ at $T_j = 175°\mathrm{C}$	-	0.33 Ω	-	$V_{\mathrm{GS}} = 8$ V, $I_{\mathrm{D}} = 11$ A, $T_j = 175°\mathrm{C}$
Drain-to-source leakage current, $I_{\mathrm{DSS(on)}}$ at $T_j = 25°\mathrm{C}$	-	2.5 μA	90 μA	$V_{\mathrm{DS}} = 600$ V, $V_{\mathrm{GS}} = 0$ V, $T_j = 25°\mathrm{C}$
Drain-to-source leakage current, I_{DSS} at $T_j = 150°\mathrm{C}$	-	10 μA	-	$V_{\mathrm{DS}} = 600$ V, $V_{\mathrm{GS}} = 0$ V, $T_j = 150°\mathrm{C}$
Gate-to-source forward leakage current, I_{GSS}	-	-	100 nA	$V_{\mathrm{GS}} = 18$ V
Gate-to-source reverse leakage current, I_{GSS}	-	-	-100 nA	$V_{\mathrm{GS}} = -18$ V
Input capacitance, C_{ISS}	-	740 pF	-	$V_{\mathrm{GS}} = 0$ V, $V_{\mathrm{DS}} = 100$ V, $f = 1$ MHz
Output capacitance, C_{OSS}	-	133 pF	-	$V_{\mathrm{GS}} = 0$ V, $V_{\mathrm{DS}} = 100$ V, $f = 1$ MHz
Reverse transfer capacitance, C_{RSS}	-	3.6 pF	-	$V_{\mathrm{GS}} = 0$ V, $V_{\mathrm{DS}} = 100$ V, $f = 1$ MHz
Turn-On Delay, $t_{\mathrm{d(on)}}$	-	4 ns	-	$V_{\mathrm{DS}} = 480$ V, $V_{\mathrm{GS}} = 0 - 10$ V, $I_{\mathrm{D}} = 11$ A, $R_{\mathrm{G}} = 2\ \Omega$
Rise Time, t_r	-	3 ns	-	$V_{\mathrm{DS}} = 480$ V, $V_{\mathrm{GS}} = 0 - 10$ V, $I_{\mathrm{D}} = 11$ A, $R_{\mathrm{G}} = 2\ \Omega$
Turn-Off Delay, $t_{\mathrm{d(off)}}$	-	10.5 ns	-	$V_{\mathrm{DS}} = 480$ V, $V_{\mathrm{GS}} = 0 - 10$ V, $I_{\mathrm{D}} = 11$ A, $R_{\mathrm{G}} = 2\ \Omega$
Fall Time, t_f	-	3.5 ns	-	$V_{\mathrm{DS}} = 480$ V, $V_{\mathrm{GS}} = 0 - 10$ V, $I_{\mathrm{D}} = 11$ A, $R_{\mathrm{G}} = 2\ \Omega$

It is strongly recommend that the measure on-state resistance ($R_{\mathrm{DS(on)}}$) characteristics depends on the junction temperature and does not depend on the drain current.

2.4 WBG Power DC-DC Converter Topologies

Renewable energy sources such as solar PV are a promising alternative for clean and efficient energy production. Renewable energy sources are probably the most demanding of all distributed power generation. However, it is necessary to sets strict limits on the amount of ripple current, common mode voltage and load variations. The typically low output voltage from a renewable sources stack needs to be boosted to a higher voltage level before connected to the grid (Roy et al. 2018, Alzahrani et al. 2019, Ramadass & Chandrakasan 2007). So, there is a need for high efficiency power converters, and in the case of low voltage, high current and galvanic isolation. It is worth noting that, the implementation of such converters is not a trivial task. The favorable characteristics of these DC-DC converters are cost, reliability, wide input range—flexibility, scalability and efficiency (Tavakoli et al. 2020, Ramadass & Chandrakasan 2007, Rehman et al. 2015). Of these, scalability can refer to the different power ratings and the ability to select a design topology that results in

lower losses and less stress on the converter's components in terms of the maximum voltage or current values. Note that there are two types of losses seen in power semiconductors, namely, (i) static losses, which occur due to finite response time that a device takes in response to an applied voltage, while (ii) conduction losses are function of the voltage drop across the device and the current passing through it. For low-voltage and high-current applications, conduction losses dominate (Rehman-Shaikh et al. 2007).

WBG power DC–DC converter topologies can be classified into SiC and GaN based DC-DC converters as shown in Figure 2.20, while Table 2.6 provides some qualitative performance comparison between these topologies. As an example, several types of WBG-based high frequency high power DC-DC converter topologies such as (i) GaN FET and SiC Schottky diode based boost converter, (ii) GaN HEMTs SS converter, (iii) critical current mode (CRM) bidirectional buck-boost converter, (iv) double- hetorostructure FET (DHEFET) converter, (v) high breakdown voltage GaN heterojunction-field-effect transistor (GaN-HFET), (vi) GaN isolated FB converter), (vii) GaN-based HB resonant converter for speed control of Brushless DC (BLDC) motor, (viii) non-isolated DC-DC buck converter, (ix) SiC Schottky/GaN E-HEMT based DC-DC ZETA converter, (x) SiC-cascode based Interleaved DC-DC SEPIC converter, and (xi) SiC based isolated bidirectional DC-DC converter are shown in Figures (2.21-2.31).

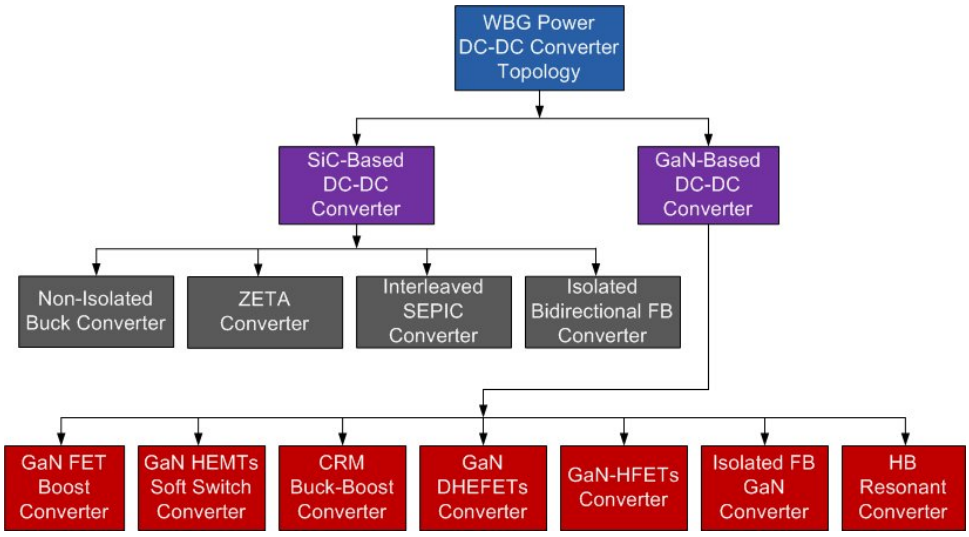


Figure 2.20: Classification of WBG power DC–DC converter topologies.

Table 2.6: Performance comparisons of SiC and GaN-based DC-DC converter topologies.

Parameters	SiC-based converter topologies	GaN-based converter topologies
Switching speed	Lower	Higher
Switching frequency	Lower	Higher
Power loss	Lower	Higher
Power density	Medium	Higher
Converter size	Medium	Smaller
Operating temperature	Higher	Higher
Discharge	Lower	Higher
Filter component	Resonable	Light
Voltage stress	Medium	Lower
Voltage drop on active devices	Medium	Lower
Control mechanism	Easier	Compex
Control variable	Multiple	Multiple
Complexity	Less	Higher
Necessity switching device	Less	Lower
Efficiency	Lower	Higher

2.4.1 GaN FET and SiC Schottky diode based boost converter

Boutros et al. (2009), proposed a 360 V/180 W boost converter using GaN FET and SiC Schottky operating at 200 kHz switching frequency, with an efficiency better than 92% as shown in Figure 2.21. The converter was built with normally-off GaN-on-Si HEMTs to allow to high breakdown voltage ($V_B > 1100$ V), low-leakage current ($< 10\ \mu$A/mm at $V_B/2$), highest peak current $I_{\max} = 5$ A, and the highest $V_B^2/R_{\text{on,sp}}$ ratio of 272 MW/cm^2. Table 2.7 shows a performance summary of this 1:2 boost converter for a normally-off GaN-on-Si device.

2.4.2 GaN HEMTs based SS Class-Φ_2 converter

A Class-Φ_2 converter topology that uses a GaN HEMT as soft-switching devices is shown in Figure 2.22 (Zulauf et al. 2018), which has been utilized in HP applications under zero-voltage/zerocurrent conditions with very high-speed switching range in the HF-to-VHF range (Zulauf et al. 2018). The converter switching loss is function

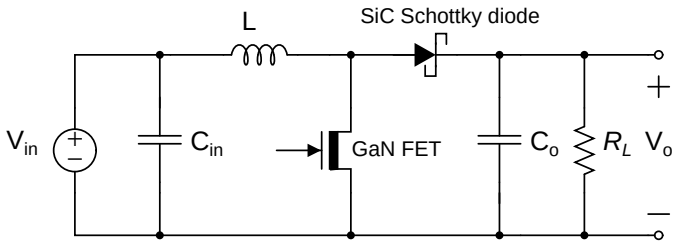


Figure 2.21: Schematic of 1:2 boost converter using GaN FET and SiC Schottky diode. A dynamic load was used to hold the output current at 0.5 A while ramping the output voltage to 360 V (Boutros et al. 2009).

Table 2.7: Performance summarised of 1:2 boost converter for a normally-off GaN-on-Si device (Boutros et al. 2009).

Parameters	Symbol	Value
Output power	P_o	180 W
Output voltage	V_o	360 V
Switching frequency	f_{sw}	200 kHz
Breakdown voltage	V_B	> 1100 V
Low-leakage current	i_c	$< 10\ \mu\mathrm{A/mm}$
High peak current	$I_{\max}$	5 A
Highest ratio	$\mathrm{V_B}^2/\mathrm{R_{on,sp}}$	$272\ \mathrm{MW/cm^2}$
Breakdown field	F_B	$95\ \mathrm{V}/\mu$m
Efficiency	η	>92%

of capacitance, voltage, and frequency, a decrease in any of these parameters leads to reduced loss. For verification, datasheet parameters (typical) for the GaN device are used from every manufacturer with commercially available voltage ratings over 600 V_{DS}. The selected GaN package GS66504B HEMT has the best combination of the drain–source ON-resistance ($R_{\mathrm{DS,ON}}$), he output capacitance (C_{OSS}), and the input capacitance (C_{ISS}) for the planned family of converters. The performance of GaN package GS66504B HEMT model is shown in Table 2.8.

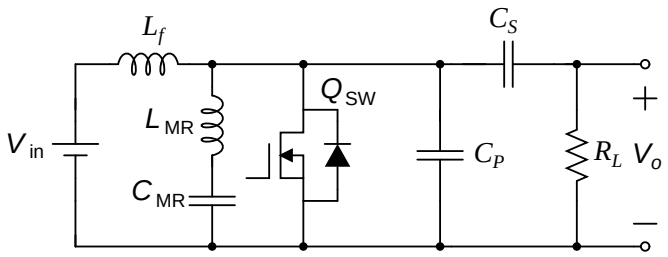


Figure 2.22: GaN-based HEMTs (GaN HEMTs) soft switch Class-Φ_2 converter. The GaN-based soft switched converters operate in high power applications under zero-voltage/zero-current switching and can operate at frequencies in the HF or VHF ranges (Zulauf et al. 2018).

Table 2.8: Performance of GaN package GS66504B HEMT model at several frequency (Zulauf et al. 2018).

Parameters	10 MHz	30 MHz	54.24 MHz
P_{IN}	1185 W	1046 W	1003 W
η	94.5%	93.5%	93.5%
I_{RMS}	10.9 A	9.6 A	10.9 A
P_{DISS}	5.4 W	10.5 W	17.1 W
$V_{DS,MAX}$	603 V	606 V	540 V

2.4.3 GaN-based CRM bidirectional buck-boost converter

The GaN-based critical current mode (CRM) bidirectional buck-boost converter with an inverse coupled inductor is shown in Figure 2.23, which can be continuously driven at high switching frequency (MHz range) with low switching loss and driving loss, and also is more compact in physical size (Huang et al. 2016). The advantage of the inverse coupled inductor is a reduced resonant time period in CRM compared to non-coupled inductor with also improved soft switching and circulating energy when the duty cycle is less than 50% and greater than 50%, respectively.

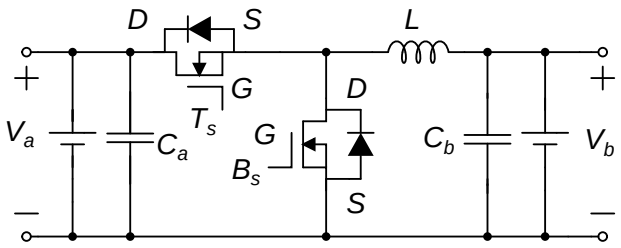


Figure 2.23: GaN-based CRM (GaN CRM) bidirectional buck-boost converter with an inverse coupled inductor (Huang et al. 2016).

2.4.4 E-mode GaN double-heterostructure FET (GaN DHEFET) boost converter

A 100 W Enhancement-mode (E-mode) GaN double-heterostructure FET (GaN DHEFET) boost converter is shown in Figure 2.24. For switching application, E-mode GaN devices have been proposed in the literature (Kanamura et al. 2010) to build E-mode GaN transistors by using a triple cap layer coupled with recessed gated structure and using high-k gate dielectric material. Recently, E-mode devices have been proposed to obtain high efficiency values of 96.1% and 93.9% at switching frequencies of 500 kHz and 850 kHz, respectively (Das et al. 2011). The high potential of GaN-on-Si devices for high-frequency power switching applications shown in Table 2.9.

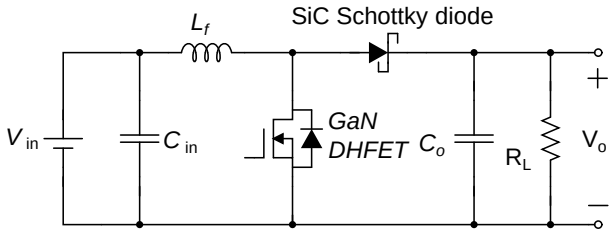


Figure 2.24: GaN-based double-heterostructure FETs (GaN DHEFETs) converter. Recently, E-mode devices have been proposed to obtain high efficiency (Das et al. 2011).

2.4.5 GaN heterojunction-field-effect transistor (GaN-HFET)

Mishima & Morita (2017) proposed a novel zero-voltage soft-switching bridgeless active rectifier based multiresonant 700 W DC-DC power converter, while using a

Table 2.9: E-mode GaN DHEFET based converter specifications and efficiency demonstrated at several switching frequencies (Das et al. 2011, Choi & Young 2010).

Parameters	Symbol	Value
Output power	P_o	100 W
Drain-source voltage	V_{DS}	140 V
Total gate charge	Q_G	11 nC
Drain-source on-resistance	$R_{\mathrm{DS,ON}}$	2.5 Ω
Switching frequency	f_{sw}	500 kHz and 850 kHz
Efficiency	η	96.1% and 93.9%
Rise time	t_r	5 ns
Fall time	t_f	20 ns

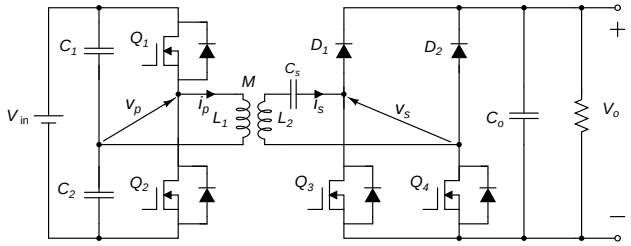


Figure 2.25: IPT-ZVS converter using GaN heterojunction-field-effect transistor (GaN-HFET) (Mishima & Morita 2017).

high breakdown voltage GaN heterojunction-field-effect transistor (GaN-HFET) for an inductive power transfer (IPT) system as shown in Figure 2.25. This converter obtains high efficiency due to low switching losses and normally-off operation. The performance comparison of this GaN-HFET converter with super junction MOSFET (SJ MOSFET) based converter is given in Table 2.10.

2.4.6 Isolated FB DC-DC GaN converter

Figure 2.26 shows the GaN FET isolated FB converter, which is attractive for synchronous rectification and has a high efficiency in the order of 98.8%. Moreover, GaN-based FETs can achieve high efficiency power conversion even with hard switching topologies. Unlike Si MOSFETs, GaN-base FETs have no reverse recovery

Table 2.10: Electrical characteristics of GaN-HFET and SJ-MOSFET in comparison (Mishima & Morita 2017).

Parameters	Symbol	GaN-HFET PGA26C09DV (panasonic)	SJ-MOSFET IXKC-15N60C5 (IXYS)
Drain-source voltage	V_{ds}	600 V	600 V
Drain current	I_d	15 A	15 A
Gate threshold voltage	V_{th}	1.2 V	3.0 V
Drain-source on-resistance	$R_{\mathrm{DS,on}}$	71 mΩ	150 mΩ
Gate charge	Q_g	9 nC	40 nC
Input capacitance	C_{iss}	115 pF	1100 pF
Output capacitance	C_{oss}	80 pF	70 pF
Dead time interval	t_d	500 ns	500 ns

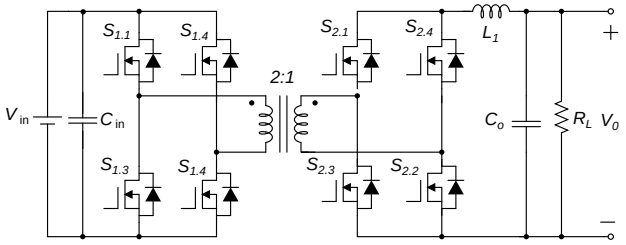


Figure 2.26: GaN-based isolated full bridge DC-DC step down converter. This topology has no reverse recovery losses because no minority carriers are engaged in the reverse diode conduction (Ramachandran & Nymand 2017).

losses because no minority carriers are engaged in reverse diode conduction (Park & Rivas-Davila 2017, Ramachandran & Nymand 2017). On the other hand, high forward voltage drop occurs due to forward diode conduction losses. These losses can be minimized by appropriate selection of the duty cycle of each switch. The GaN device package EPC2010C and EPC2001C different transistors are used to observe the converter performance, with a beakdown voltage of 200 V and 100 V, respectively. Compared to an equivalent silicon MOSFET, GaN devices have low output charge, very low gate drive losses, and zero reverse recovery losses. Table 2.11 shows the performance comparison of Land Grid Array (LGA) GaN FET with alternative Si MOSFET.

Table 2.11: Performance comparison of Land Grid Array (LGA) GaN FET with alternative Si MOSFET (Ramachandran & Nymand 2017).

Device (package)	GaN FET (LGA)	Si MOSFET #1 (Power56)	Si MOSFET #2 (SuperS08)
Area (mm^2)	6.6	31.7	30.9
$R_{\mathrm{DS(on)}}(\mathrm{m}\Omega)$	5.6	3.3	4
Drain-source on-resistance, $R_{\mathrm{DS(on)}} \times$ Area ($\Omega\mathrm{m}^2$)	37	105	124
Input capacitance, C_{iss} (pF)	770	2945	2320
Output capacitance, C_{oss} (pF)	430	1730	1070
Output charge, Q_{oss} (nC)	31	123	120
Output reverse recovery charge, Q_{oss} (nC)	0	57	76

2.4.7 GaN-based HB resonant converter for BLDC motor

A GaN-based HB resonant converter operating at 100 kHz switching frequency for BLDC (Niknejad et al. 2017) is shown in Figure 2.27. This converter uses GaN FETs switches instead of Si-based switches, which realizes a Switched Mode Power Supply (SMPS) with compact size. The use of GaN switches not only reduces the size of converter but also improved its efficiency in comparison to Si-based counterparts. A resonant circuit is also engaged in this arrangement, which allow for ZVS and ZCS to reduce the voltage and current stress on GaN switches. Table 2.12 shows a comparison between GaN FET and Si-based MOSFET.

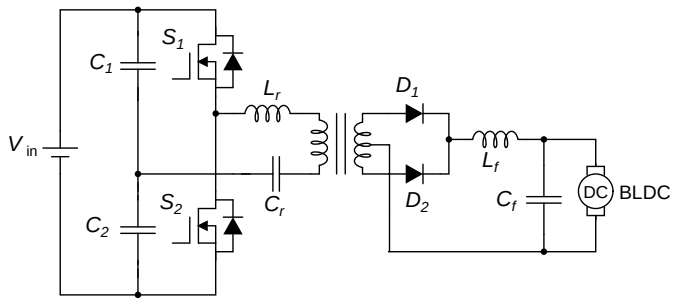


Figure 2.27: GaN-based HB resonant converter for BLDC motor (Niknejad et al. 2017).

Table 2.12: Comparison of GaN FET and Si MOSFET (Niknejad et al. 2017).

Parameters	GaN FET (GS66508T)	Si-MOSFET (Infineon SPP20N60CFD)
Output voltage, V_o	12 V	12 V
Output current, I_o	1.5 A	1.5 A
Efficiency, η	93.87%	71.63%
Power loss, P_{diss}	1.19 W	6.62 W
Temperature, T_j	41.6°C	62.5°C
Drain-source on-resistance, $R_{\text{DS(on)}}$	0.05 Ω	0.22 Ω
Input capacitance, C_{iss}	260 pF	2400 pF
Output capacitance, C_{oss}	65 pF	780 pF
Parasitic inductance, L_p	10 nH	150 nH

2.4.8 Non-isolated DC-DC buck converter based on Si-MOSFET, SiC-JFET and GaN-transistor

A non-isolated DC-DC buck converter is shown in Figure 2.28 (Al-bayati et al. 2017), which is designed using Si-MOSFET, SiC-JFET and GaN device for an industrial application. Note that selected SiC devices were used for both lower and higher voltage range, while the GaN devices are used for lower voltage range. However, the low voltage WBG power devices show outstanding performance in comparison to conventional Si-based power devices. They operate with a gate voltage (V_{GS}) of +25 V and −25 V that is applied to turn on and off the Si-MOSFET respectively, whereas a gate voltage of +3 V and −15 V is supplied to turn on and off a SiC-JFET, respectively. On the other hand, a gate voltage +6 V and 0 V is used to turn on and off a GaN transistor.

In addition, the switching energy losses for Si-MOSFET during turn-on and turn-off conditions are 218 μJ and 6 μJ, respectively. While switching energy losses for SiC-JFET during turn-on and turn-off conditions are 26.731 μJ and 12.058 μJ, respectively. Whereas the switching energy losses for the GaN-transistor are 17.987 μJ and 8.1175 μJ during the turn-on and turn-off condition, respectively. Table 2.13 shows a performance comparison of several power devices.

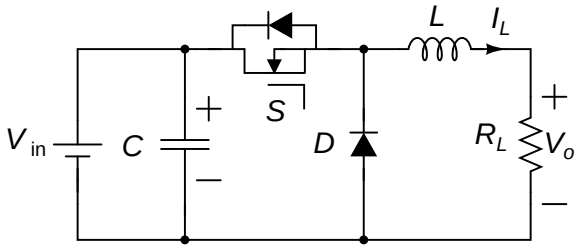


Figure 2.28: Non-isolated DC-DC buck converter (Al-bayati et al. 2017).

Table 2.13: Performance comparison of several power devices (Al-bayati et al. 2017).

Parameters	Si-MOSFET (R6020PNJ)	SiC-JFET (UJN1205Z)	GaN-transistor (GS66516B)
Breakdown voltage (V)	600	1200	650
Rated current (A)	20	38	60
Junction temparature (°C)	150	175	150
Switching energy losses during turn-on and turn-off (μJ)	218.72 and 6.0312	26.731 and 12.058	17.987 and 8.1175
Gate-source voltage during turn-onn and turn-off (V)	+25 and -25	+3 and -15	+6 and 0
Gate resistance (Ω)	13.4	5	5

Note that the design requirements depend on the size of power converter and power density by many applications (Moradpour & Gatto 2018). The selection of switching frequency is most important for the converter to operate the power switches with high efficiency. This is because converter switching loss depends on the selection of switching frequency, where high switching frequency leads to higher switching loss. On the other hand, high switching frequency can result in smaller reactive components, facilitating integration and leading to a more compact converter. The total power loss and overall efficiency are calculated for several power devices with 20 kHz to 200 kHz switching frequency at a junction temperature of 150°C as shown in Table 2.14. It is clear that the power loss of the converter dramatically increases with increased switching frequency, resulting in a degradation of the overall efficiency. According to analysis of the total power losses the GaN-based converter provides the best performance efficiency. Noted that the efficiency of Si-MOSFET, SiC-JFET and GaN-transistor based converter are 96%, 97.85% and 98.25%, respectively up to a 20 kHz switching frequency.

Table 2.14: Power loss and efficiency calculated by using various power devices with 20 kHz to 200 kHz switching frequency at junction temperature of 150°C (Al-bayati et al. 2017).

Parameters	Si-MOSFET/Si-diode based converter		SiC-JFET/SiC-Schottky diode based converter		GaN-transistor/SiC-Schottky diode based converter	
Switching frequency (kHz)	power losse (W)	efficiency (%)	power losse (W)	efficiency (%)	power losse (W)	efficiency (%)
20	9.41	96	5.19	97.85	4.92	98.25
80	21.72	91	7.57	97	6.63	97.23
140	37.61	87	10	95.75	8.34	96.85
200	52.64	83	12.46	95	10.07	96

2.4.9 SiC Schottky/GaN E-HEMT based DC-DC ZETA converter

In Al-bayati & Matin (2018), a DC-DC ZETA converter was proposed for high step-up applications by using a Schottky/GaN E-HEMT device as shown in Figure 2.29. This converter can produce continuous output current and noninverting output voltage.

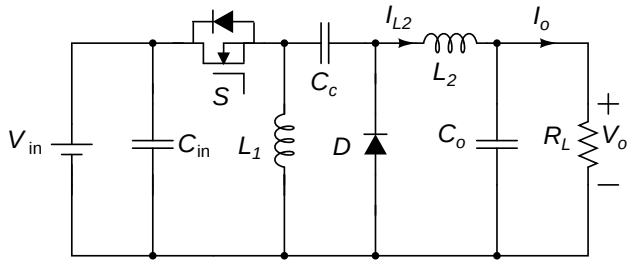


Figure 2.29: SiC Schottky/GaN E-HEMT based DC-DC ZETA converter (Al-bayati & Matin 2018).

For performance evaluation, several types of semiconductor power devices such as: Si-MOSFET (R6047ENZ1), SiC Schottky diode (CPW5-0650-Z030B) and GaN E-HEMT (GS66506T) are integrated in this converter. During the test condition, the Si-MOSFET/SiC Schottky diode is turned-on with +15 V and turned-off with -15 V at the gate. While the turn-on gate voltage of +6 V and turn-off gate voltage of 0 V are used for the GaN E-HEMT/SiC Schottky diode. The overall efficiency using these devices are 96.186%, and 98.082% for the Si-MOSFET/SiC Schottky diode and GaN E-HEMT/SiC Schottky diode, respectively at 48 V of input voltage. Table 2.15 shows the performance comparison of DC-DC ZETA converter based on several semiconductor power devices.

Table 2.15: Performance comparison of DC-DC ZETA converter based on several semiconductor power devices (Al-bayati & Matin 2018).

Parameters	Si-MOSFET/SiC Schottky diode (R6047ENZ1)	GaN E-HEMT/SiC Schottky diode (GS66506T)
Breakdown voltage (V)	600	650
Rated current (A)	47	22.5
Junction temparature (°C)	150	150
Switching energy losses during turn-on and turn-off (μJ)	44.219 and 23.317	24.15 and 7.77
Gate-source voltage during turn-on and turn-off (V)	+15 and -15	+6 and 0
Gate resistance (Ω)	5	5
Overall efficiency (%) at $f_{sw} = 100$ kHz, and $V_{in} = 48$ V	96.186	98.082

2.4.10 SiC-cascode based Interleaved DC-DC SEPIC converter

Typically, Interleaved SEPIC converters can be broadly used in renewable power generation systems, including PV and fuel cell, which are facing the critical problems of high-input current ripples and varying low-output voltages. These problems can be overcome by applying the interleaved SEPIC converter as shown in Figure 2.30 (Alharbi et al. 2018). The interleaved method is well-recognised, which is applied to DC-DC converters in order to generate more power and reduce the harmonic distortion. In order to evaluate the performance of Si-MOSFET/Si-diode and SiC-JFET/SiC-Schottky diode power devices, the interleaved DC-DC SEPIC converter is integrated with these power devices and with a rated power of 600 W, an input and output voltage of 100 V and 400 V, respectively. The performance comparison based on Si-MOSFET/Si-diode and SiC-JFET/SiC-Schottky power devices as shown in Table 2.16.

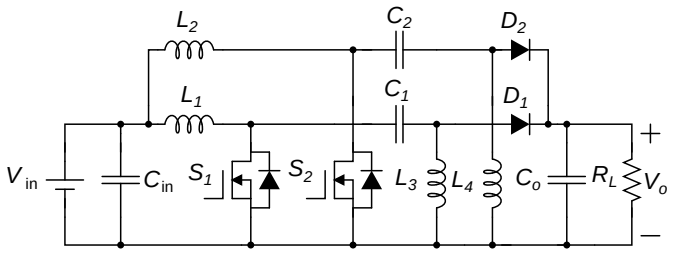


Figure 2.30: Interleaved DC-DC SEPIC converter based on SiC-cascode power devices (Alharbi et al. 2018).

Table 2.16: Performance comparison based on Si-MOSFET/Si-diode and SiC-JFET/SiC-Schottky diode power devices (Alharbi et al. 2018).

Parameters	Si-MOSFET/Si-diode (R6535ENZI)	SiC-JFET/SiC-Schottky diode (UJC06505K)
Blocking voltage (V)	650	650
Rated current (A) at $T_j = 25°C$	35	36.5
Maximum junction temparature (°C)	150	150
Drain-source on-resistance ($R_{DS,on}$) at $T_j = 25°C$	98 mΩ	34 mΩ
Gate resistance (Ω) at $T_j = 25°C$	10	20
Gate-source voltage during turn-on and turn-off (V)	+20 and -20	+12 and 0
Switching energy losses during turn-on and turn-off (μJ)	102.5 and 165.7	130.8 and 43.2
Power loss (W) at $T_j = 25°C$	14.6	10.4
Overall efficiency (%) at $f_{sw} = 50$ kHz, and $V_{in} = 100$ V	95	97.5

2.4.11 SiC based isolated bidirectional DC-DC converter

During recent progress development in the area of semiconductor devices, the SiC MOSFET has attracted growing attention. In comparison to traditional Si MOSFETs, the SiC MOSFET has a high blocking voltage capability, low on-state resistance, and short turn-on/turn-off times. A SiC-based 1200 V/110 V isolated bidirectional DC-DC converter topology is shown in Figure 2.31 (Wang, Zhang, Wang, Yang, Fu & Zha 2019). In this converter, three-level FB structure is used on the primary side, which can make the switching device tolerate half of the input voltage. A full wave rectifier is used on the secondary side, which can reduce the loss and ensure the bidirectional flow of the system. In order to avoid switching overlap within the primary side of the converter, a dead-band time is fixed between S_1 and S_3, S_2 and S_4, S_5 and S_7, and S_6 and S_8 switches. While the switching pulses of the secondary side adopt a synchronous rectification approach (Wang, Zhang, Wang, Yang, Fu & Zha 2019).

2.5 Design Recommendation and Future Trends

To enable the development of a high-efficiency power supply on-chip, a number of research challenges need to be overcome, as follows:

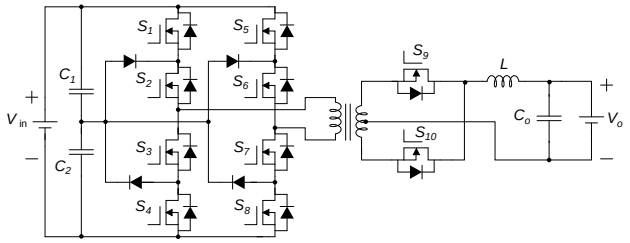


Figure 2.31: SiC based isolated bidirectional DC-DC converter (Wang, Zhang, Wang, Yang, Fu & Zha 2019).

2.5.1 Inaccurate switching models

Proper switching models that incorporate quiescent bias and frequency-dependent trap models need to be developed for proper simulation and design work. The characterization for the modeling needs to be carried out using pulsed IV techniques. One of the major challenges with design in a GaN process is the devices are D-Mode n-type. The lack of p-type devices makes the design of complex logic circuits challenging. Hence, the design of complex analog circuitry is challenging; however, circuit design approaches that have already been developed in GaAs designs can be applied.

2.5.2 Optimisation of the power switch

A significant criterion for evaluating the quality of a power device is thermal performance in end-system applications. It is well known that thermal problems severely constrain converter performance requirements, such as ripple and harmonic distortion. The problem is exacerbated when operating at a high switching speed and higher output power levels. In order to design HF, high-efficiency and high-voltage power switches' accurate circuit and thermal modeling are needed since the proper sizing of source–drain metallization is critical. The layout with proper thermal vias to extract the generated heat away from the chip surface must also be modeled. This modeling is critical for accurate estimation of the quality of a power device, as excessive heating can severely limit the overall performance of the integrated converter in terms of output ripple, harmonic distortion, and so on. The problem is further exacerbated when operating at high switching speed and high output power levels

and the need for special cooling mechanisms to limit chip heating (Qian et al. 2018, Guo et al. 2019).

2.5.3 Co-design of mixed signal circuits and custom design flows

The design of mixed-signal circuits in GaN is very challenging since most of the circuits designed are tailored toward RF or for power switching. There is a significant knowledge gap in how the circuits interact due to spikes that may be caused by the high-voltage switching. A combination of schematic design, mixed-signal simulation, layout, and layout extraction (dc, RF, time domain, and EM) analysis will have to be combined to fully understand all the forces at play within the codesign environment.

2.5.4 Optimisation of control circuits

One of the major challenges in implementing mixed-signal control circuits and high-voltage switches is the feature size and transconductance temperature dependence of the transistor. High-voltage devices usually have larger peripheries, hence drawing more current through them, while digital circuits work with minimal drain currents; hence, proper sizing of both analog and digital circuits needs to be fully investigated.

2.5.5 Integration of high-voltage GaN with logic functionalities

The physical integration of mixed-signal circuitry with high-voltage power switches needs to be carefully examined. The layout must have separate probe points to independently test the separate logic functions without interfering with each other. Moreover, the on-chip thermal distribution profile must be modeled with all the functionalities operating within the same substrate and environment to give an understanding of the packaging requirements and thermal hotspots.

2.5.6 Testing and packaging

The fabricated structures need to be initially tested on-wafer to determine the yield within the die and then diced for packaging. The on-wafer test will include functional

testing of all the mixed-signal circuitry and the high-voltage switch. The diced chips can be placed onto a high thermal conductivity carrier substrate and glued onto a package, which can be ceramic, metal, or plastic. Measurements can then be conducted to optimize the devices to minimize parasitics from the bonding wires and leads that form part of the chip interface to the external world. The packaged chipset can be measured for its performance and compared to simulated results. Test and measurement setups will be similar to an on-wafer setup, except that the chip is mounted on a prototype PCB with good thermal conductivity to draw the heat away from thermal bottlenecks.

2.6 Summary

Notably DC-DC converter topologies are commonly used in renewable energy, high-voltage direct current (HVDC), medium-voltage direct current (MVDC), aerospace, automobile, and many other systems. This chapter presented an overview of classical and recent development in power DC-DC converter topologies based on WBG semiconductor devices. The properties of WBG devices motivate a new generation of high efficiency converters in applications where classical power converters present significant limitations; such as, high voltage, high temperature and high frequency operation.

In addition, WBG devices with suitable circuit topologies are ideal for high power high density mobile applications such as aerospace, and EVs. The outstanding performance of HEMTs fabricated on GaN heterostructures have emerged in the last decade. The two dimensional electron gas (2DEG) together with high electron mobility make these structures more attractive for high switching frequency applications. It can be concluded that advances in GaN based DC-DC converters present promising solutions for obtaining high efficiency at higher switching frequencies with low power loss due to high carrier mobility in the 2DEG channel and associated parasitic in these devices.

Chapter 3

GaN-Based High-Frequency High-Voltage Gain DC-DC Converter

The conventional boost converter based on the Cockcroft-Walton (CW) voltage multiplier provides a high voltage gain at cost of extremely high duty cycle (Young et al. 2012). The main drawback is the presence of a high output voltage ripple when low switching frequency is used.

In this chapter, a high frequency high voltage gain GaN-based transformerless DC-DC boost converter with a voltage-lift switched-inductor circuit based on a CW voltage multiplier is proposed.

Most of this chapter contents have been submitted to the IEEE Access.

1. **M. Parvez,** A. T. Pereira, N. H. E. Weste, D. Abbott, and S. F. Al-Sarawi. GaN-Based High-Frequency High-Voltage Gain Non-Isolated Transformerless DC-DC Boost Converter with voltage-lift switched-inductor circuit. In *IEEE Access*, Submitted.

3.1 Introduction

Recently, wide band gap (WBG) semiconductor materials have been introduced in the power semiconductor market. Among several WBG devices, silicon carbide (SiC) and gallium nitrate (GaN) devices seems to attract more attention because

of their outstanding material features with respect to Si devices (Millan et al. 2014, Kaminski & Hilt 2014, Ramachandran & Nymand 2015, Mitova et al. 2013). Several studies on SiC power devices are widely recognized in the recent literature (Inoue & Akagi 2007, Boutros et al. 2009). On the other hand, there are only a few studies on GaN devices for high power converters (kW converters) (Das et al. 2011, Huang et al. 2016, Zulauf et al. 2018).

Devices based on GaN technology have a high frequency dielectric constant of 5.3 versus almost 12 for either silicon or GaAs. This lower dielectric constant will translate into lower intrinsic interterminal capacitances, which will provide a significant reduction in degenerate RF feedback for GaN based transistors as compared to similar silicon or GaAs based structures. In addition, GaN as a material, has an inherent breakdown field strength that is roughly 10 times that of silicon or GaAs. Thus, for equivalent silicon or GaAs devices a gallium nitride high electron mobility transistor (GaN HEMT) requires only one tenth of the physical distance in the drain region to obtain the same breakdown (Boles 2018).

In the last decades, the advantages of the broadly used conventional CW network are high voltage step-up ratio, lower voltage stresses on capacitors and diodes, reduced size and cost. Therefore, the CW multiplier is commonly used in several high step-up DC applications. A four-switch CW multiplier cell based DC-DC converter has been implemented by Young et al. (2012) that offers high voltage gain without using a high frequency transformer (Amir et al. 2018). Furthermore, the voltage stresses on switches, diodes, and capacitors are lower, and also independent of the number of cascaded stages. Nonetheless, the high switching losses due to the lack of soft switching, i.e., the lower efficiency and large boost inductor size make this topology unpopular.

To overcome these problems, a high frequency high voltage gain nonisolated transformer less DC-DC boost converter with a voltage-lift switched-inductor circuit based on a CW voltage multiplier is proposed in this chapter. The proposed converter uses GaN based integrated circuits that are suitable for downstream applications including automotive and photovoltaic solar panel technologies as shown in Figure 3.1.

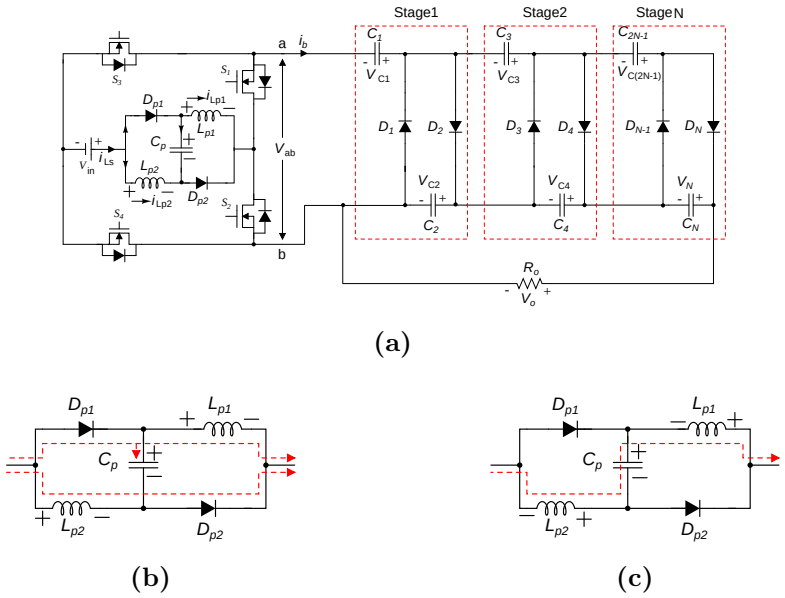


Figure 3.1: (a) Proposed converter topology using voltage-lift switched-inductor; (b) Voltage-lift switched-inductor cell during ON state; (c) Voltage-lift switched-inductor cell during OFF state.

GaN-based DC-DC converters are promising semiconductor devices for high switching frequency and high efficiency applications compared to well-known silicon devices. The GaN-based converter permits the increase of high switching frequency, high efficiency and high voltage gain due to their small switching losses. The control strategy is improved to allow high switching frequency up to the megahertz (MHz) range and to minimize the output voltage ripple. The proposed converter is demonstrated through the design of a 420 W high voltage gain high efficiency DC-DC boost and is validated through simulation and compared to published converters in the literature.

3.2 Converter Analysis and Operating Principle

Before presenting the proposed topology analysis, it is worth noting that the following:

- All of the circuit parasitic elements are considered in order to analyze the power dissipation.

- At higher switching frequency, alternating current is flowing into the CW voltage multiplier through the voltage-lift switched-inductor cell, and all capacitors are sufficiently large. Therefore the voltages across all capacitors of the CW voltage multiplier are the same, except for the first capacitor.
- The proposed converter operates in continuous current mode (CCM) with steady-state operation.
- Only one diode within the CW voltage multipler conducts during the input voltage-lift switched-inductors L_{p1} and L_{p2} transfer of storage energy.

3.2.1 Operating principle

The operating modes of proposed converter topology consists of one voltage-lift switched inductor cell as shown in Figure 3.2, where both inductors L_{p1} and L_{p2} have considered the same value. The both inductors are charged and discharged in parallel by input voltage V_{in} during switching ON and OFF state, respectively. The full-bridge (FB) converter GaN switches S_1 & S_2 are operated by at low switching frequency (e.g. 10 kHz), f_{sw} while S_3 and S_4 are operated by at higher operating frequency—a modulating frequency (e.g. 6 MHz), f_{mo}. In this topology, the switches $S_1(S_4)$ and $S_2(S_3)$ operate in a complementary mode, and the switching frequency f_{sw} is tuned to obtain the desired output voltage ripple, f_{mo} is tuned to operate at higher than f_{sw} and the output voltage is regulated by controlling the f_{sw} or f_{mo} signal duty cycle. The duty cycle, D, of each switch is targeted at 50% to avoid cross conduction and associated losses during switching. The voltage gain of the converter depends on the number of stages and duty cycle of the modulating switches.

3.2.2 Operating modes based on 2-stage CW-voltage multiplier

There are six operating modes for a FB converter based on a 2-stage CW-voltage multiplier in continuous current mode (CCM). With regard to the controlling waveforms of the proposed converter, the operation of the converter can be divided into two intervals namely even and odd intervals. During the even interval, only even numbered diodes (D_2, D_4) are conducting. On the other hand, during the odd interval, only the odd numbered diodes (D_1, D_3) are conducting.

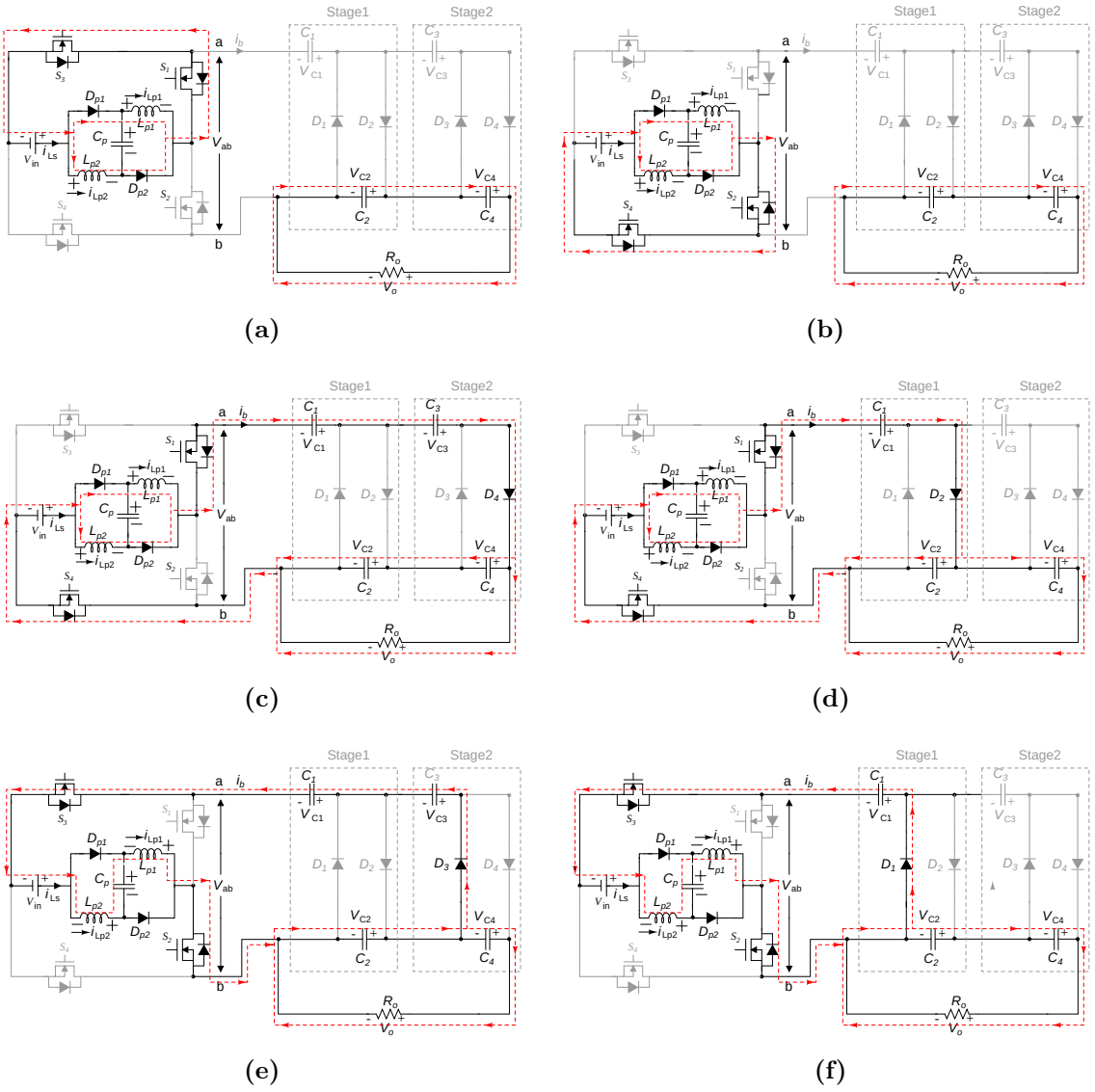


Figure 3.2: Operating modes of proposed converter (a) Mode I; (b) Mode II; (c) Mode III; (d) Mode IV; (e) Mode V; and (f) Mode V.

Figure 3.3 shows the theoretical steady-state operational waveforms of the proposed converter including switching signals, inductor current, FB output voltage, output current, capacitors voltage and diode current.

- *Mode I & II* : Switches S_1 and S_3 are closed, and S_2 and S_4 are open, and all diodes of voltage multiplier are open, the input voltage-lift switched-inductors L_{p1} and L_{p2} are charged by the input dc supply, as shown in Figure 3.2 (a). By this configuration, even capacitors C_2 and C_4 supply to the load, and odd

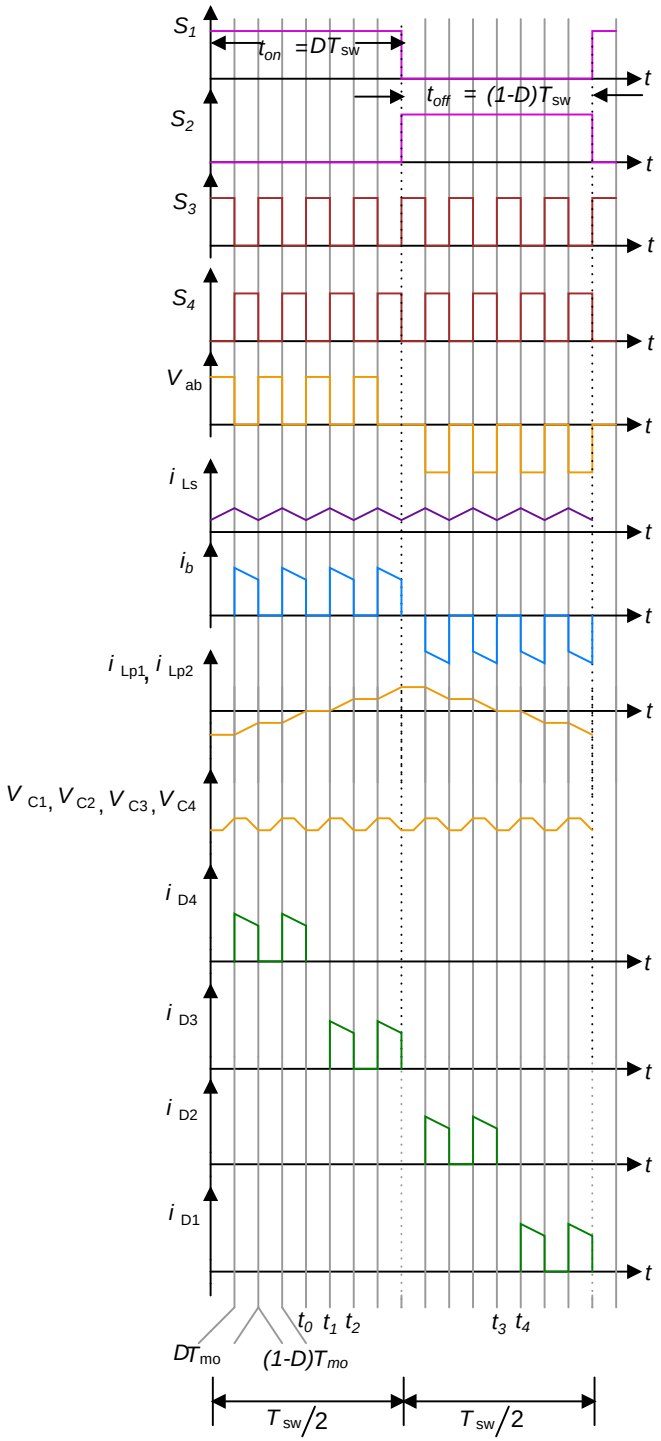


Figure 3.3: Steady-state waveforms of the proposed converter.

capacitors C_1 and C_3 are floating. Similarly, from Figure 3.2 (b), when switches

S_2 and S_4 are closed and S_1 and S_3 are open, the input voltage-lift switched-inductors L_{p1} and L_{p2} are charged by the input supply, the even capacitors of voltage multiplier supply to the load and odd capacitors are floating.

- *Mode III to VI* : Switches S_1 and S_4 are closed, and S_2 and S_3 are open, the FB output current i_b flows foward into the voltage-lift switched inductors L_{p1}, and L_{p2}. The dc source energy transfer to the load is through the even diodes D_2 and D_4, thus the parallel capacitor C_p, even capacitors C_2 and C_4 are charged, and odd capacitors C_1 and C_3 are discharged by the FB output current i_b, as shown in Figure 3.2 (c) & 3.2 (d). Similarly, when switches S_2 and S_3 are closed, and S_1 and S_4 are open, the FB output current i_b is flowing out of the voltage-lift switched inductors L_{p1}, and L_{p2}. The dc source energy transfer to the voltage multiplier is through the odd diodes D_1 and D_3, thus the odd capacitors C_1 and C_3 are charged, and the capacitor C_p, even capacitors C_2 and C_4 are discharged by the FB output current i_b, as shown in Figure 3.2 (e) & 3.2 (f).

3.2.3 Boost converter stage

According to the continuous conduction modes for the energy storage inductors L_{p1}, and L_{p2} the average inductors voltage can be defined by

$$v_{\mathrm{Lp1,2}} = L_{p1,2}\frac{di_{\mathrm{Lp1,2}}}{dt} = V_{\mathrm{in}} - (d_{\mathrm{sw}} - d_{\mathrm{mo}}) \cdot V_{\mathrm{ab}} \ , \tag{3.1}$$

where d_{sw} and d_{mo} are the converter's conduction states when the switches are operated by f_{sw} and f_{mo}, respectively, V_{in} is the input voltage, i_{Lp1} and i_{Lp2} are the voltage-lift switched-inductors current and V_{ab} is the output voltage of the full-bridge (FB) converter. The Equation (3.1) can be rewritten as,

$$V_{\mathrm{ab}} = \frac{1}{d_{\mathrm{sw}} - d_{\mathrm{mo}}} V_{\mathrm{in}} \ , \tag{3.2}$$

The FB output current i_b flowing into the voltage-lift switched-inductor cell depends on d_{sw} and d_{mo} conduction states and can be expresses by,

$$\frac{i_b}{i_{\mathrm{Ls}}} = (d_{\mathrm{sw}} - d_{\mathrm{mo}}), \tag{3.3}$$

where i_{Ls} is the input current flowing into the voltage-lift switched-inductor cell.

3.2.4 Voltage gain and inductor current analysis

In the operating modes I and II as depicted in Figure 3.2 (a) & 3.2 (b), respectively. Therefore, according to the ideal wave shapes in Figure 3.3, during time interval $t_0 < t < t_1$, the input inductor current is circulating to the voltage-lift switched-inductor cell. The input current can be expressed during this interval,

$$i_{\mathrm{Ls}}(t_1 - t_0) = \frac{V_{\mathrm{in}}}{L_{p1,2}}(t_1 - t_0). \tag{3.4}$$

Regarding the operating modes III and IV, the voltage across the CW terminal, $V_{\mathrm{ab}} = V_o/2N$. Where, N is the cascade voltage multiplier stage, and $V_o/2$ is that the other half over C_1. Then, during the interval $t_1 < t < t_2$, the input current can be defined by,

$$i_{\mathrm{Ls}}(t_2 - t_1) = \frac{V_{\mathrm{in}} - \frac{V_o}{2N}}{L_{p1,2}}(t_2 - t_1). \tag{3.5}$$

The currents i_{Lp1} and i_{Lp2} only flows through the parallel inductors L_{p1} and L_{p2} during six operating modes from I to VI as shown in Figure 3.2. The operating time interval can be observed from Figure 3.3, i_{Lp1} and i_{Lp2} are starts from time interval t_0 to t_3 (through t_1) is considered as the first half cycle, and t_3 to t_0 (through t_2) is considered as the second half cycle. For mode I in Figure 3.2 (a), the parallel inductor current i_{Lp1} and i_{Lp2} can be defined during time interval $t_0 < t < t_1$,

$$i_{\mathrm{Lp1}}(t_1 - t_0) = \frac{1}{L_{p1}} \int_{t_0}^{t_1} V_{\mathrm{Lp1}}\, dt\cdot \tag{3.6}$$

$$i_{\mathrm{Lp2}}(t_3 - t_2) = \frac{1}{L_{p2}} \int_{t_2}^{t_3} V_{\mathrm{Lp2}}\, dt\cdot \tag{3.7}$$

For modes III and IV in Figure 3.2 (c) & 3.2 (d), the parallel inductor current i_{Lp1} and i_{Lp2} can be expressed during the time interval $t_1 < t < t_2$,

$$\begin{aligned} i_{\mathrm{Lp1}}(t_2 - t_1) &= \frac{1}{L_{p1}} \int_{t_1}^{t_2} V_{\mathrm{Lp1}}\, dt \\ &= \frac{1}{L_{p1}} \int_{t_1}^{t_2} (V_{\mathrm{in}} - V_{\mathrm{ab}})\, dt = \frac{V_{\mathrm{in}} - \frac{V_o}{2N}}{L_{p1}} (t_2 - t_1)\,, \end{aligned} \tag{3.8}$$

$$\begin{aligned} i_{\mathrm{Lp2}}(t_2 - t_1) &= \frac{1}{L_{p2}} \int_{t_1}^{t_2} V_{\mathrm{Lp2}}\, dt \\ &= \frac{1}{L_{p2}} \int_{t_1}^{t_2} (V_{\mathrm{in}} - V_{\mathrm{ab}})\, dt = \frac{V_{\mathrm{in}} - \frac{V_o}{2N}}{L_{p2}} (t_2 - t_1)\,, \end{aligned} \tag{3.9}$$

where V_{Lp1} and V_{Lp2} are the parallel inductor voltage. Similarly as modes II and II in Figure 3.2 (b), the parallel inductors current i_{Lp1} and i_{Lp2} can be expressed during time interval $t_2 < t < t_3$,

$$i_{\mathrm{Lp1}}(t_3 - t_2) = \frac{1}{L_{p1}} \int_{t_2}^{t_3} V_{\mathrm{Lp1}}\, dt\cdot \tag{3.10}$$

$$i_{\mathrm{Lp2}}(t_3 - t_2) = \frac{1}{L_{p2}} \int_{t_2}^{t_3} V_{\mathrm{Lp2}}\, dt\cdot \tag{3.11}$$

For modes V and VI in Figure 3.2 (e) & 3.2 (f), the parallel inductor current i_{Lp1} and i_{Lp1} can be obtained during time interval $t_3 < t < t_0$,

$$\begin{aligned} i_{\mathrm{Lp1}}(t_0 - t_3) &= \frac{1}{L_{p1}} \int_{t_3}^{t_0} V_{\mathrm{Lp1}}\, dt \\ &= \frac{1}{L_{p1}} \int_{t_3}^{t_0} (V_{\mathrm{ab}} - V_{\mathrm{in}})\, dt = \frac{V_{\mathrm{ab}} - V_{\mathrm{in}}}{L_{p1}} (t_0 - t_3)\cdot \end{aligned} \tag{3.12}$$

$$\begin{aligned} i_{\mathrm{Lp2}}(t_0 - t_3) &= \frac{1}{L_{p2}} \int_{t_3}^{t_0} V_{\mathrm{Lp2}}\, dt \\ &= \frac{1}{L_{p2}} \int_{t_3}^{t_0} (V_{\mathrm{ab}} - V_{\mathrm{in}})\, dt = \frac{V_{\mathrm{ab}} - V_{\mathrm{in}}}{L_{p2}} (t_0 - t_3)\cdot \end{aligned} \tag{3.13}$$

It can be observed from Figure 3.3, the time intervals $(t_0 - t_1)$ and $(t_1 - t_2)$ are similar to the intervals DT_{mo} and $(1-D)T_{\mathrm{mo}}$, respectively. Therefore, putting DT_{mo} and $(1-D)T_{\mathrm{mo}}$ in Eqns. (3.4) and (3.5), and then applying the volt-second balance principle to the boost inductor, the voltage gain of the proposed converter can be obtained as,

$$G_v = \frac{V_0}{V_{\mathrm{in}}} = 2\gamma N, \tag{3.14}$$

where $\gamma = (1 + D)/(1 - D)$, and the output voltage V_o is regulated by controlling the duty cycle D of switches S_3 and S_4 in the positive and negative conducting interval during the modulating switching period $f_{\mathrm{mo}} = 1/T_{\mathrm{mo}}$. The relationship between voltage gain and duty cycle for proposed converter for $N = 1$ to 6 and also compared with conventional boost converter as shown in Figure 3.4. It can bee seen from Figure 3.4, the voltage gain is higher in compression to a conventional boost converter.

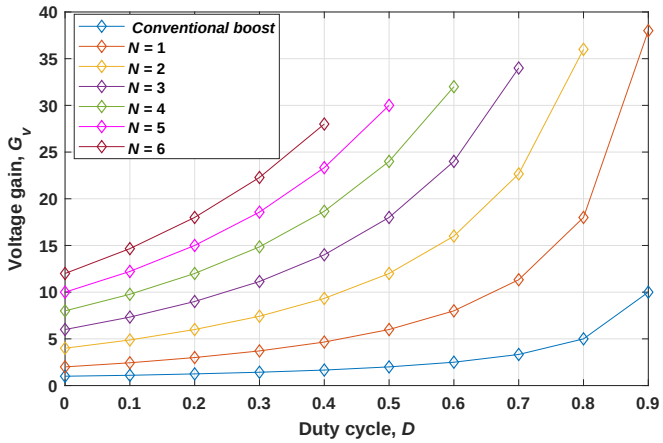


Figure 3.4: Relationship between voltage gain and duty cycle for the proposed converter from $N = 1$ to 6 in comparison to conventional DC-DC boost converter.

3.3 Design Consideration

In order to obtain realistic results of the proposed converter, the values of the parasitic elements are selected based on actual components. Both GaN switch TPH3006PS with ($R_{\mathrm{DS_{ON}}} = 0.15\ \Omega$) are from Transphorm company. The transistor diode model IDH04G65C6 ($V_F = 1.25$ V) is from Infineon technologies.

3.3.1 Input boost inductor

The input voltage-lift switched inductors are a significant design components which permits high voltage gain and lower ripple current of proposed converter. To decrease the inductor size and avoid higher cost, it should be selected in such a way that ripple current is at a minimum. For a 420 W system, the maximum input voltage is considered as the decrease in duty cycle increases the current ripple. The input voltage-lift switched-inductor L_{p1} and L_{p2} are added to obtain high voltage gain and reduce the input current ripple. Using a maximum peak to peak output full-bridge current of $i_{b,\mathrm{max(p\text{-}p)}} = 10$ A, the percentage of the maximum peak to peak ripple current in the voltage-lift switched-inductor $\delta_i = 0.41\%$ and modulating frequency $T_{\mathrm{mo}} = 1/f_{\mathrm{mo}} = 0.16$ µs into (3.15) (Young et al. 2012, Amir et al. 2018) a input voltage-lift switched-inductor value equal to $L_{p1} = L_{p2} = 100$ µH is found using,

$$L_{p1} = L_{p1} = \frac{V_{\mathrm{in}} D}{\delta_i f_{\mathrm{mo}}\ i_{\mathrm{Ls.(p\text{-}p)}}}\ . \tag{3.15}$$

Figure 3.5 (a) represents the voltage-lift switched inductance versus input ripple current at the constant modulating frequency, $f_{\mathrm{mo}} = 6$ MHz and for a duty cycle range from $D = 0.1$ to 0.9. When the duty cycle is kept at 50%, i.e $D = 0.5$, and varying the modulating frequency f_{mo} from 1 MHz to 10 MHz, the responses of input inductance and input ripple current are shown in Figure 3.5 (b).

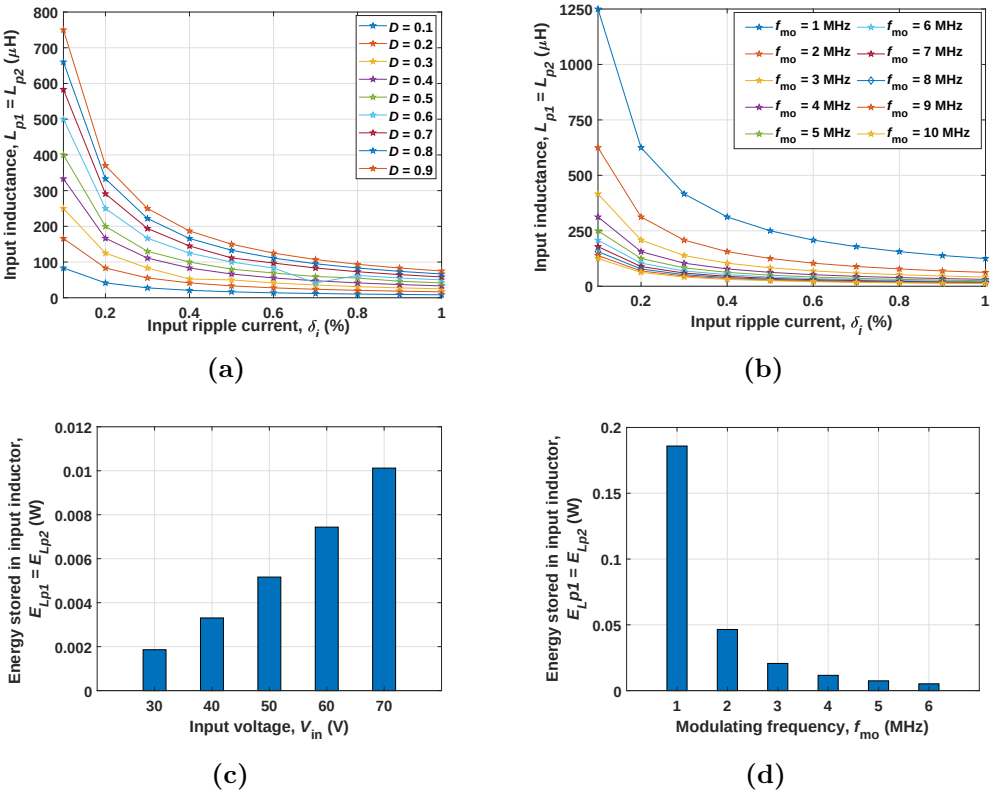


Figure 3.5: (a) The input voltage-lift switched inductance versus input ripple current with change in duty cycle; (b) Input voltage-lift switched inductance versus input ripple current with change in modulating frequency; (c) Energy stored in input voltage-lift switched inductor at different input voltage levels; and (d) Energy stored in input voltage-lift switched inductor at different modulating frequencies.

The maximum energy stored in the input voltage-lift switched-inductor can be calculated by (3.16), where the Figures 3.5 (c) and 3.5 (d) graphically represented energy stored in input voltage-lift switched-inductor at different input voltage level and at different modulating frequencies, respectively. It can be seen from Figure 3.5 (c), the energy stored in the input voltage-lift switched-inductor, E_{Lp1} and E_{Lp2} increases due to an increase in the input voltage level, V_{in}. On the other hand it can be seen

from Figure 3.5 (d), E_{Lp1} and E_{Lp1} decreases when the modulating frequency, f_{mo} is increased. Note high modulating frequency used to reduce the size of inductor. For the proposed converter, the number of stages $N = 2$, and V_{in} should be within 30 V to 50 V.

$$\begin{aligned} E_{\mathrm{Lp1}} &= E_{\mathrm{Lp2}} \\ &= \frac{1}{2} L_p i^2_{\mathrm{Ls.(p\text{-}p)}} = \frac{1}{2} L_p i^2_{\mathrm{Ls.(p\text{-}p)}} \ . \end{aligned} \tag{3.16}$$

Equation (3.16) can be rearranged by using (3.15),

$$\begin{aligned} E_{\mathrm{Lp1}} &= E_{\mathrm{Lp1}} \\ &= \frac{1}{2} L_{p1} \left(\frac{V_{\mathrm{in}} D}{\delta_i f_{\mathrm{mo}}\ L_{\mathrm{p1}}} \right)^2 = \frac{1}{2} L_{p2} \left(\frac{V_{\mathrm{in}} D}{\delta_i f_{\mathrm{mo}}\ L_{\mathrm{p2}}} \right)^2 \ . \end{aligned} \tag{3.17}$$

3.3.2 Capacitors of CW voltage multiplier

The proposed converter can be extended for N stage cascade voltage multiplier as shown in Figure 3.1. According to the aforementioned second assumption, the capacitor voltage in cascade stage can be measureed as:

$$V_{ci} = \begin{cases} \frac{V_c}{2}, \ \text{for } i = 1 \\ V_c, \ \text{for } i = 2, 3, \cdots, N \end{cases} \tag{3.18}$$

where V_{ci} is the ith capacitor of cascade stage, and V_c is the steady-state voltage across all capacitor in cascade stage except the first capacitor. It is noted that from Figure 3.1, the output voltage V_o, is equal to the summation of all even capacitors voltage and can be defined as:

$$V_o = N V_c \ . \tag{3.19}$$

Putting (3.19) into (3.18), the steady-state voltage of each capacitor for N stage cascade network can be expressed as:

$$V_{ci} = \begin{cases} \frac{V_0}{2N}, \ \text{for } i = 1 \\ \frac{V_0}{N}, \ \text{for } i = 2, 3, \cdots, N. \end{cases} \tag{3.20}$$

The capacitors of the CW voltage multiplier are designed to limit the output voltage ripple. The following Equation (3.21) can be used to obtain the capacitors values of

CW voltage multiplier to achieve the desired output voltage ripple

$$\delta V_{C_i} = \frac{I_o \; N^2}{2 f_{\text{sw}} \; C_i} \; , \tag{3.21}$$

where δV_{Ci} denotes the voltage ripple across the CW voltage multiplier capacitors. It is clear from (3.21), the ripple voltage is function of the multiplier capacitance value, the relation is between them is plotted in Figure 3.6. Therefore, four film capacitors are obtained as the capacitors C_1, C_2, C_3 and C_4 with capacitance 50 µF.

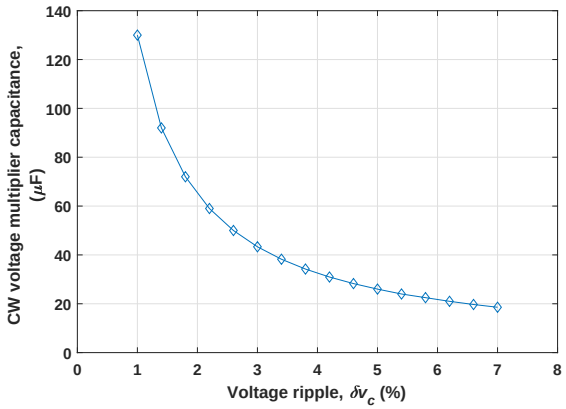


Figure 3.6: CW voltage multiplier capacitance changes with the change in voltage ripple.

3.3.3 Voltage stress of each capacitor in CW voltage multiplier

According to the second assumption in CW voltage multiplier, the voltage across the first capacitor is one-half of the other capacitors at the same input voltage level. The maximum voltage stress in the proposed converter depends on the switching of duty cycle ($D = 0.5$), and input voltage, and number of stages needed to achieve the required output voltage.

From equations (3.14) and (3.20), the maximum voltage stress of each capacitor can be calculated by:

$$V_{ci} = \begin{cases} \gamma V_{\text{in}}, \;\; \text{for } i = 1 \\ 2\gamma V_{\text{in}}, \;\; \text{for } i = 2, 3, \cdots, N. \end{cases} \tag{3.22}$$

The voltage stress on each capacitor in CW voltage multiplier for proposed converter as function on the input voltage value is shown in Figure 3.7.

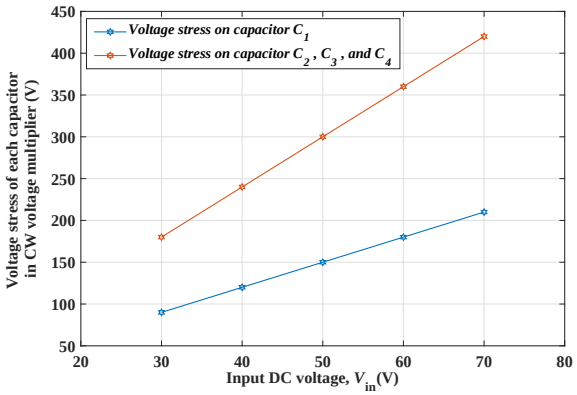


Figure 3.7: Votage stresses of each capacitor in CW voltage multiplier at several input voltage level, when $D = 0.5$.

The capacitor energy stored can be calculated by:

$$E_{ci} = \frac{1}{2} C_i V_{ci}^2. \tag{3.23}$$

Putting (3.20) and (3.21) into (3.23), the energy stored in capacitor of CW voltage multiplier can be defined by:

$$E_{ci} = \frac{1}{4} \frac{I_o \; N^2}{\delta V_{C_i} f_{\text{sw}} \; C_i} \begin{cases} \gamma^2 V_{\text{in}}^2, & \text{for } i = 1 \\ 4\gamma^2 V_{\text{in}}^2, & \text{for } i = 2, 3, \cdots, N. \end{cases} \tag{3.24}$$

3.3.4 Voltage ripple analysis of capacitors

The total voltage ripple of parallel capacitor C_p is denoted by (δV_{C_p}). The voltage ripple on capacitor C_p generated due to current flowing through the equivalent series resistance (ESR) $(\delta V_{C_{p,\text{ESR}}})$ is defined by:

$$\begin{aligned} \delta V_{C_{p,\text{ESR}}} &= r_{C_p} \delta i_{C_p} \\ &= r_{C_p} (i_{C_{p,\text{charge}}} - i_{C_{p,\text{discharge}}}) = 2\gamma N r_{C_p} I_o \; . \end{aligned} \tag{3.25}$$

The voltage ripple on capacitor C_p generated due to charging $(\delta V_{Cp,\text{charge}})$ can be obtained by:

$$\delta V_{C_{p,\text{charge}}} = \frac{i_{C_{p,\text{charge}}} D}{C_p f_{\text{sw}}} \; . \tag{3.26}$$

Hence, the total voltage ripple of parallel capacitor δV_{Cp} can be expressed by:

$$\delta V_{C_p} = \delta V_{C_{p,\text{ESR}}} + \delta V_{C_{p,\text{charge}}} = 2\gamma N r_{C_p} I_o + \frac{i_{C_{p,\text{charge}}} D}{C_p f_{\text{sw}}} \; . \tag{3.27}$$

The voltage ripple of CW voltage multiplier capacitors C_1, C_2, C_3 and C_4 ($\delta V_{C_{1,2,3,4}}$) can be obtained using

$$\delta V_{C_{1,2,3,4}} = \frac{I_o\ N^2}{2 f_{\rm sw}\ C_{1,2,3,4}}\ . \tag{3.28}$$

3.3.5 Efficiency analysis

For efficiency analysis of converter, parasitic resistive elements have also been considered as follows: $R_{\rm ON}$ is the switch ON-state resistance, $R_{\rm FD1}$, $R_{\rm FD2}$, $R_{\rm FD3}$, $R_{\rm FD4}$, $R_{\rm FDp1}$ and $R_{\rm FDp2}$ are the forward diode resistances of diodes D_1, D_2, D_3, D_4, D_{p1} and D_{p2} respectively, $V_{\rm TD1}$, $V_{\rm TD2}$, $V_{\rm TD3}$, $V_{\rm TD4}$, $V_{\rm TDp1}$ and $V_{\rm TDp2}$ are the threshold voltages of diodes D_1, D_2, D_3, D_4, D_{p1} and D_{p2} respectively. Note that $r_{\rm Lp1}$ and $r_{\rm Lp2}$ are the equivalent series resistance (ESR) of inductors L_{p1} and L_{p2}, respectively, $r_{\rm Cp}$, r_{C_1}, r_{C_2}, r_{C_3}, and r_{C_4}, are the ESR of capacitors C_p, C_1, C_2, C_3, and C_4, respectively. Figure 3.8 shows an equivalent circuit of proposed converter considering the highlighted parasitic elements correspons mode III in Figures 3.2 (c).

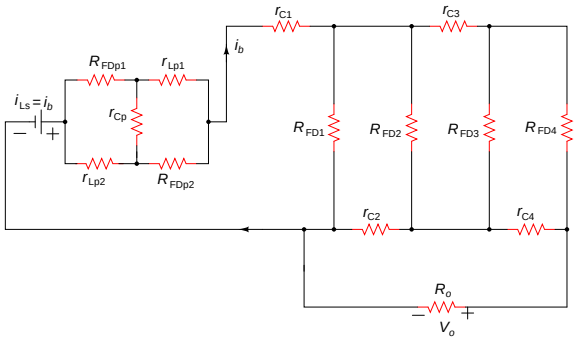


Figure 3.8: Equivalent circuit of proposed converter considering parasitic resistive elements.

The power dissipated ($P_{S_{1,2,3,4}}$) in switches S_1, S_2, S_3 and S_4 can be expressed as:

$$\begin{aligned} P_{S_{1,2,3,4}} &= 8 i_{b,\rm rms}^2 R_{\rm ON}\gamma N \\ &= 8\Big(\frac{I_o}{\sqrt{2}}\Big)^2 R_{\rm ON}\gamma N = 4\gamma N R_{\rm ON} I_o^2\ . \end{aligned} \tag{3.29}$$

The switching losses ($P_{\rm tsw}$) of $f_{\rm sw}$ and $f_{\rm mo}$ can be obtained by:

$$\begin{aligned} P_{\rm tsw} &= 2\gamma N C_S V_{\rm ab}^2 (S_{1,2} T_{\rm sw} + S_{3,4} T_{\rm mo}) \\ &= 2\gamma N C_S V_{\rm in}^2 (S_{1,2} T_{\rm sw} + S_{3,4} T_{\rm mo})\ . \end{aligned} \tag{3.30}$$

The power dissipated due to gate threshold voltage $P_{\mathrm{GS(th)}}$ of S_1, S_2, S_3 and S_4 can be expressed by:

$$P_{\mathrm{GS(th)}} = 4V_{\mathrm{GS(th)}} i_{b,\mathrm{rms}} = 4V_{\mathrm{GS(th)}}\Big(\frac{I_o}{\sqrt{2}}\Big) \ . \tag{3.31}$$

The total power dissipated in switches ($P_{\mathrm{TS}_{1,2,3,4}}$) can be expressed by:

$$\begin{aligned} P_{\mathrm{TS}_{1,2,3,4}} &= P_{S_{1,2,3,4}} + P_{\mathrm{tsw}} + P_{\mathrm{GS(th)}} = 4\gamma N R_{\mathrm{ON}} I_o^2 \\ &\quad + 2\gamma N C_S V_{\mathrm{in}}^2 (S_{1,2} T_{\mathrm{sw}} + S_{3,4} T_{\mathrm{mo}}) + 4V_{\mathrm{GS(th)}}\Big(\frac{I_o}{\sqrt{2}}\Big) \ . \end{aligned} \tag{3.32}$$

The power dissipated due to forward diodes resistance ($P_{\mathrm{FRD}_{1,2,3,4,p1,p2}}$) of D_1, D_2, D_3, D_4, D_{p1} and D_{p2} can be obtained by:

$$\begin{aligned} P_{\mathrm{FRD}_{1,2,3,4,p1,p2}} &= 12 i_{b,\mathrm{rms}}^2 R_{\mathrm{FD}_{1,2,3,4,p1,p2}} \gamma N \\ &= 12\Big(\frac{I_o}{\sqrt{2}}\Big)^2 R_{\mathrm{FD}} \gamma N = 6\gamma N R_{\mathrm{FD}} I_o^2 \ . \end{aligned} \tag{3.33}$$

Due to ESR of inductors L_{p1} and L_{p2}, the power dissipated in inductors ($P_{r_{L_{p1}}, r_{L_{p2}}}$) can be expressed by:

$$\begin{aligned} P_{r_{L_{p1}}, r_{L_{p2}}} &= 2\gamma N (r_{L_{p1}} i_{b,\mathrm{rms}}^2 + r_{L_{p2}} i_{b,\mathrm{rms}}^2) \\ &= 2\gamma N (r_{L_{p1}} + r_{L_{p2}})\Big(\frac{I_o}{\sqrt{2}}\Big)^2 = \gamma N (r_{L_{p1}} + r_{L_{p2}})\Big) I_o^2 \ . \end{aligned} \tag{3.34}$$

The power dissipated in capacitors C_p, C_1, C_2, C_3, and C_4 ($P_{r_{C_{p,1,2,3,4}}}$) due to ESR, is defined by:

$$\begin{aligned} P_{r_{C_{p,1,2,3,4}}} &= r_{C_{p,1,2,3,4}} i_{C_{p,1,2,3,4,\mathrm{rms}}}^2 2\gamma N \\ &= 10 r_C \Big(\frac{I_o}{\sqrt{2}}\Big)^2 \gamma N = 5\gamma N r_C I_o^2 \ . \end{aligned} \tag{3.35}$$

The total power dissipated (P_{diss}) of proposed converter is be defined by:

$$P_{\mathrm{diss}} = P_{\mathrm{TS}_{1,2,3,4}} + \sum_{n=1}^{6} P_{\mathrm{FRD}_n} + P_{r_{L_{p1}}, r_{L_{p2}}} + P_{r_{C_{p,1,2,3,4}}} \ . \tag{3.36}$$

For simplicity, the equation (3.36) can be represented by the following equations:

$$\begin{aligned} P_{\mathrm{diss}} &= 4\gamma N R_{\mathrm{ON}} I_o^2 + 2\gamma N C_S V_{\mathrm{in}}^2 (S_{1,2} T_{\mathrm{sw}} + S_{3,4} T_{\mathrm{mo}}) + 4V_{\mathrm{GS(th)}}\Big(\frac{I_o}{\sqrt{2}}\Big) \\ &\quad + 6\gamma N R_{\mathrm{FD}} I_o^2 + \gamma N (r_{L_{p1}} + r_{L_{p2}}) I_o^2 + 5\gamma N r_C I_o^2 \ , \end{aligned} \tag{3.37}$$

Table 3.1: GaN switch internal parameters.

Parameters	TPH3006PS (GaN)
Drain-source on-resistance, $R_{\mathrm{DS_{ON}}}$	0.15 Ω
Gate charge, Q	9.3 nC
Gate threshold voltage, $V_{\mathrm{GS(th)}}$	1.35 V
Internal diode resistance, R_D	0.01 Ω

$$P_{\mathrm{diss}} = \lambda_1 \gamma I_o^2 + \lambda_3 I_o + \lambda_2 I_o \ . \tag{3.38}$$

where

$$\lambda_1 = 2N(2R_{\mathrm{ON}} + 3R_{\mathrm{FD}}) + N(r_{L_s} + r_{L_p}) + 5Nr_C \ ,$$

$$\lambda_2 = (S_{1,2}T_{\mathrm{sw}} + S_{3,4}T_{\mathrm{mo}})2NC_S V_{\mathrm{in}}^2 \ ,$$

$$\lambda_3 = 2\sqrt{2}V_{\mathrm{GS(th)}} \ ,$$

The efficiency (η) of the proposed converter can be expressed by:

$$\eta = \frac{P_o}{P_o + P_{\mathrm{diss}}} = \frac{1}{1 + \frac{P_{\mathrm{diss}}}{P_o}} = \frac{1}{1 + \frac{\lambda_1}{R_o}\gamma + \frac{\lambda_2}{I_o^2 R_o}\gamma + \frac{\lambda_3}{I_o R_o}} \ . \tag{3.39}$$

3.4 Results and Discussion

To model the GaN switches using MATLAB tools, the internal features of existing MOSFETs in the Simulink library have been modified. The values of drain to source on resistance R_{ON}, gate threshold voltage $V_{\mathrm{GS(th)}}$, and internal diode resistance R_D are shown in Table 3.1, where the cascode structure for the GaN switches is shown in Figure 3.1 is considered for topology under implementation. A 420 W model of proposed converter is designed and simulated in MATLAB/Simulink and LT Spice software as shown in Figures 3.9 and 3.10, respectively. The specification of the proposed converter are listed in Table 3.2. According to the components in Table 3.2, the converter model based on MATLAB/Simulink is fully run for 0.2 s, where load resistance is fixed 1 kΩ.

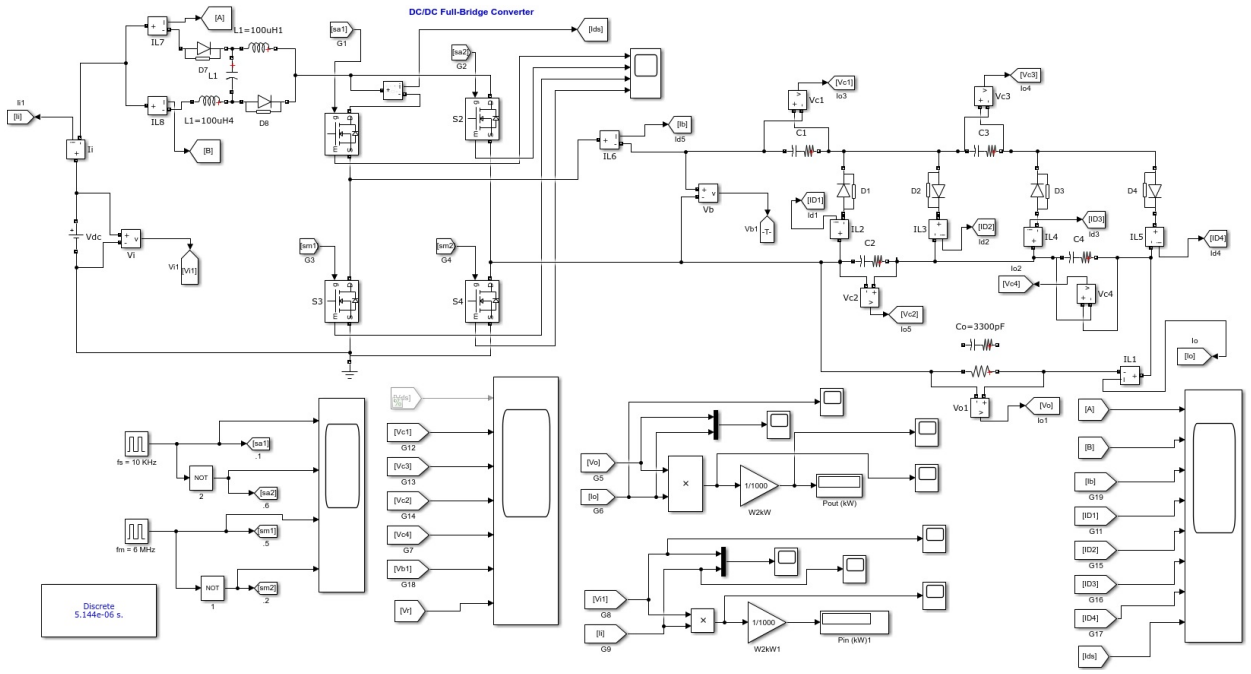


Figure 3.9: Simulink model of a high-frequency high-voltage gain nonisolated transformer-less DC-DC boost converter with voltage-lift switched inductor circuit.

The simulation results of proposed converter are shown in Figures 3.11 to 3.17. The waveforms of input current and power are shown in Figure 3.11 (a) and (b), respectively. Simulation results of full bridge output voltage and current are shown in Figure 3.12 (a) and (b), respectively. Figure 3.13 shows the simulation waveforms of voltage-lift switched inductor current. The CW voltage multiplier capacitors voltages across C_1 to C_4 are shown in Figure 3.14. The current through the CW voltage multiplier diodes D_1 to D_4 are shown in Figure 3.15.

The converter is connected with pure resistive load, where the output voltage and current are obtained 650 V and 0.65 A respectively, as shown in Figures 3.16 (a) and (b). It is shown that the transient response of voltage and current within 0 to 0.05 s, on the other hand from 0.05 s to 0.2 s, there is no overshoot and the steady-state position of voltage at 650 V and current at 0.65 A. The output power is achieved 410 W as shown in Figure 3.17 (a). The simulation efficiency vs output power curve of proposed converter is plotted in Figure 3.17 (b), where the highest efficiency was obtained is 98.23% at 50 V input voltage.

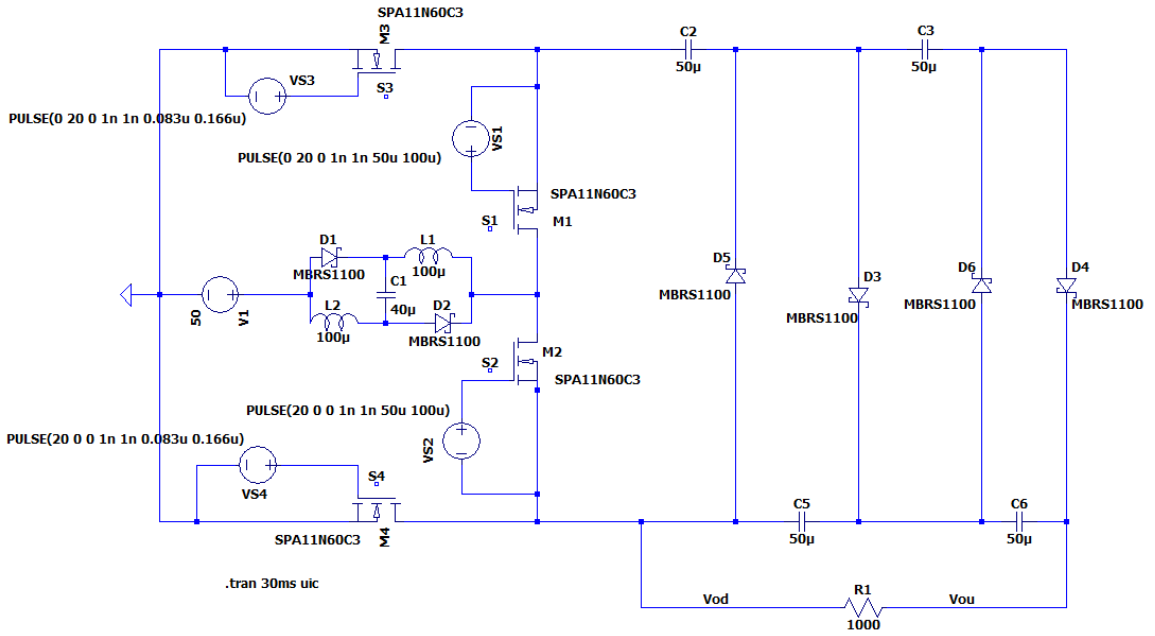
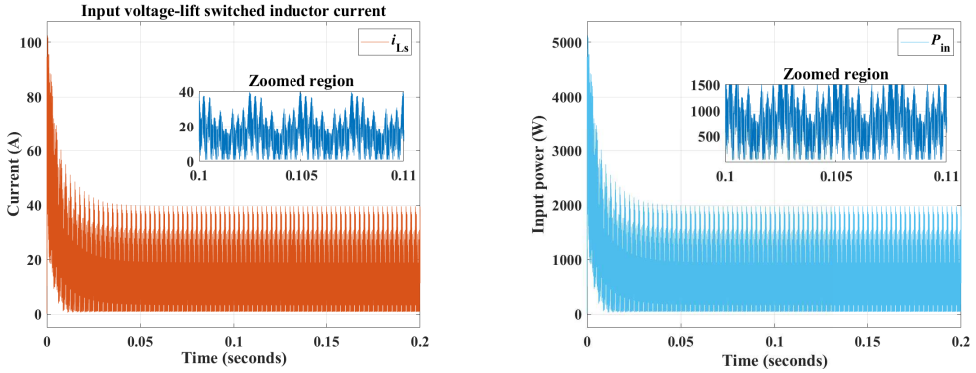


Figure 3.10: LTspice model of a high-frequency high-voltage gain nonisolated transformer-less DC-DC boost converter with voltage-lift switched inductor circuit.



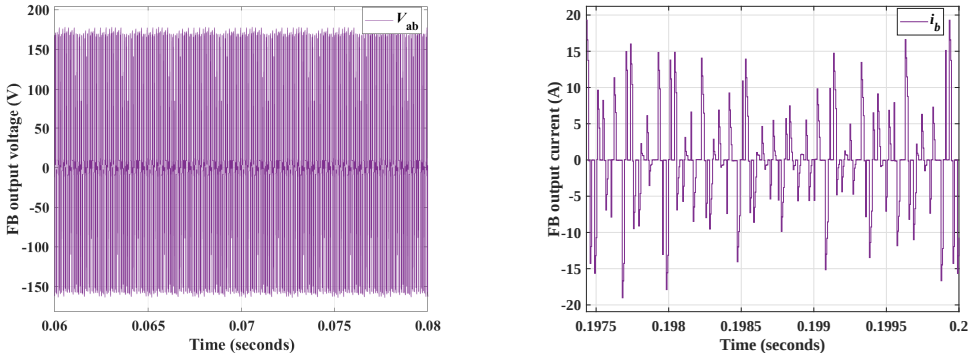
(a) (b)

Figure 3.11: Simulation results of input current and input power: (a) Input current within 0 to 0.02 s transient overshoot and from 0.02 to 0.2 s, there is no overshoot; (b) Input power within 0 to 0.02 s transient overshoot and from 0.02 to 0.2 s, there is no overshoot.

To verify the MATLAB simulation results of proposed DC-DC boost converter, the popular LT Spice software was utilised. The LT Spice simulation results of proposed converter are shown in Figures 3.18 to 3.20. These simulations validate the proposed converter architecture and the reported MATLAB simulation results. The

Table 3.2: Converter specifications.

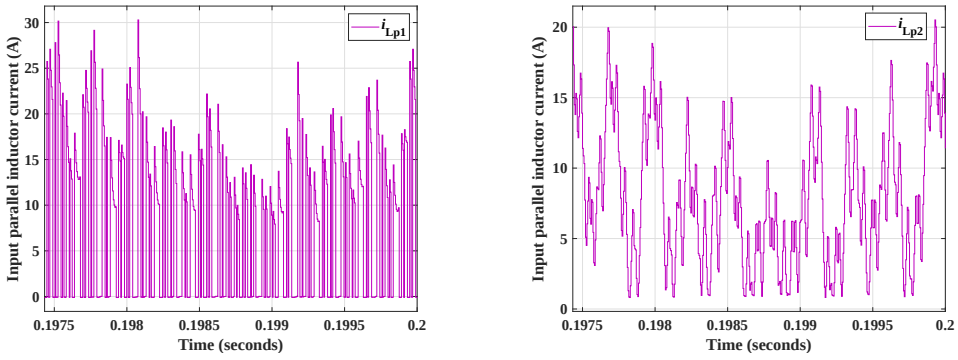
Parameters	Value
Input dc voltage, V_{in}	30–50 V
Output voltage, V_o	650 V
Output power, P_o	420 W
Input inductor, L_{p1}, L_{p2}	100 µH
Input parallel capacitor, C_P	40 µF
Transphorm GaN Switches ($S_1 - S_4$)	TPH3006PS
Switching frequency, f_{sw}	10 kHz
Modulating frequency, f_{mo}	6 MHz
Film capacitors ($C_1 - C_4$)	50 µF
Diode ($D_1 - D_4$)	IDH04G65C6
Load resistor, R_o	1 kΩ
Number of stages, N	2



(a) **(b)**

Figure 3.12: Simulation results of full bridge (FB) output voltage and current: (a) Voltage across FB output (V_{ab}); and (b) FB output current through the CW voltage multiplier (i_b).

simulation waveforms of voltage-lift switched inductor current are shown in Figure 3.18. The simulation results of CW voltage multiplier voltage and current are shown in Figures 3.19 (a) and (b), respectively, followed by the output signal of



(a) (b)

Figure 3.13: Simulation results of input voltage-lift switched inductor current (a) Current through the parallel inductor L_{p1} (i_{Lp1}); and (b) Current through the parallel inductor L_{p2} (i_{Lp2}).

Table 3.3: Performance summary of the proposed DC-DC converter topology with several other WBG power DC-DC converter topologies.

Topologies	P_o (W)	f_{sw} (MHz)	η (%) (For GaN device)	η (%) (For SiC device)	V_{in} (V)	V_o (V)	Duty cycle (%)	Dead-time (μs)
Converter in (Boutros et al. 2009)	180	0.2	>92	N/A	N/A	360	N/A	N/A
Converter in (Das et al. 2011)	100	0.5	96.1	N/A	N/A	140	50	N/A
Converter in (Huang et al. 2016)	N/A	1	98.5	N/A	150 and 380	380 and 150	>50	N/A
Converter in (Ramachandran & Nymand 2017)	2400	0.05	98.5	N/A	130	50	<50	N/A
Converter in (Zulauf et al. 2018)	1000	54.24	93.5	N/A	250	N/A	>50	N/A
Converter in (Mishima & Morita 2017)	700	0.085	93.4	N/A	230	130	>50	0.5
Converter in (Niknejad et al. 2017)	N/A	0.1	93.87	N/A	40	12	N/A	0.004
Converter in (Al-bayati et al. 2017)	280	0.02	98.25	97.85	140	48	N/A	N/A
Converter in (Al-bayati & Matin 2018)	N/A	0.1	98.082	97.450	48	400	N/A	N/A
Converter in (Alharbi et al. 2018)	600	0.05	N/A	97.5	100	400	N/A	N/A
Converter in (Mitova et al. 2013)	500	0.05	96	93.50	120	210	N/A	0.1
Proposed converter	420	0.01 and 6	98.23	N/A	50	650	50	0.3 and 0.005

the converter shown in Figure 3.20. The MATLAB simulation results of proposed DC-DC boost converter are compared, in Table 3.3, with other published converters results, in some cases using reported simulations, while in other cases using experimental results. According to the comparision analysis, the proposed converter topology has higher efficiency and higher voltage gain. In addition, the developed converter topology obtains lower output voltage ripple and current ripple.

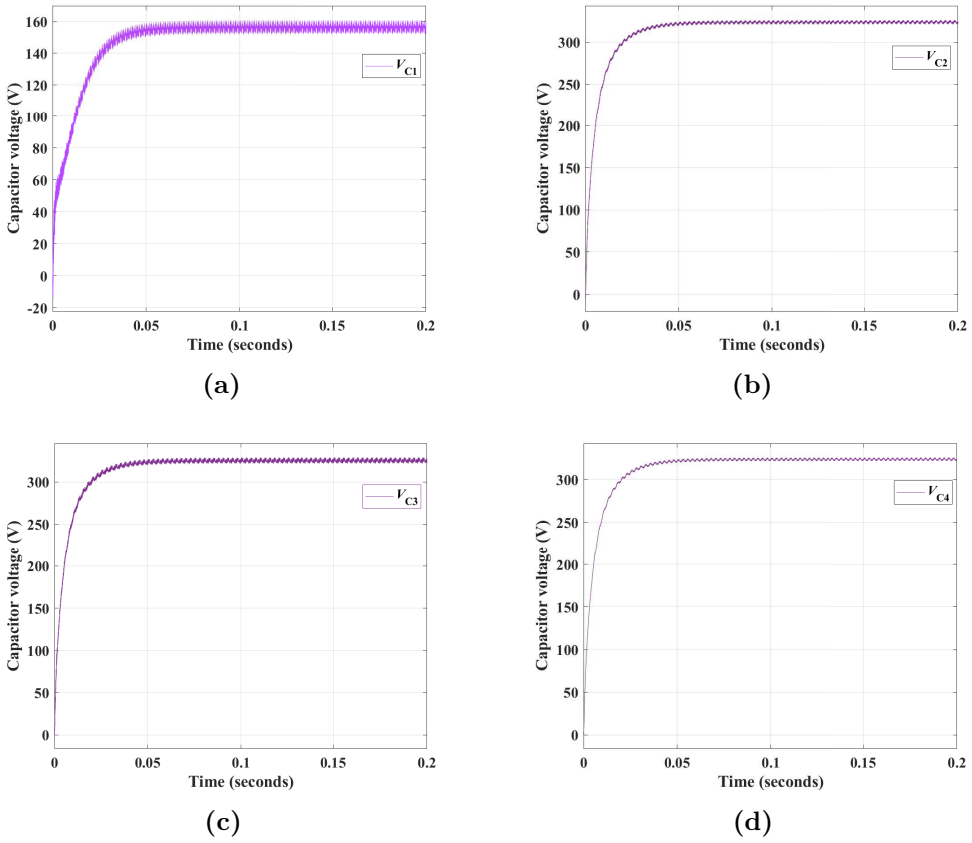
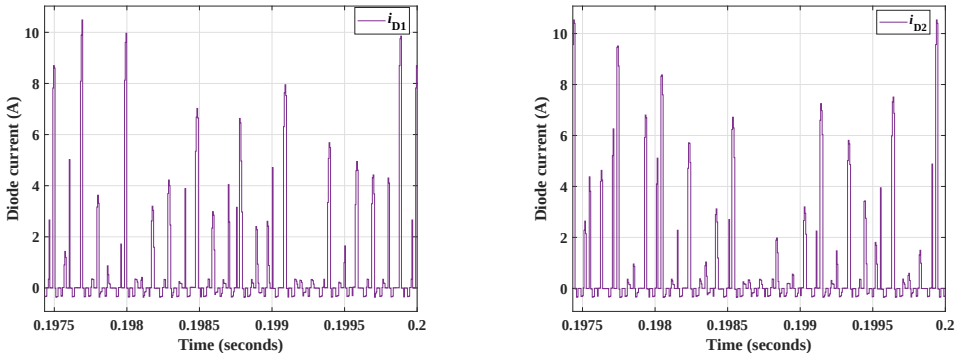


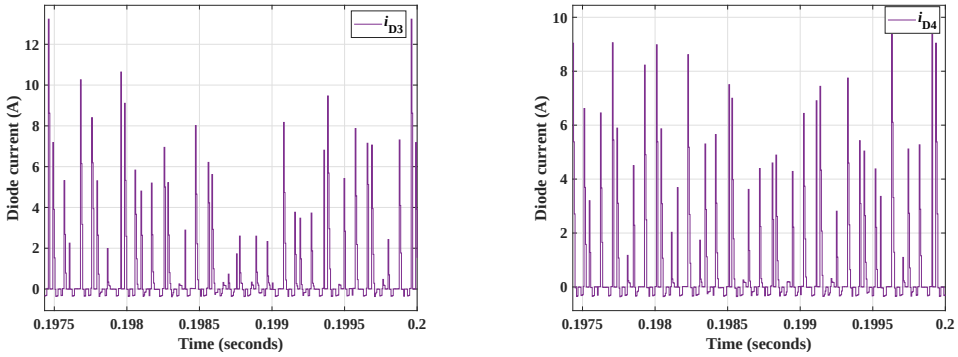
Figure 3.14: Voltage across the CW voltage multiplier capacitors within 0 to 0.05 s transient overshoot and from 0.05 to 0.2 s, there is no overshoot: (a) Voltage across the CW voltage multiplier capacitor C_1 (V_{C_1}); (b) Voltage across the CW voltage multiplier capacitor C_2 (V_{C_2}); (c) Voltage across the CW voltage multiplier capacitor C_3 (V_{C_3}), and (d) Voltage across the CW voltage multiplier capacitor C_4 (V_{C_4}).

3.5 Summary

In this chapter, the mathematical design consideration, operation principle, efficiency analysis and thermal analysis of converter are presented and discussed. An advanced control technique to control the converter was developed. The control strategy is improved to allow two independent switching frequencies: one of which operates at a high switching frequency up to the megahertz (MHz) range to reduce the size of the converter components, and the other one operates at a relatively low switching frequency which is led to output voltage ripple. When increase the switching frequency, the ripple of inductance current and capacitance voltage reduces, but it causes to increase power loss. The converter is demonstrated through the design

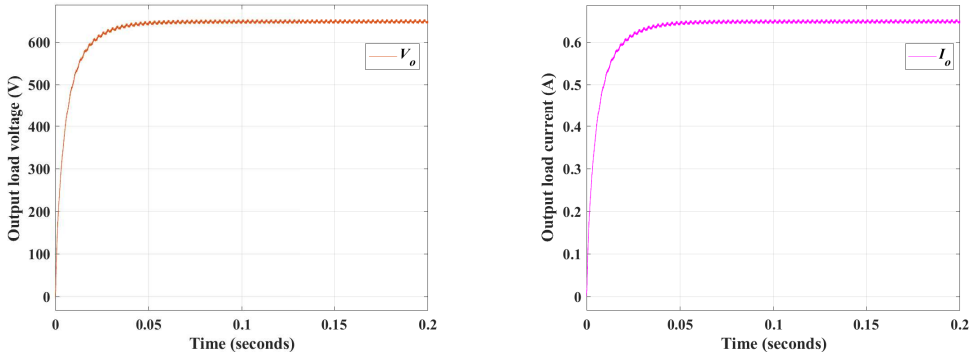


(a) Current through the diode D_1 **(b)** Current through the diode D_2



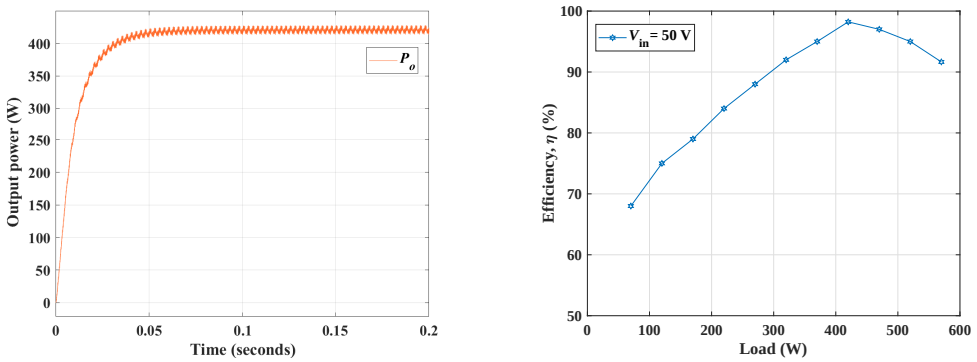
(c) Current through the diode D_3 **(d)** Current through the diode D_4

Figure 3.15: Current through the CW voltage multiplier diodes (a) Diode D_1 (i_{D_1}); (b) Diode D_2 (i_{D_2}); (c) Diode D_3 (i_{D_3}) and (d) Diode D_4 (i_{D_4}).



(a) **(b)**

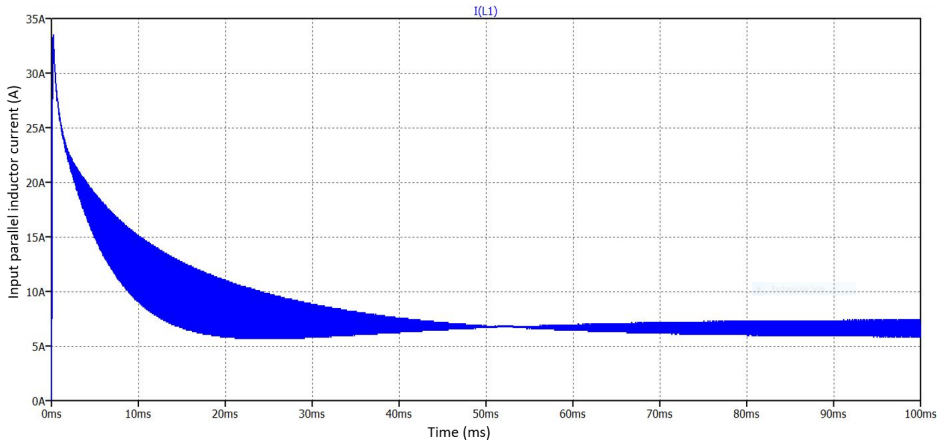
Figure 3.16: Simulation results of CW voltage multiplier output voltage and current: (a) CW voltage multiplier output voltage ($V_o = 650$ V) with 0.05 s needed to reach steady state, and (b) the corresponding output current ($I_o = 0.65$ A).



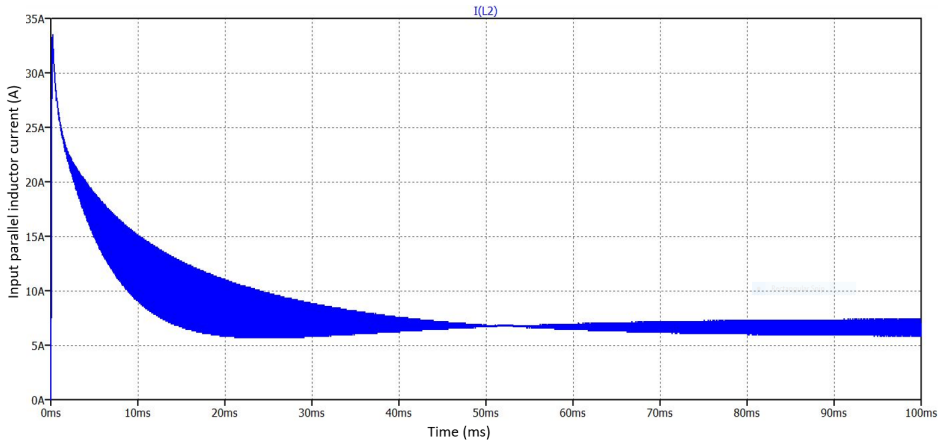
(a) (b)

Figure 3.17: (a) Simulation results of CW voltage multiplier output power (P_o = 420 W) 0.05 s needed to reach steady state, and (b) Efficiency vs output power for 2-stage based proposed converter.

of a 420-W high voltage gain, with a maximum voltage multiplication, $M_v = 13$, resulting in $V_o = 650$ V for a 50-V input. The simulated peak efficiency for this structure is 98.23% at 420 W. The performance comparison are demonstrated using Matlab based simulation of the proposed converter using practical parameter values. It is worth noting that, the proposed DC-DC converter is an open-loop system. The modelling of the feedback controller achieved by behaviour modelling, from a practical point of view, such controller is possible through using "Hardware in the Loop" modelling approach, but this option was not possible due to the pandemic.

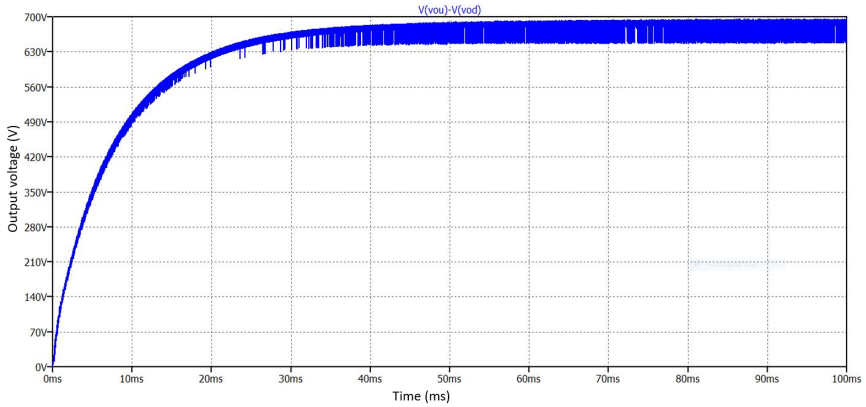


(a)

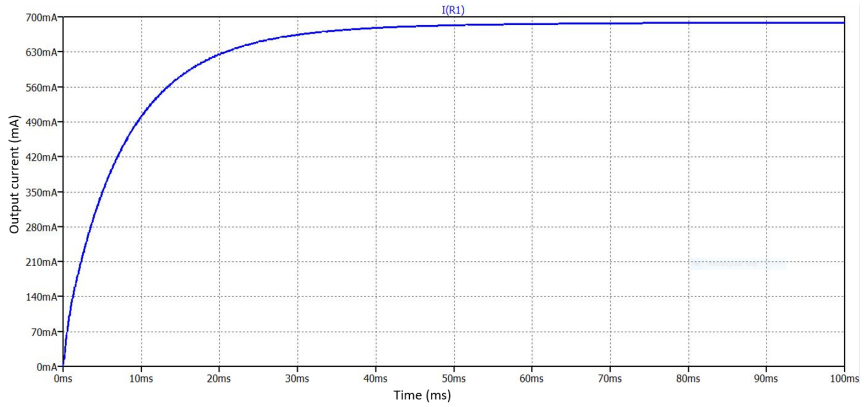


(b)

Figure 3.18: Simulation results of input voltage-lift switched inductor current using LT spice software (a) Current through the parallel inductor L_1 (i_{L1}); and (b) Current through the parallel inductor L_2 (i_{L2}).



(a)



(b)

Figure 3.19: Simulation results of CW voltage multiplier output voltage and current using LT spice software: (a) CW voltage multiplier output voltage ($V_o = 650$ V), and (b) the corresponding output current ($I_o = 650$ mA$= 0.65$ A).

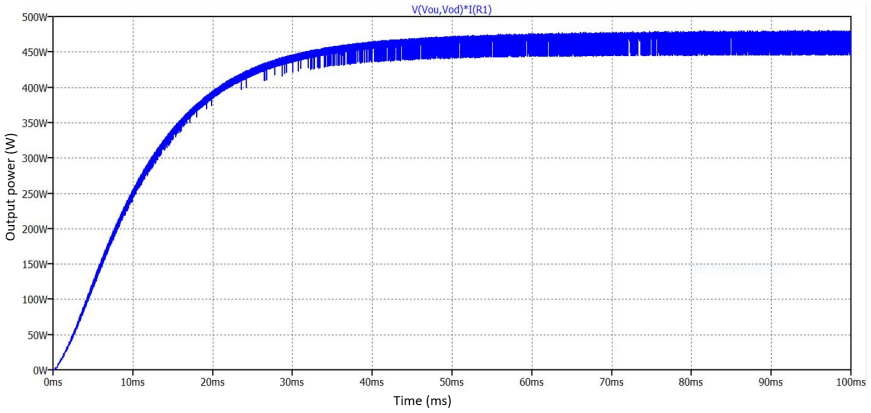


Figure 3.20: Simulation results of CW voltage multiplier output power ($P_o = 420$ W) using LT spice software.

Chapter 4

Current Controls for Single-Phase UPS Inverter

Several types of current control techniques have been used in literature, such as: proportional-integral (PI) control, proportional resonant (PR) control, repetitive current (RC) control, dead-beat (DB) control, hysteresis control, and predictive control. This chapter presents a comparative study of discrete proportional integral (PI) and proportional resonant (PR) current control for single-phase uninterruptible power supply (UPS) inverters, because these control techniques are widely used in industry and relatively easy to design. There is an increasing requirement for current and voltage-controlled UPS inverters with very low or zero steady-state error, improved transient response and lower total harmonic distortion (THD). The most promising type of current regulator for single-phase inverters is PR control because it can introduce an infinite gain at a selected resonance frequency such as the fundamental frequency to eliminate the steady-state error, which cannot be achieved by well-known proportional integral (PI) control. Note that PI control has limitations in terms of the steady-state magnitude and phase errors. In addition, PI control also has limited harmonic rejection capability, unlike the PR control, also can compensate for low-order harmonics. Imperfections in the current and voltage control scheme result in higher harmonic distortion in the output current and voltage. In this chapter, performance of PR control parameters (K_p, K_i, and ω_c) and filter parameters (L_f and C_f) are optimally tuned to obtain a very low current THD with reduced output voltage ripple and steady-state error. The analysis, design and implementation of both PI and PR current control in single-phase UPS inverter applications through simulations and experiments are also presented in this

chapter. The performance of both of these control schemes are analyzed in terms of steady-state response, transient response, and level of current harmonics.

Most of this chapter contents have been published in IEEE Access.

1. **M. Parvez,** M. F. M. Elias, N.A. Rahim, F. Blaabjerg, D. Abbott, and S. F. Al-Sarawi. Comparative Study of Discrete PI and PR Control for Single-Phase UPS Inverter. In *IEEE Access*, Published – 07 January 2020, *ISI-Indexed*, Q1, Impact factor: 4.098. DOI: 10.1109/ACCESS.2020.2964603

4.1 Introduction

Present day uninterruptible power supplies (UPSs) are most popular due to clean power delivery to the varying load in all grid conditions. With today's advancement in power electronics, it is required to design UPS systems with high-quality outputs under extreme loading conditions for communications devices, medical equipment, and military equipment. Maintaining sinusoidal output requires voltage or current regulation to be incorporated into the UPS control system, thus keeping the system output with low harmonic content for sustaining its performance, stability and reliability. According to the IEEE 1547 standard, minimum THD in the output voltage of UPS system must be maintained to less than 5% for nonlinear loads (Hossain et al. 2014, Marei et al. 2011, Nsiri et al. 2010, Blaabjerg & Ionel 2015).

The current controlled UPS inverter is more commonly used compared to voltage control inverters. The control strategy involves two cascade or inner current loops, which are used to control the utility current, and an external voltage loop that is used to control the DC-link voltage. Current-based controllers can be divided into two major categories, namely, non-linear control technique and linear control technique.

Several high performance of non-linear control schemes such as dead-beat control (Mattavelli 2005, Blaabjerg et al. 2006), hysteresis control, predictive control (Blaabjerg et al. 2006, Cortés et al. 2009), iterative learning control (Deng et al. 2007), and sliding mode control have been implemented for UPS inverters (Tai & Chen 2002, Hu et al. 2011). Among these control techniques, the dead-beat control technique

belongs to the family of predictive regulators and has been the choice in several applications (Benyoucef et al. 2014). When the deadbeat controller is optimally tuned, it provides faster transient response with close-to-zero tracking error in finite sampling steps. However, the dead-beat control is more prone to uncertainties, data mismatch and noise at high sampling frequency.

The hysteresis control method may be used in a voltage source inverter to compare the output utility current to the input reference current in order to generate switching signals for inverters. The benefits of hysteresis control are simplicity, self-dependent of load factors and good transient response (Sharma & Gali 2021, Blaabjerg et al. 2006, Parvez et al. 2016).

Predictive control method is well-known for its capability for in nonlinear control systems. The predictive control technique can obtain precise current control with low THD and noise, but it is typically quite challenging for practical implementation (Cortés et al. 2008, Gálvez-Carrillo et al. 2009, Katibi et al. 2019, Jamshed Abbas et al. 2021). This control technique observes the inverter voltage needed to force the output utility current to follow a current reference.

On the other hand, the sliding mode (SM) control technique has gained more interest for both non-linear and linear loads (Del Pizzo et al. 2017, Gensior 2020, Yan et al. 2008, Schirone et al. 2012, Navarro-López et al. 2009). The SM control technique is widely recognised as the algorithm of choice for implementing an inverter system because of its outstanding performance. The major benefits of this control is high dynamic response, stability, robustness, and easy implementation. On the other hand, the SM control technique has well known limitations when it is used with variable switching frequency, because it causes control imprecision, high power losses, and complex of output filter design. In order to overcome these limitations, rotating SM control (Komurcugil 2012, Komurcugil et al. 2015), control strategy (Kukrer et al. 2003), and the SM control with fixed switching and variable width hysteresis compensator are proposed (Pichan & Rastegar 2017, Abeywardana et al. 2016)

Currently, the SM control technique has been widely adapted due to its ability to AC tracing of the system's output (Xiong et al. 2017, Lubbad et al. 2019, Aamir et al. 2017, Abrishamifar et al. 2012). Though, this control technique has decreased

the harmonic level in the output, but it has limited rejection capability of high-order harmonics. The SM control with continuous-time control technique has been proposed, where the output filter current has been used as a state variable (Carpita & Marchesoni 1996, Chiang et al. 1998). Although, the SM control technique uses variable switching signal, it results in an undesirable chattering phenomenon. Hysteresis category switching has been considered for each leg of the inverter, resulting in further hardware complexity (Kukrer et al. 2009).

Linear control techniques, such as proportional integral (PI) control, repetitive control (RC) and proportional resonant (PR) control have been implemented in various power converters especially when tracking a sinusoidal signal for single-phase converters (Errouissi et al. 2021, Isik et al. 2021, Blaabjerg et al. 2006, Teodorescu et al. 2006, Govind et al. 2020, Güler 2020). Note that SM control together with the PI control technique has been proposed in Gudey & Gupta (2015), where the PI controller also well-known drawbacks such as being associated with a theoretically infinite gain, and it is unable to track a sinusoidal reference with steady state error. Therefore, the performance of this controller in an inverter is not adequate. The RC was built based on internal model principle (IMP), which is able to minimize steady-state error by periodically settling its parameters resulting in excellent harmonic rejection capability (Jiang et al. 2011, Baek et al. 2019). However, it is rather problematic, exhibiting a slow dynamic response that affects its stability.

Over the last decade, PR control has gained dominance in current regulation for stand-alone or grid-connected converters, which are able to track a sinusoidal current reference with minimal steady-state and phase error. Note that PR control can achieve a large gain around the resonance frequency spectrum, depending on the value of resonance gain K_r (Govind et al. 2020, Errouissi et al. 2021, Timbus et al. 2009) whilst improving the system stability.

This chapter considers both PI and PR current control techniques, focusing on single-phase UPS inverter systems. Among the control techniques, two of them have been selected for comparison in terms of performance that are proportional integral (PI) and proportional resonant (PR), taking into account their significance and also practical implementation.

A single-phase inverter for the UPS system connected to the load through an L_fC_f filter with a control strategy is shown in Figure 4.1, where V_{dc} is the inverter input DC voltage, V_o is the output voltage, L_f is the filter inductance, C_f is the filter capacitance, and R_L is the load resistor. Note that I_L is the filter current through the inductor, I_C is the filter current through the capacitor, and I_o is the output current through the resistor.

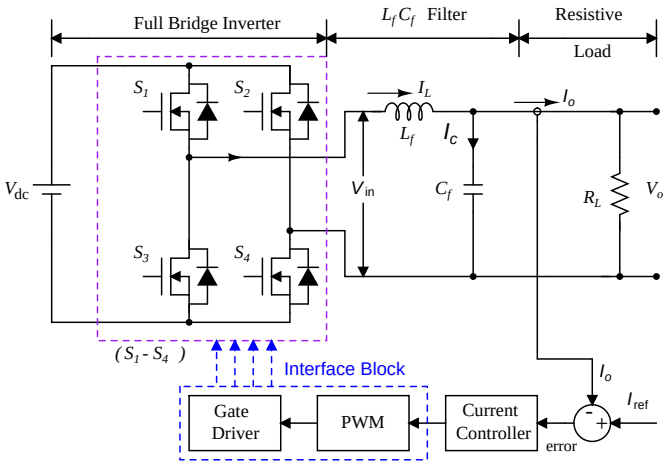


Figure 4.1: Single-phase inverter for UPS system with control strategy. The full bridge inverter is connected to the load through the low pass L_fC_f filter, where input DC voltage V_{dc} is applied through the DC power supply.

4.2 Output Filter Parameters

The pulse-width modulation invertes are widely used in many applications including single-phase stand-alone PV inverter system (Vazquez et al. 2016, Ray et al. 2017, Hossain et al. 2017). The inverter generates of output voltage due to switching which need to be filtered to generate a sinusoidal output voltage. Therefore, a power filter is essential to clean sinusoidal output and can be classified into active and passive filters. Passive filter is considered in this experiment because it is very simple and easier to be implemented.

A first order passive L-filter, which contains only inductor component, can attenuate current ripples due to inverter switching (Hobraiche et al. 2009, Kim & Sul 2011). The limitation of L-filter is the size which is very bulky especially when the system deals with high power.

A second order passive LC-filter can be used to attain a fairly good quality output which is the reason why it is very useful for standalone application (Hobraiche et al. 2009, Kim & Sul 2011, 2005). The alternative third order LCL-filter offer smaller filter size at lower switching frequencies as compared to the other two filters for the same level of current harmonics. However, due to resonance it can cause steady-state and transient problems for the output current (Güler 2020, Gabe et al. 2009, Liserre et al. 2005, Park et al. 2008).

In this study, as a trade-off between the requirement to attenuate the ripples and the LC-filter size is chosen for simulation and hardware implementation. The resonant frequency of filter can be defined by

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}}\ , \tag{4.1}$$

where f_r is the resonant frequency of filter. The transfer function of $L_f C_f$ including R_L can be expressed by

$$G_F(s) = \frac{\frac{1}{sC_f} \parallel R_L}{\frac{1}{sC_f} \parallel R_L + sL_f}. \tag{4.2}$$

The frequency response of the $L_f C_f$-filter attenuation is shown in Figure 4.2 with an attenuation of -30 dB at 20 kHz switching frequency. Therefore, the output current ripples due to inverter switching are highly attenuated.

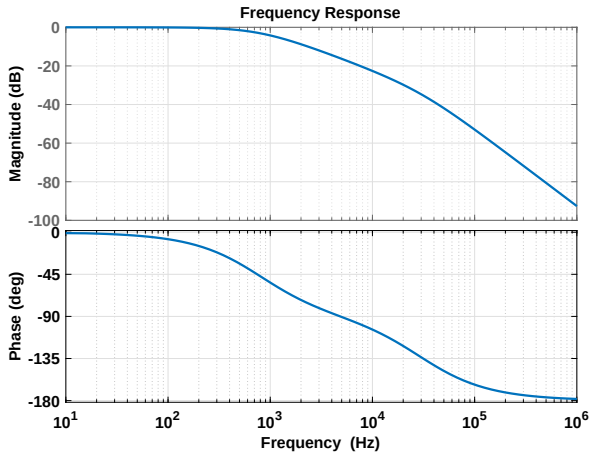


Figure 4.2: Frequency response of open-loop $L_f C_f$-filter. The magnitude of -30 dB is obtained at 20 kHz switching frequency.

4.3 Current Control using PI and PR Controller

Current control technique for single-phase UPS inverter system which can offer low harmonics content in the output current waveform. In Figure 4.1, there is only one current control loop to regulate the inverter output current to be sinusoidal. First, the current error is obtained by comparing the reference current generated and the measured load current. Then, the error will be fed to the current controller and the output is the modulating signal used for PWM switching signals generation. The output voltage is not controlled in which its magnitude depends on the amount of current flows into the load.

For stand-alone applications, the control scheme usually consists of two cascaded loops. One is the internal current loop, which is used to regulate the load current, and another is the outer voltage loop, which is used to maintain the sinusoidal output voltage (Teodorescu et al. 2004, 2006).

4.3.1 Proportional-integral (PI) controller

PI controller is one of the most studied, well-known and established controllers in many applications, in which a constant or slowly-varying reference should be tracked (Espinoza et al. 2015, Kim, Chung & Moon 2015).

A conventional s-domain PI controller can be expressed by

$$G_{\mathrm{PI}}(s) = K_p + \frac{K_i}{s}. \tag{4.3}$$

where K_p is the proportional gain constant, K_i is the integral gain constant of the controller. The low order harmonics compensation capability of this controller is very poor (Timbus et al. 2009, Hassaine et al. 2014).

4.3.2 Proportional-resonant (PR) controller

Over the last decade, PR controller popularity in current regulation for the stand-alone and grid-connected system has increased (Teodorescu et al. 2006, Hassaine et al. 2014, Monfared & Golestan 2012). Unlike PI controller, PR controller is able

to track a sinusoidal current reference with zero steady-state magnitude and phase error.

The transfer function of s-domain ideal PR controller is defined by

$$G_{\mathrm{PR}}(s) = K_p + \frac{2K_i s}{s^2 + \omega_o^2}, \tag{4.4}$$

where ω_o is the resonance frequency. The limitation of ideal PR controller which can obtain an infinite gain and zero phase shift at the resonance frequency spectrum depending on the value of the integral gain K_i. Figure 4.3 shows the frequency response of ideal PR controller.

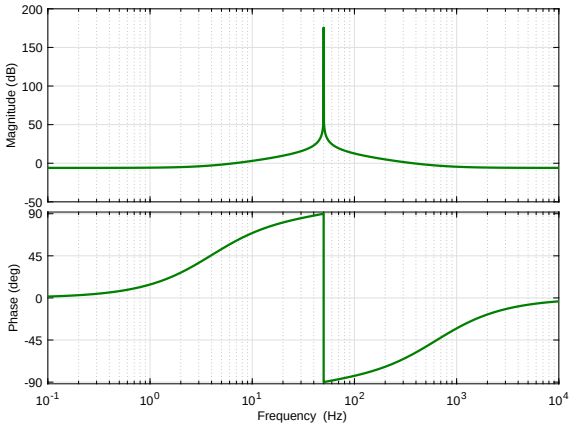


Figure 4.3: Frequency response of open-loop ideal PR controller using ($K_p = 0.5$, $K_i = 1000$, and $\omega_c = 0.1$ rad/s). The limitation of ideal PR controller is obtained very high gain and zero phase shift at fundamental frequency.

To avoid the stability problem associated with an infinite gain, a non-ideal s-domain PR controller can be expressed as

$$G_{\mathrm{PR}}(s) = K_p + K_i \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_o^2}, \tag{4.5}$$

where ω_c is the cut off frequency. The benefit of the non-ideal PR controller can achieve finite gain, which is satisfactorily high for eliminating the current tracking error.

4.3.3 Controller tuning using bode diagrams and phase margin criterion

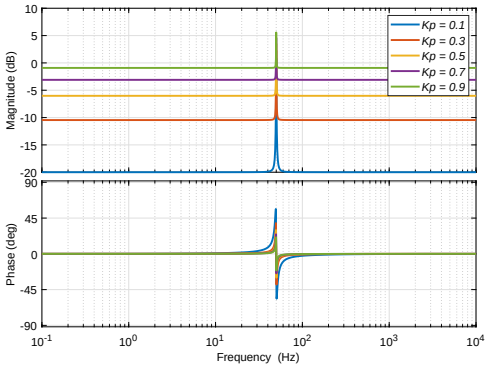
The tuning of controller parameters is normally performed using Bode diagrams and phase margin criterion, these allow analyzing the stability by means of the phase margin at the crossover frequency defined by the proportional gain. In many applications, analysis using Bode diagrams is enough to achieve required results. A more systematic method by means of Nyquist diagrams can also be used to tune the controller parameters, which can give higher stability and improved performance (Bojoi et al. 2008).

In order to investigate the effect of controller parameters on the non-ideal PR controller performance, one of the parameters will be varied while the other parameters will be kept constant. When $K_i = 1$, $\omega_c = 1$ rad/s, and the proportional gain K_p is varied, the magnitude of PR controller increases, but the phase of PR controller decreases, as shown in Figure 4.4 (a). Figure 4.4 (b) shows the frequency response of the controller in terms of the magnitude and phase when K_i is varied while $K_p = 0$, and $\omega_c = 1$ rad/s.

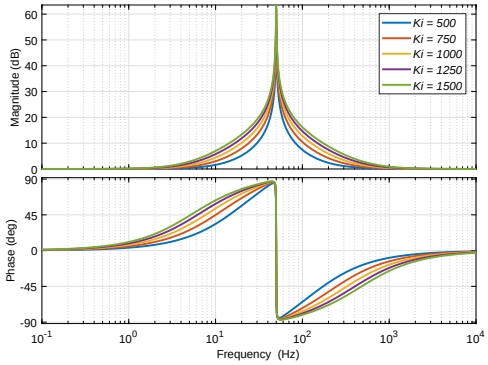
It can be observed that the magnitude of the PR controller gain increases when K_i is increased. But K_i has no effect on the bandwidth of the system as seen from the phase response of the PR controller. Assuming $K_p = 0$, $K_i = 1$, the change of ω_c has an effect on both the magnitude and the phase of the PR controller. Both the magnitude and the phase increase when ω_c is increased, as shown in Figure 4.4 (c).

As mentioned by Yang et al., the gain constants K_p and K_i can range from 0 to 1 for K_p and 100 to 2000 for K_i (Yang et al. 2015), resulting in a frequency response change for the controller as shown in Figure 4.4 (a) and (b), respectively. The controller parameters K_p and K_i are usually selected to achieve a closed-loop response, steady-state and transient performance. The K_p gives to the superior tracking performance. A higher value of K_i leads to faster response with better current harmonics rejection and also lead to higher bandwidth and phase margin.

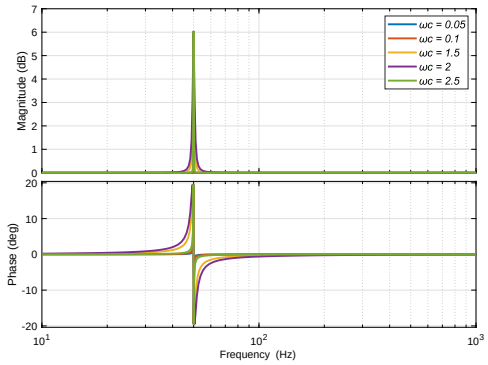
Therefore a value for ω_c can be chosen according to the required bandwidth and phase margin (Cha et al. 2009, Teodorescu et al. 2006). A higher value of ω_c increases the peak magnitude at the fundamental frequency, corresponding to higher gain and



(a)



(b)



(c)

Figure 4.4: Frequency response of open-loop non-ideal PR controller as a function of (a) K_p changes, (b) K_i changes, and (c) ω_c changes.

better ripple attenuation. A small value of ω_c gives rise to a wider bandwidth at the fundamental frequency.

The basic trade-off PR controller parameters selection requirements are as follows (Yang et al. 2015, Teodorescu et al. 2006).

- A suitable ω_c should be selected to provide a reasonable bandwidth around the resonance frequency.
- The proportional gain constant K_p is then should be selected the range from 0 to 1 to ensure that superior performance in sinusoidal reference tracking could be attained.
- Finally, K_i should be selected the range from 100 to 2000 so that the steady-state errors in both magnitude and phase are eliminated.

4.3.4 Controllers tuning using auto optimisation

To veryfy the model and controllers performance, auto optimisation technique can also be analyzed in MATLAB system. Converters are non-linear systems, analysis, control, and auto optimization could be difficult. Linear techniques based on classical controller have problems related to the stability around the operation point. Non-linear controllers such as: PI and PR controllers can be implemented to improve the stability of the converter, but such techniques could be complex. So in the following subsection, the model will be linearized before auto-optimisation can be applied. The algorithm of controllers tuning using auto optimisation technique as shown in Figure 4.5.

4.3.5 Controller performance analysis for open-loop system

Based on the initial investigation results, shown by the simulations in Figure 4.4, and the trade-off controller parameters selection requirement for resonable bandwidth, harmonic rejection capability, and higher tracking response, where the selected controller parameters are $K_p = 0.5$, $K_i = 1000$, and $\omega_c = 0.1$ rad/s.

Figure 4.6, shows the frequency response of non-ideal PR controller in MATLAB using the selected values, while Figures 4.7 show the frequency response results after using auto optimisation values. The simulation results shown in Figure 4.6

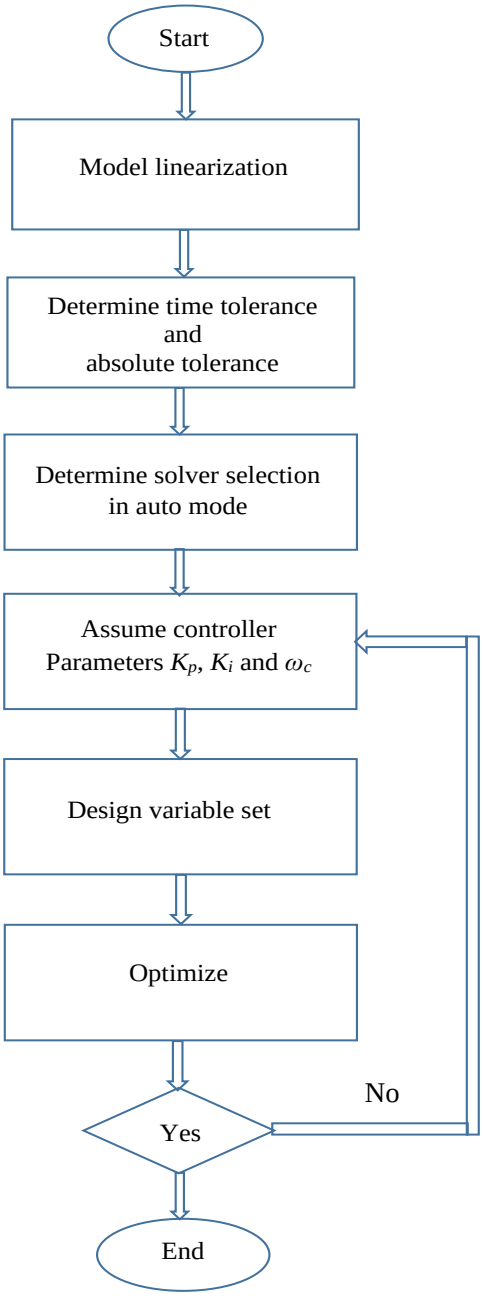


Figure 4.5: Flow chart of controllers tuning using auto optimisation.

indicate that the transfer function of open loop non-ideal PR controller shows that the gain margin of the system is finite, and the phase margin of the system is 79.3°(leading), and 76.4°(lagging) at under frequency (48 Hz), and over frequency (51 Hz), respectively.

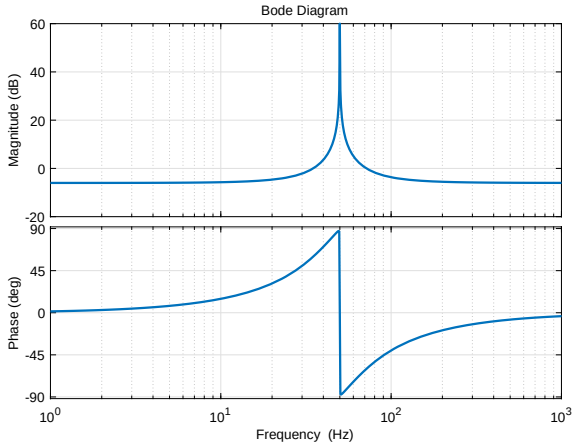


Figure 4.6: Frequency response of open-loop non-ideal PR controller using the selected values ($K_p = 0.5$, $K_i = 1000$, and $\omega_c = 0.1$ rad/s). The non-ideal PR controller is reduced the stability problem associated with an infinite gain.

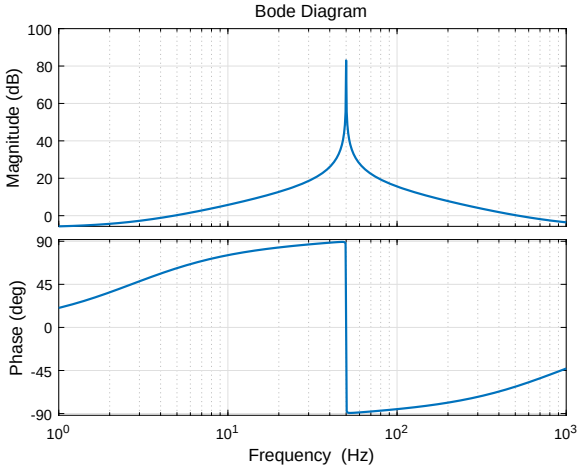


Figure 4.7: Frequency response of open-loop non-ideal PR controller using auto optimisation values ($K_p = 0.4856$, $K_i = 14164$, and $\omega_c = 0.1$ rad/s). The non-ideal PR controller is reduced the stability problem associated with an infinite gain.

4.4 Closed-Loop Current Controllers

For comparison, both the closed-loop transfer functions of the PI and PR current controllers are analyzed. Block diagrams of closed-loop PI and PR current control schemes used for the comparison are shown in Figures 4.8 and 4.9 respectively.

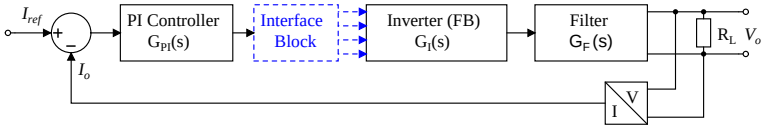


Figure 4.8: Block diagram of closed-loop PI control scheme.

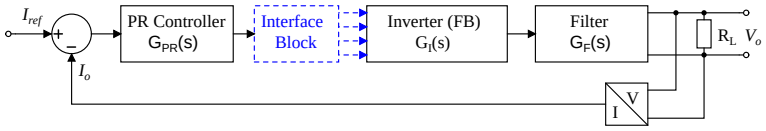


Figure 4.9: Block diagram of closed-loop PR control scheme.

The closed-loop transfer function of the system using PI controller can be defined by

$$M_{\mathrm{PI}}(s) = \frac{I_o}{I_{\mathrm{ref}}} = \frac{G_{\mathrm{PI}}(s)G_I(s)G_F(s)}{1 + G_{\mathrm{PI}}(s)G_I(s)G_F(s)}, \tag{4.6}$$

where $G_{\mathrm{PI}}(s) = K_p + \frac{K_i}{s}$, $G_I(s) = K$ and $G_F(s) = \frac{R_L}{R_L L_f C_f s^2 + L_f s + R_L}$ are the transfer functions of the PI controller, the inverter, and the filter including the load, respectively. Substituting all the transfer functions yields the complete transfer function of the system that is represented by

$$M_{\mathrm{PI}}(s) = \frac{K(K_p s + K_i)}{L_f C_f s^3 + \frac{L_f}{R_L} s^2 + (1 + KK_p)s + KK_i}. \tag{4.7}$$

Similarly, the closed-loop transfer function of the system using PR controller can be defined by

$$M_{\mathrm{PR}}(s) = \frac{I_o}{I_{\mathrm{ref}}} = \frac{G_{\mathrm{PR}}(s)G_I(s)G_F(s)}{1 + G_{\mathrm{PR}}(s)G_I(s)G_F(s)}, \tag{4.8}$$

where $G_{\mathrm{PR}}(s) = K_p + K_i \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_o^2}$, $G_I(s) = K$, and $G_F(s) = \frac{R_L}{R_L L_f C_f s^2 + L_f s + R_L}$ are the transfer functions of the PR controller, the inverter, and the filter including the load, respectively. The complete transfer function of the system can be obtained by

$$M_{\mathrm{PR}}(s) = \frac{K\{K_p s^2 + 2(K_p\omega_c + K_i\omega_c)s + K_p\omega_o^2\}}{\lambda_4 s^4 + \lambda_3 s^3 + \lambda_2 s^2 + \lambda_1 s + \lambda_o}, \tag{4.9}$$

where $\lambda_4 = L_f C_f$;
$\lambda_3 = (\frac{L_f}{R_L} + 2\omega_c L_f C_f)$;
$\lambda_2 = (1 + 2\omega_c \frac{L_f}{R_L} + L_f C_f \omega_o^2 + KK_p)$;
$\lambda_1 = (2\omega_c + \omega_o^2 \frac{L_f}{R_L} + 2KK_p\omega_c + 2KK_i\omega_c)$; and
$\lambda_o = \omega_o^2 + KK_p\omega_o^2$.

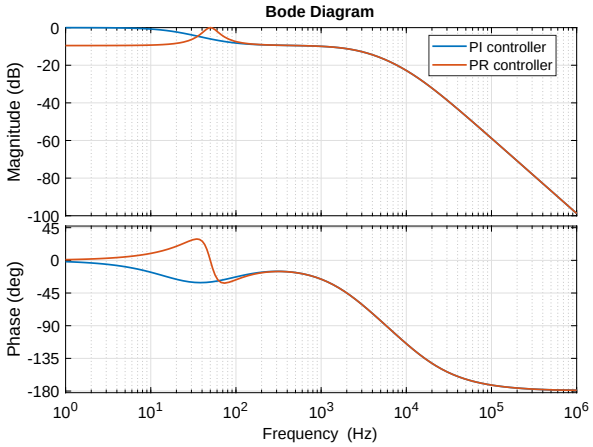


Figure 4.10: Frequency response of closed-loop transfer function using PI controller ($K_p = 0.5$, and $K_i = 200$); and using PR controller ($K_p = 0.5$, $K_i = 1000$, $\omega_o = 314$ rad/s, and $\omega_c = 0.1$ rad/s).

4.4.1 Controller performance analysis for closed-loop system

Typically, a closed-loop system attains improved stability compared to an open loop system, since it has better disturbance rejection capability. Although the PR controller has more advantages over PI controllers, its closed-loop performance can be affected by a various factors such as grid frequency variation, voltage fliker, etc. When the fundamental frequency of the PR controller varies, the expected output will be attenuated and will contain a phase error. The effect of frequency variation is not performed on PI controller since its output system is unstable.

Figure 4.10 shows the frequency responses of the closed-loop PI and PR current controller using optimal tuned values. Therefore the effect of frequency variation can be investigated from the figure, where the PR controller maintains its stability where the phase margin of the system is 15.1° (leading), and 3.46° (lagging) at under frequency (48 Hz), and over frequency (51 Hz), respectively. The bandwidth can be widened by tuning ω_c appropriately, which can reduce the controller sensitivity to slight frequency variations (Teodorescu et al. 2006).

For a more realistic analysis, the frequency responses of closed-loop PI and PR controllers using auto optimisation values are shown in Figure 4.11 where the target frequency variation is attained and phase error is highly attenuated.

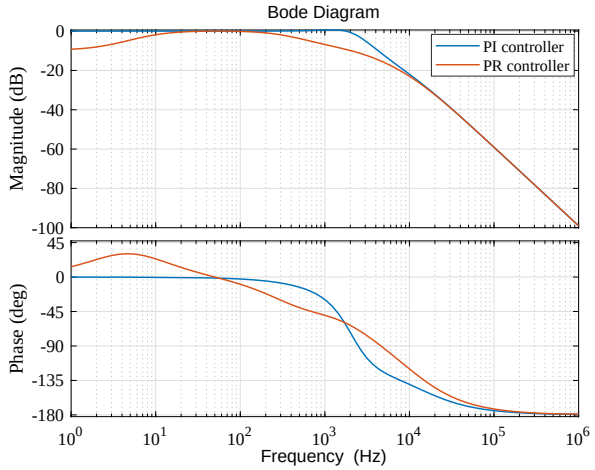


Figure 4.11: Frequency response of closed-loop transfer function using PI controller ($K_p = 0.4856$, and $K_i = 14164$); and using PR controller ($K_p = 0.4856$, $K_i = 14164$, $\omega_o = 314$ rad/s, and $\omega_c = 0.1$ rad/s).

4.4.2 Implementation of PI controller using discrete transfer function

The discrete transfer function of the PI controller can be obtained by applying the bilinear transformation and substituting $s = \frac{2(z-1)}{T(z+1)}$ into in $G_{\text{PI}}(s) = K_p + \frac{K_i}{s}$. This yields the following transfer function in z-domain;

$$G_{\text{PI}}(z) = \frac{(K_p + K_i\frac{T}{2}) + (-K_p + K_i\frac{T}{2})z^{-1}}{1 - z^{-1}} \tag{4.10}$$

$$G_{\text{PI}}(z) = \frac{b_0 + b_1 z^{-1}}{a_0 + a_1 z^{-1}}\ , \tag{4.11}$$

where T is the sampling time and: $b_o = K_p + K_i\frac{T}{2}$, $b_1 = -K_p + K_i\frac{T}{2}$, and $a_0 = 1$.

Figure 4.12 shows a block diagram of discrete transfer function of the PI controller.

Finally, the difference equation of PI controller can be written as

$$u(n) = b_0 e(n) + b_1 e(n-1) - a_1 u(n-1), \tag{4.12}$$

where, $u(n)$ is the present controller output, $u(n-1)$ is the previous controller output, $e(n)$ is the present error, and $e(n-1)$ is the previous error.

Based on the optimised PI controller parameters ($K_p = 0.5$ and $K_i = 200$), the coefficients of the PI controller become, $b_0 = 0.505$, $b_1 = -0.995$, and $a_1 = -1$.

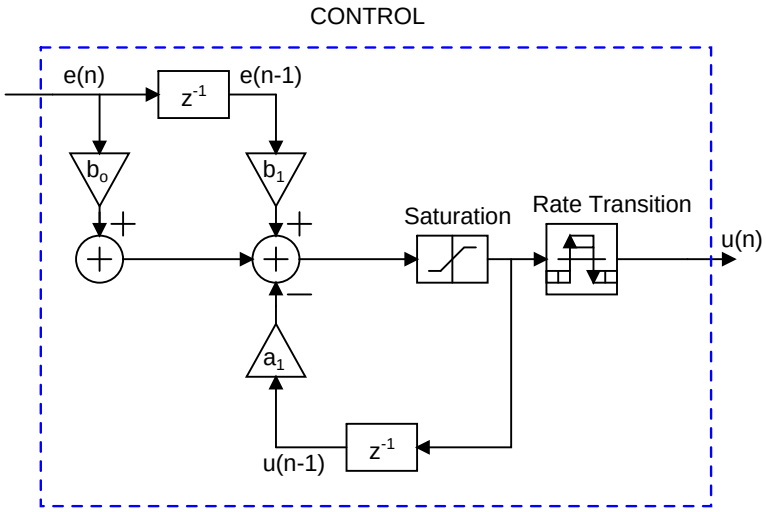


Figure 4.12: Discrete PI control.

The transfer function in z-domain PI controller is given by

$$G_{\mathrm{PI}}(z) = \frac{0.505 - 0.995z^{-1}}{1 - z^{-1}}. \tag{4.13}$$

4.4.3 Implementation of PR controller using discrete transfer function

The discrete transfer function of the non-ideal PR controller can be obtained by applying bi-linear transformation and putting $s = \frac{2(z-1)}{T(z+1)}$ into in $G_{\mathrm{PR}}(s) = K_p + K_i \frac{2\omega_c s}{s^2+2\omega_c s+\omega_o^2}$. This yields the following transfer function in the z-domain;

$$G_{\mathrm{PR}}(z) = K_p + \frac{2K_i\omega_c \frac{2(z-1)}{T(z+1)}}{\frac{4(z-1)^2}{T^2(z+1)^2} + 2\omega_c \frac{2(z-1)}{T(z+1)} + \omega_o^2}, \tag{4.14}$$

where T is the sampling time. Equation (4.14) can be rearranged in the following form in terms of the controller's output $U(z)$ and the error $E(z)$,

$$G_{\mathrm{PR}}(z) = \frac{U(z)}{E(z)} = \frac{b_0 + b_1 z^1 + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}, \tag{4.15}$$

where

$b_0 = \frac{(4+4T\omega_c+\omega_o^2T^2)K_p+4K_iT\omega_c}{4+4T\omega_c+\omega_o^2T^2}$, $b_1 = \frac{(2\omega_o^2T^2-8)K_p}{4+4T\omega_c+\omega_o^2T^2}$, $b_2 = \frac{(4-4T\omega_c+\omega_o^2T^2)K_p-4K_iT\omega_c}{4+4T\omega_c+\omega_o^2T^2}$,

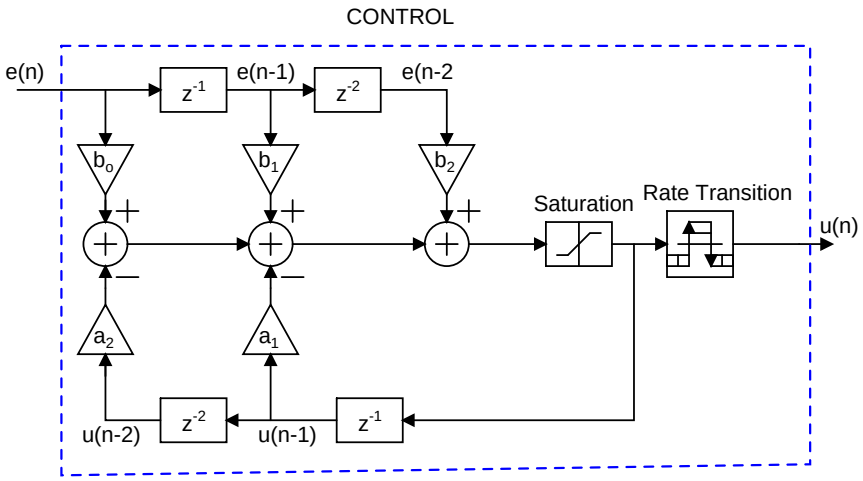


Figure 4.13: Discrete PR control.

$a_0 = 1$, $a_1 = \frac{2\omega_o^2T^2-8}{4+4T\omega_c+\omega_o^2T^2}$, and $a_2 = \frac{4-4T\omega_c+\omega_o^2T^2}{4+4T\omega_c+\omega_o^2T^2}$.

Figure 4.13 shows a block diagram of discrete transfer function of the PR controller.

Finally, the difference equation of the PR controller for hardware implementation is given by

$$u(n) = b_0e(n) + b_1e(n-1) + b_2e(n-2) - a_1u(n-1) - a_2u(n-2). \tag{4.16}$$

Based on the optimised PR controller parameters ($K_p = 0.5$, $K_i = 1000$ and $\omega_c = 0.1$ rad/s), the coefficients of the PR controller become, $b_0 = 0.504999$, $b_1 = -0.99987$, $b_2 = 0.494995$, $a_0 = 1$, $a_1 = -1.9997$, and $a_2 = 1$.

The transfer function in the z-domain of the PR controller is given by

$$G_{\mathrm{PR}}(z) = \frac{U(z)}{E(z)} = \frac{0.504999 - 0.99987z^{-1} + 0.494995z^{-2}}{1 - 1.9997z^{-1} + z^{-2}}. \tag{4.17}$$

4.5 Design and Setup

The experimental prototype for testing the performance of both PI and PR current controllers is shown in Figure 4.14, with the inverter parameters are given in Table 4.1. At ideal condition, the IGBT module inverter gain consider can be considered $K = 1$. The switching frequency range can be considered from 10 to 20 kHz for the IGBT module inverter gain as a constant. For this project, we consider the 20 kHz switching frequency at inverter gain constant $K = 1$.

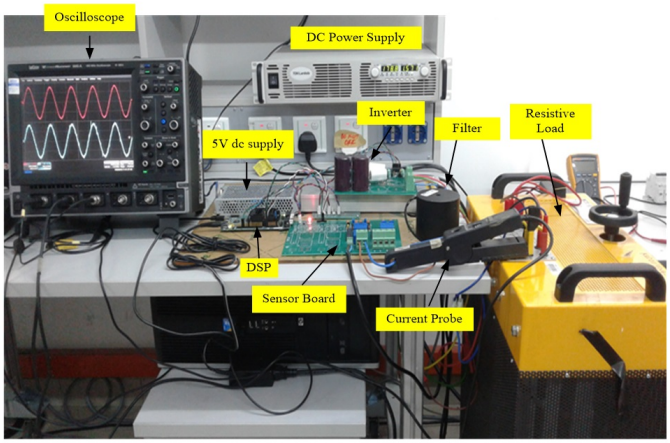


Figure 4.14: Experimental setup.

Table 4.1: Inverter specifications.

Parameters	Value
DC voltage, V_{dc}	180 V
IGBT Module (S1-S4)	INFINEON (F4-50R06W1E30)
Voltage transducer	LEM LV25 – P
Current transducer	LEM LA25 – NP
Filter inductor, L_f	5 mH
Filter capacitance, C_f	0.22 μF
Resistor, R_L	50 Ω
Proportional gain constant, K_p	0.5
PI/PR Controller Integral gain constant, K_i	200/1000
Cut-off frequency, ω_c	0.1 rad/s
Switching frequency, f_s	20 kHz

The inverter is connected to the resistive load through the LC filter. For implementation of both controllers' algorithms, a 32-bit floating-point TMS320F28335 eZdsp provide a reference to the board. A C program for both controllers was developed by using Texas Instrument Code Composer Studio 6.0 (CCS) software. The inverter switching frequency is set to 20 kHz and the dead-band time is set t_{d1}=1.3 μs for the switching frequency. The PWM pulses are generated through the internal

Table 4.2: Optimised value of controller parameters using phase margin criterion.

Parameters	Value
Proportional gain constant, K_p	0.5
PI/PR Controller Integral gain constant, K_i	200/1000
Cut-off frequency, ω_c	0.1 rad/s

Table 4.3: Optimised value of controller parameters using auto optimisation.

Parameters	Value
Proportional gain constant, K_p	0.4856
Integral gain constant, K_i	14164
Cut-off frequency, ω_c	0.1 rad/s

PWM module of the digital signal processor (DSP). Voltage and current signals are measured by using a 12-bit analog-to-digital converter (ADC) built in the eZdsp development board. A sinusoidal reference signal is generated by sensing the grid voltage and frequency using a phase-locked-loop module, which consisting of a variable frequency oscillator and a phase detector in a feedback loop. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal. When the two signal inputs are equal in phase and frequency, the error will be constant and the loop is said to be in a "locked" condition. The power electronic switches used were IGBT-based modules. Tables 4.2, and 4.3 shows the optimised value of controller parameters using phase margin criterion, and auto optimisation, respectively.

4.6 Simulation and Experimental Study

The simulation and experiment implementation results of PI and PR current controllers for a single-phase UPS inverter are presented. Simulation results have been

carriied out for a single-phase UPS inverter using MATLAB/SIMULINK® software. Simulink model of single-phase inverter including controller for linear load and non-linear load is shown in Figure 4.15 and 4.16, respectively.

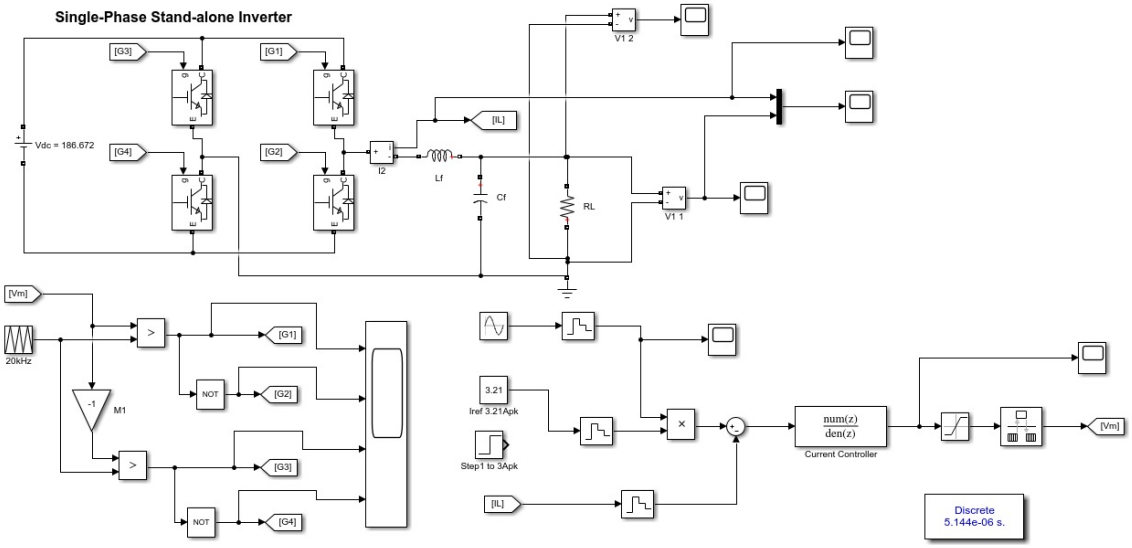


Figure 4.15: Simulink model of a single-phase inverter including controller for linear load.

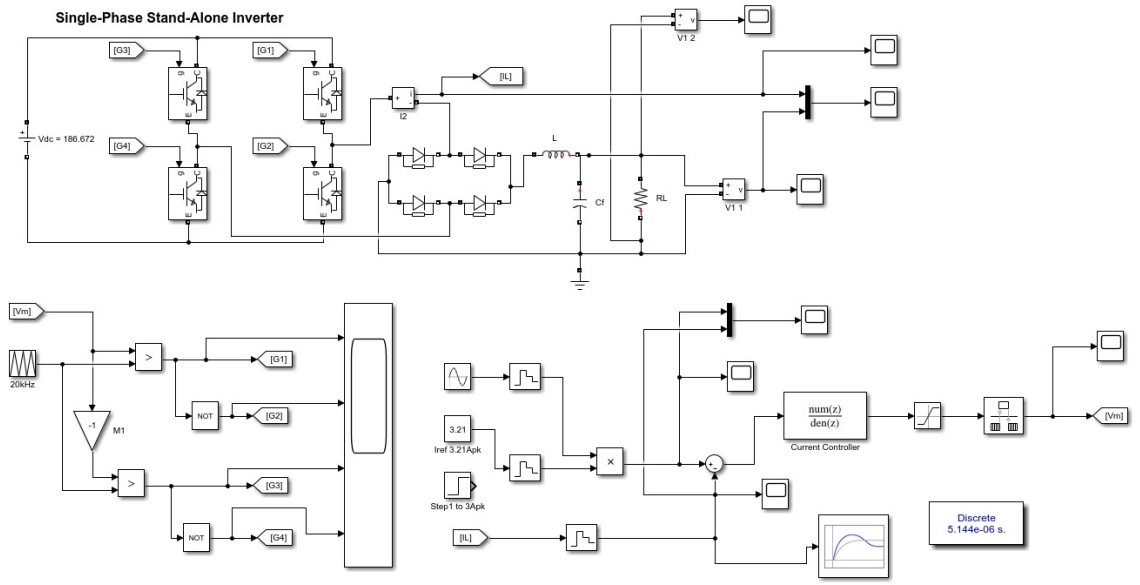


Figure 4.16: Simulink model of a single-phase inverter including controller for non-linear load.

In simulation, DC voltage source V_{dc} is 180 V. The performance of both controllers is compared in terms of the steady-state response, transient response, and current total

harmonic distortion (THDi). The optimised control parameters were obtained from the simulation then used for experimental verification. To observe the performance of current controller, the inverter can also be integrated with current power distribution network but there is a requirement for grid synchronization using a phase-lock loop (PLL). The experimental set up is demonstrated through a 250 W inverter operating at an RMS voltage of 110 V. The RMS current is therefore equal to 2.27 A with 3.21 A peak value. Figure 4.17 shows PWM pattern for unfiltered inverter output voltage.

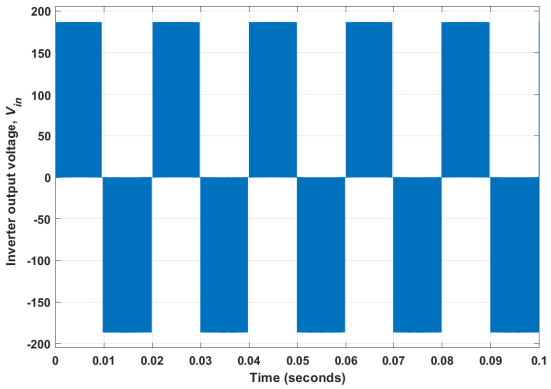


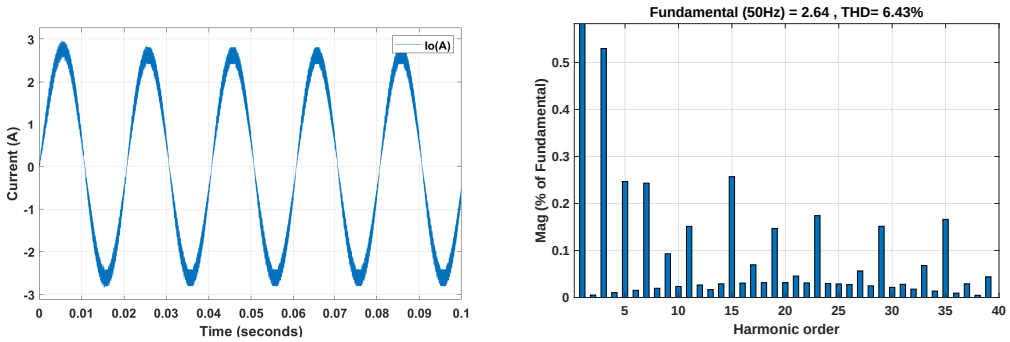
Figure 4.17: Simulation result of inverter output voltage before filter.

4.6.1 Steady-state response of PI and PR controllers

The controller parameters of K_p, K_i, and ω_c have been optimally set for UPS inverter. The simulation results of load current and fast fourier transform (FFT) analysis of THD using selected values from Bode plot and phase margin criterion are shown in Figures 4.18, and 4.19, respectively.

When using the PI controller, FFT analysis on the load current yields a THD value of 6.43% as shown in Figure 4.18 (b), whereas FFT analysis on the load current yields a THD value of 4.88% by the PR controller as shown in Figure 4.19 (b). These results indicate that the current harmonics have been well suppressed by the PR controller.

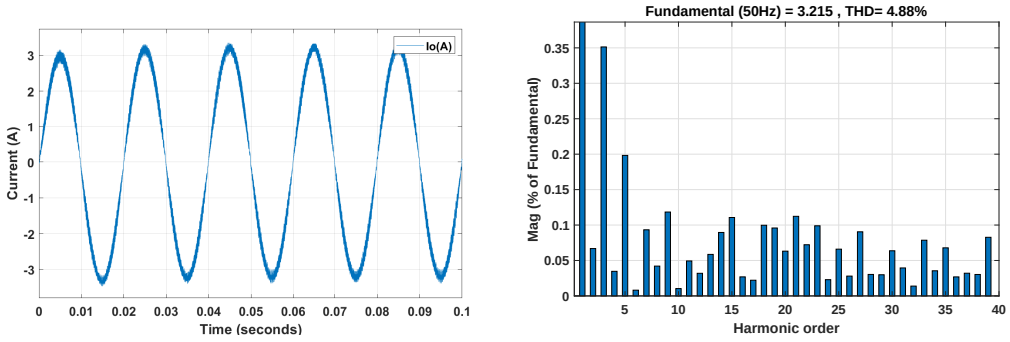
The simulation results of load current and FFT analysis of THD using auto optimisation values are shown in Figures 4.20, and 4.21. It can be observed from Figure 4.20



(a) Load current

(b) FFT analysis of THD for the number of harmonic order 40

Figure 4.18: Simulation results of load current and FFT analysis of THD using selected values from Bode plot and phase margin criterion for PI controller ($K_p = 0.5$, and $K_i = 200$).



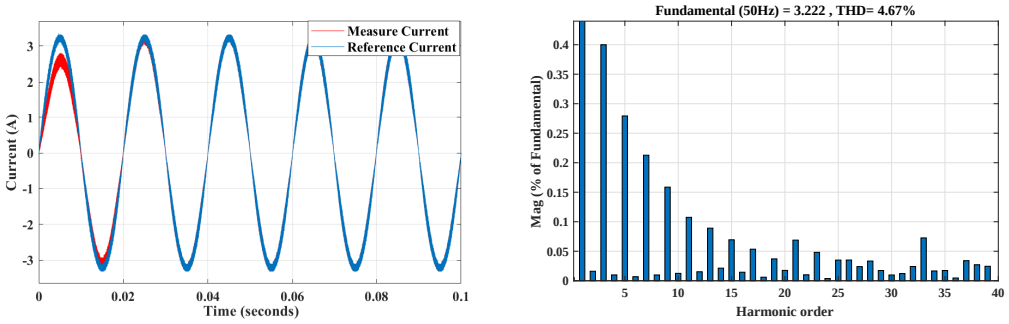
(a) Load current

(b) FFT analysis of THD for the number of harmonic order 40

Figure 4.19: Simulation results of load current and FFT analysis of THD using selected values from Bode plot and phase margin criterion for PR controller ($K_p = 0.5$, and $K_i = 1000$).

when using auto optimisation values in the PI controller, although a lower THD value is achieved, the current response is relatively slow. After certain time the current reaches steady-state. On the other hand, Figure 4.21 shows a faster current response, better tracking performance and low THD when using auto optimisation values in the PR controller.

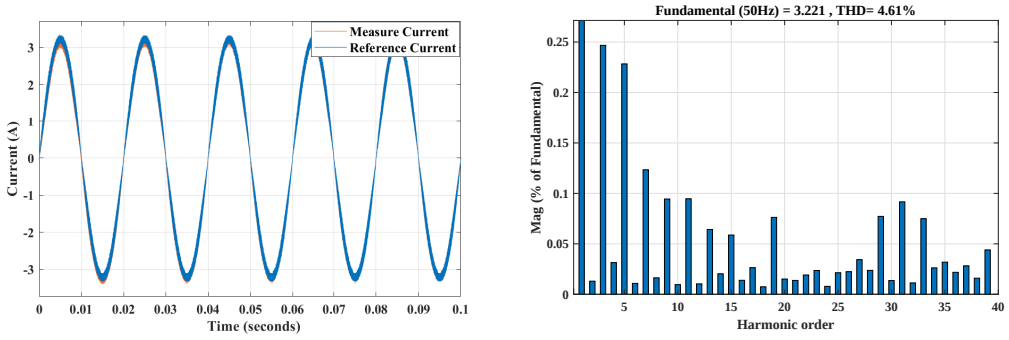
However, maintenance of power quality requires rapid energy transfers to mute the effects of switching transients, arcs, harmonic generation by nonlinear loads, etc (Pickard & Abbott 2012). In addition, to observe the performance of the PR



(a) Load current

(b) FFT analysis of THD for the number of harmonic order 40

Figure 4.20: Simulation results of load current and FFT analysis using auto optimization values for PI controller ($K_p = 0.4856$, and $K_i = 14164$).



(a) Load current

(b) FFT analysis of THD for the number of harmonic order 40

Figure 4.21: Simulation results of load current and FFT analysis using auto optimization values for PR controller ($K_p = 0.4856$, and $K_i = 14164$).

controller in a non-linear load, steady-state non-linear load tests are performed using an uncontrolled full bridge diode rectifier within a MATLAB simulation. The rectifier used between the inverter output and load. The simulation results of output voltage, current, and FFT analysis of current THD using the non-linear load (uncontrolled full bridge diode rectifier connected between the inverter output and resitive load) with the PR controller is presented in Figures 4.22, 4.23, and 4.24. According to the IEC 62040-3 standard, the current THD has tolerable increased with a nonlinear load.

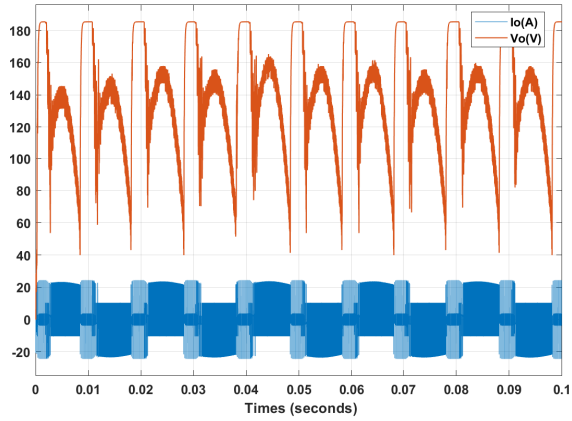


Figure 4.22: Simulation results of output voltage and current using non-linear load for PR controller. The steady-state non-linear load tests are performed using an uncontrolled full bridge diode rectifier within a MATLAB simulation.

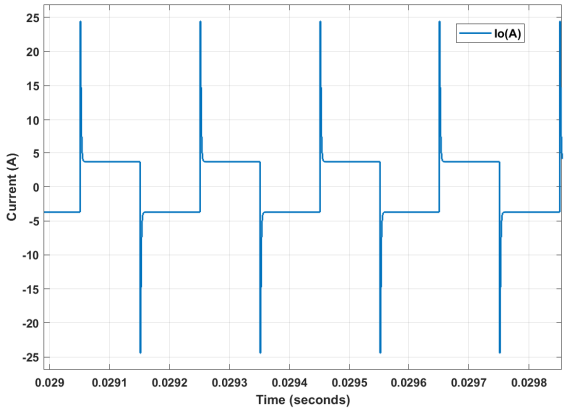


Figure 4.23: Simulation result of output current with zoom using non-linear load for PR controller.

The experimental results showing load current, load voltage, and FFT analysis of load current are given in Figures 4.25 and 4.26. From 4.25 (a), the load current only reaches 2.8 A peak, which represents an error of 12.77% from the reference current $I_{\text{ref}} = 3.21$ A peak. Both experiment and simulation results of load current show that steady-state error occurs when using the PI controller. From 4.26 (a), the load current reaches a maximum of 3.21 A peak of the current reference when using the PR controller.

It is clear that the load current achieves zero steady-state error as compared to PI controller, of 12.77%. The FFT analysis of the load current for both the PI and PR

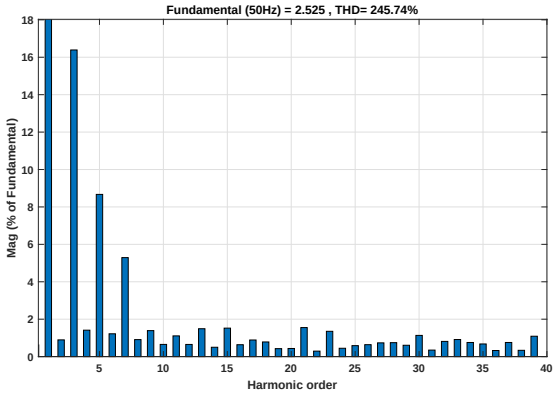
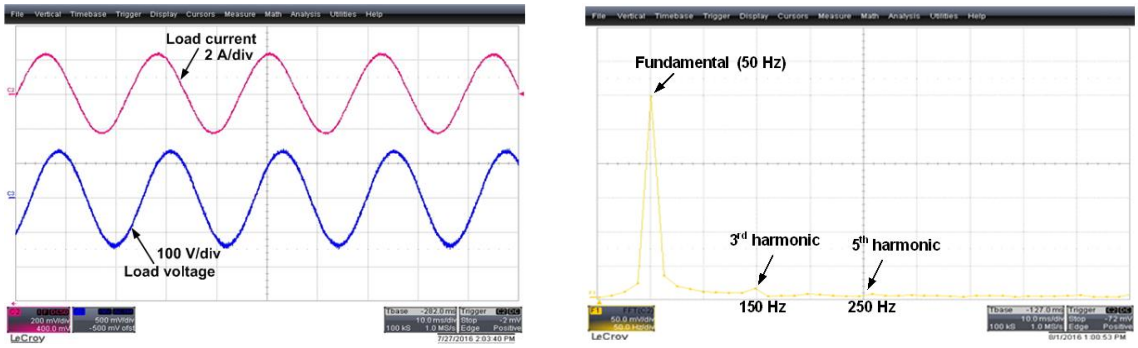


Figure 4.24: Simulation result of FFT analysis of current THD using non-linear load for PR controller.

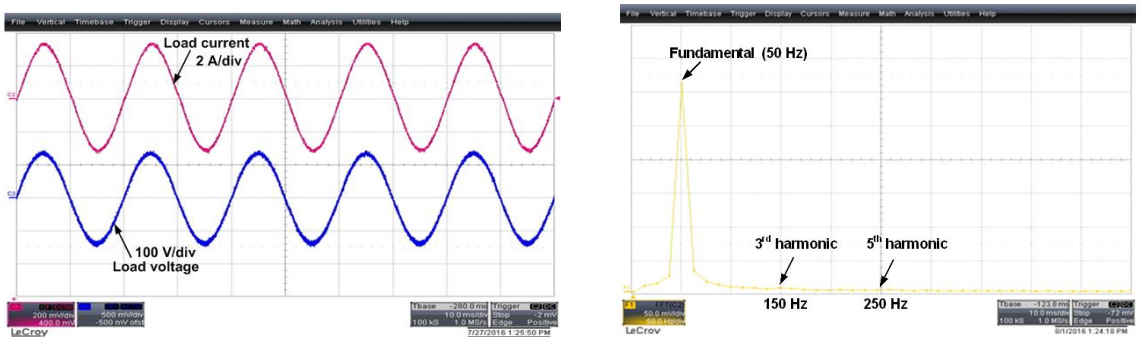
controller are shown in Figures 4.25 (b) and 4.26 (b), respectively. It can be seen from Figure 4.26 (b), when using the PR controller the magnitudes of 3^{rd} and 5^{th} harmonics were found to be very low as compared to those of the PI controller in Figure 4.25 (b).



(a) Load current and voltage **(b)** FFT analysis of load current

Figure 4.25: Experimental results of load current and FFT analysis of load current using PI controller.

Moreover, the harmonic rejection capabilities of the PI controller and the PR controller are compared, as shown in Figure 4.27. It can be observed that the PR controller can obtain an overall current THD level lower than 5%, and individual harmonics level lower than 4%, that are meet in IEEE standards requirments (*IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems* 2009).



(a) Load current and voltage **(b)** FFT analysis of load current

Figure 4.26: Experimental results of load current and FFT analysis of load current using PR controller.

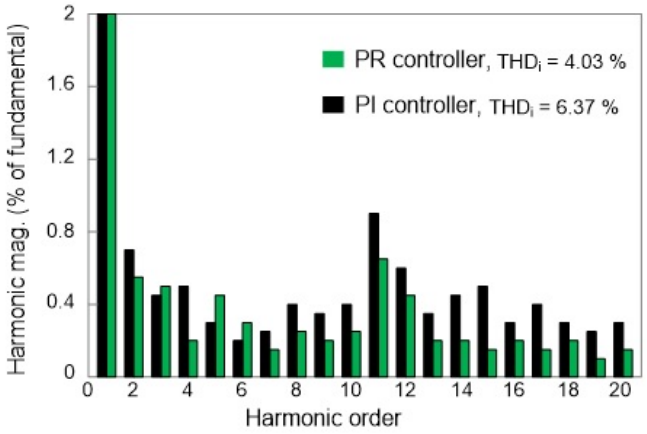


Figure 4.27: Total harmonic distortion (THD) of load current using PI and PR controller.

When the value of K_p is increased ($K_p = 0.7$) for PI controller, the results of load current and voltage are shown in Figure 4.28. The current reaches the maximum of 3.21 A peak, but it is over modulated with more ripple in the output current and voltage, and therefore an increased 3rd harmonic level is observed.

Note that the optimal selection of K_p is most significant for both THD and the steady-state condition. The simulated dependence of the THD on K_p and how that impacts the stead-state error is shown in Figure 4.29. It can be observed from Figure 4.29 (a), when the value of K_p is increased from 0.1 to 0.6, the measured THD for both controllers slightly increases.

On the other hand, when K_p is increased from 0.6 to 1.5, the output is more distorted resulting in greater THD. Figure 4.29 (b) shows the steady-state error for the PI

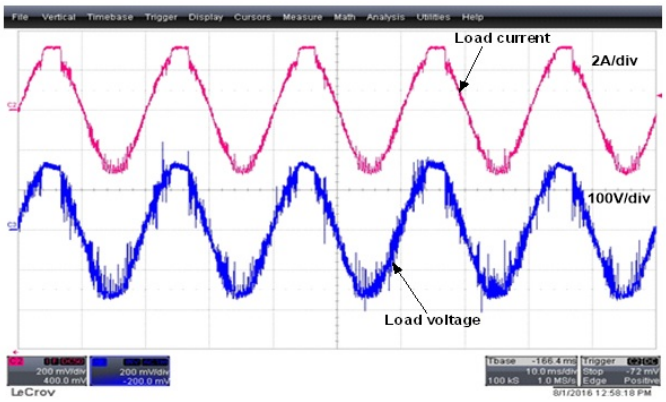
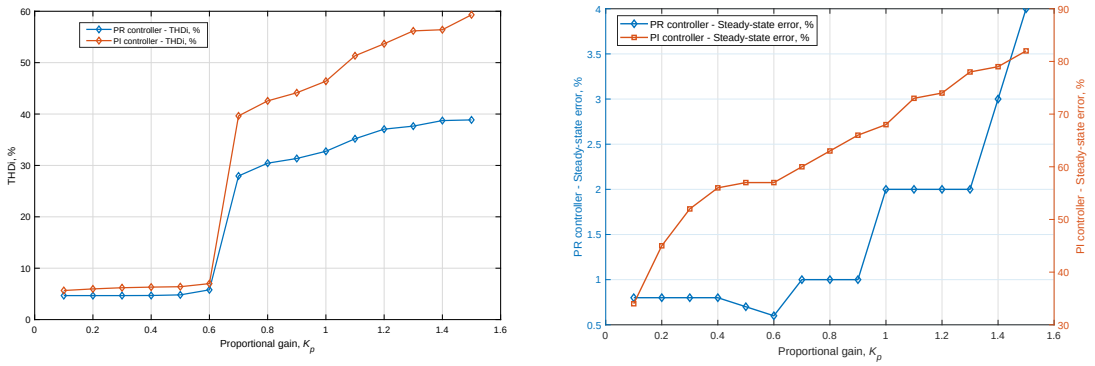


Figure 4.28: Experimental results of load current and load voltage using PI controller ($K_p = 0.7$ and $K_i = 200$).

and PR controllers when the value of K_p was increased from 0.1 to 1.5. The error value is below 1% for K_p between 0.1 and 0.6 for the PR controller. When the K_p value is increased beyond 0.6, the error value is increased. However, the error values for the PR steady state are still significantly lower than the PI controller steady state error.



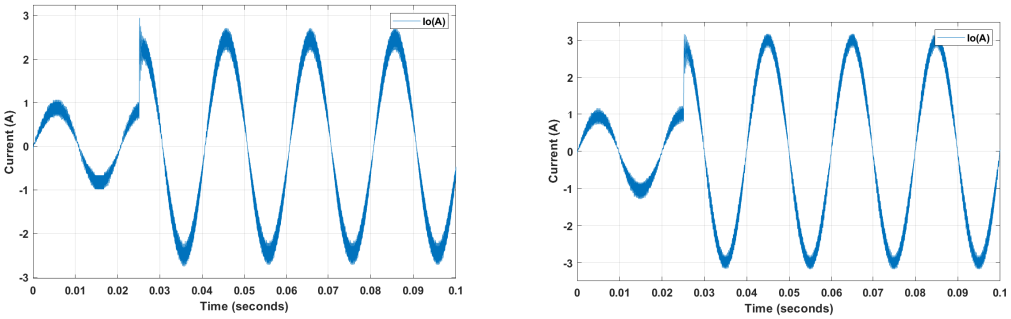
(a) THDi versus K_P **(b)** Steady-state error versus K_p

Figure 4.29: THDi and Steady-state error changes with the change in K_p for both PI and PR controller.

4.6.2 Transient response of PI and PR controllers

The transient performance is examined by applying a step change in the current reference during normal conditions. Figure 4.30 (a) and (b) shows the simulation

results for the step response in the load current using by the PI and PR controller, respectively. It can be seen that the PI controller is able to achieve a fast response to reach the steady-state condition, also the PR controller shows a fairly fast response and is comparable to the PI controller performance.



(a) Using by the PI controller **(b)** Using by the PR controller

Figure 4.30: Simulation results showing the transient response in load current.

Figure 4.31 shows the experimental results of transient response in the load current, controller output, and step signal when using the PI controller with $K_p = 0.5$ and $K_i = 200$. In all conditions, the current reference stepped from 1 A peak to 3.21 A peak. In each case, the results for the load current, controller output response, and step signal are shown in the figures.

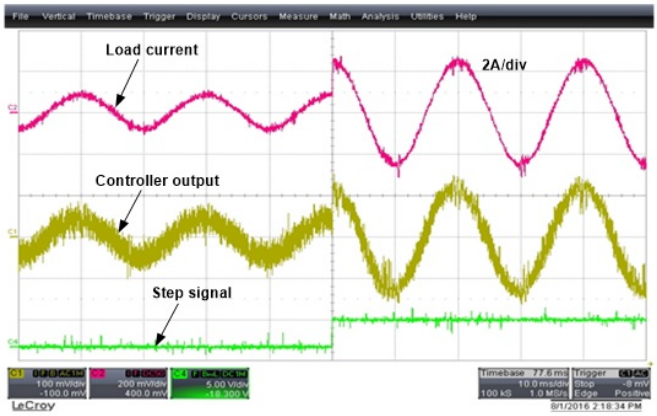


Figure 4.31: Experimental results showing the transient response in load current, controller output, and step signal using by the PI controller ($K_p = 0.5$, and $K_i = 200$).

From the analysis of transient response, the PI controller shows a reduced steady-state error when the value of K_p is increased from 0.5 to 0.7, and K_i is increased

from 200 to 300 as shown in Figure 4.32, but this leads to over modulation causing increased ripple in the load current.

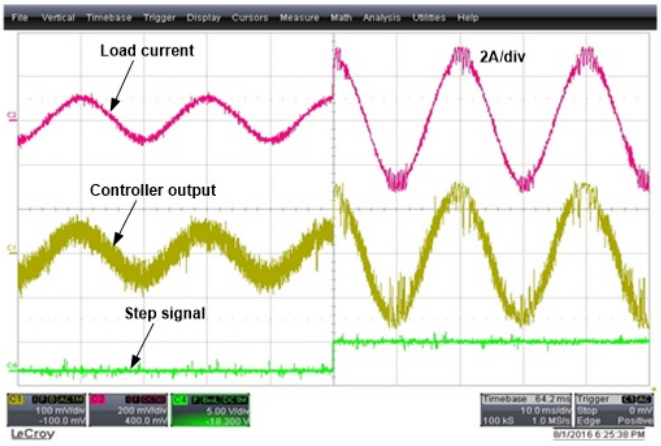


Figure 4.32: Experimental results showing the transient response in load current, controller output, and step signal using by the PI controller ($K_p = 0.7$, and $K_i = 300$).

Figure 4.33 shows the experimental results of the transient response in the load current using by the PR controller for $K_p = 0.5$, $K_i = 1000$. The transient response of PR controller is slightly slower where it takes a few cycles to reach the steady-state condition. But, it produces higher output quality with very low current harmonics as compared to PI controller with high distortion especially at both positive and negative peak of the load current. This is also reflected by the smooth controller output response in PR as compared to that of PI controller shown in the figures.

For each case, the system is tested under different values of K_p, and K_i. It can be seen from the step response analysis that the controller response is faster when the K_p, and K_i are increased to 0.7, and 2000, respectively. Increasing the K_p and K_i to a higher value will cause more distortion as more harmonic components around the fundamental frequency are included as shown in Figure 4.34.

4.7 Summary

Discrete PI and PR controls are commonly used in UPS inverters. According to the IEEE 1547 standard, minimum total harmonic should be maintained to less than 5%. In this chapter demonstrate that the performance of these controls in terms

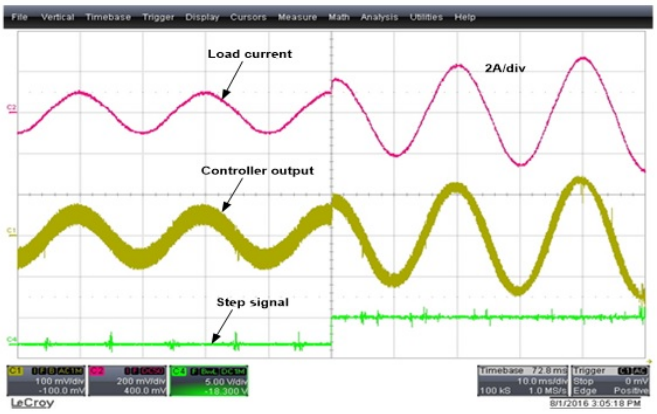


Figure 4.33: Experimental results showing the transient response in load current, controller output, and step signal using by the PR controller ($K_p = 0.5$, and $K_i = 1000$).

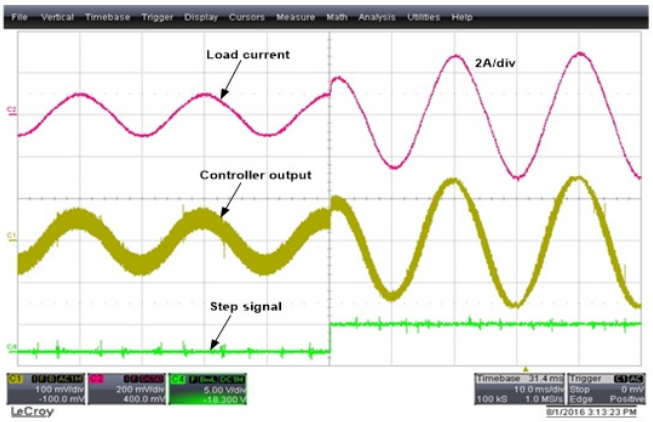


Figure 4.34: Experimental results showing the transient response in load current, controller output, and step signal using by the PR controller ($K_p = 0.7$, and $K_i = 2000$).

of current total harmonic distortion (THDi), transient response and steady state error can be improved. In case of THDi, demonstrate that the PI controller can only go down to 6.37%, while low order current harmonics being attenuated and the measured 3^{rd} and 5^{th} order harmonics are 0.52% and 0.24%, respectively. On the other hand, current THD for the PR controller is 4.03% with low order current harmonics are also attenuated and the measured 3^{rd} and 5^{th} order harmonics are 0.35% and 0.22%, respectively. These results demonstrate a significant improvement in current THD by the PR controller, with a 2.34% reduction. These improvements are achieved by tuning the controllers' parameters such as proportional gain, integral gain and cut-off frequency, also the LC parameters of filter. This is demonstrated

through the analysis, design and implementation of both PI and PR current control in single-phase UPS inverter applications and verified through simulations and experiments measurements.

Chapter 5

Conclusions and Future Work

This chapter summarises the research work the author has undertaken over the course of the PhD. Potential future work that builds upon this thesis is also discussed.

5.1 Conclusions and Contribution Summary

High voltage gain DC-DC boost converters are widely considered as the noteworthy part of the vast renewable energy and several other applications. In this research contributes to provide a high frequency high efficiency GaN-based cascade FB DC-DC boost converter to achieve high voltage step-up ratio with higher efficiency, and optimisation of current control parameters for single-phase UPS inverter. Specifically, this research deals with a wide band gap DC-DC converter, DC-AC inverter, and current controls for power applications. Their circuit operating principles, steady-state analysis, design, and control techniques have been explained. The proposed converters offer lower voltage stress of the active and passive devices and has no effect on the number of voltage multiplier cascaded stage changes. Furthermore, requirement of reduced boost inductance and cascaded capacitance ensures the compactness and lower cost. Moreover, the lower voltage stress both on the active and passive devices leading to compact size and facilitates the use of lower rating components. In addition, it also provides low output voltage ripple. A PWM control strategy of two independent frequencies and variable duty cycle has been proposed and implemented for the proposed converters. Between these two frequencies, the higher frequency minimises the size of the inductor while the other one operates at a relatively low frequency according to the desired output voltage ripple. However,

advanced current control such as PR offers low THD, better dynamic responses for UPS inverter. In addition, the PI and PR control parameters have been optimally tuned using both phase margine Bode plot and auto optimisation process. Moreover, the optimised parameters of the proposed converter and controls are simulated and compared in MATLAB/Simulink software, result in a significant reduction in the developmental time and cost of the switching system. The proposed step-up converter is especially suitable for variable input low voltage system such as PV, FC, etc.

5.2 Recommendation for Future Research

Future work can be carried out for the proposed converter and control as follows:

- The proposed converter can be experimentally implemented by using both the SiC and GaN devices for comparison purpose.
- The proposed converter is best suited for maximum output loads of 500 W. Research can be furthered to see if the load range extended by paralleling converters and see how efficient the proposed converter approach would be.
- MPPT technique can be combined with the proposed converter particular which can have unique application in PV power sources.

Appendix A

MATLAB Code

This appendix presents some MATLAB code for frquency response of both open loop and closed-loop transfer function using PI and PR controller.

A.1 Matlab Code for Frequency Response Analysis

```
clear all;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%  Matlab code for frequency response analysis of PI and PR
   controller

%  Mohammad Parvez

%  The University of Adelaide

%  Date: 20 July 2021

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%-------------------------------------------------------------------
--------------------------------------------------------------------

%%% 1. Open Loop Frequency Response Analysis for ideal PR Controller

%%------------------------------------------------------------------

% Defined controller parameters
Kp = 0.5;     % Proportional gain constant
Ki = 200;     % Integral gain constant for PI controller
Ki = 1000;    % Integral gain constant for PR controller
wo = 2*pi*50;  % Angular frequency
wc = 0.1;      % Cutt-off frequency
num = [0.5 2000 49348];  % Numerator of transfer function
den = [1 0 98696];       % Denominator of transfer function
G = tf(num, den);   % Transfer function of ideal PR  controller
bode(G),grid
```

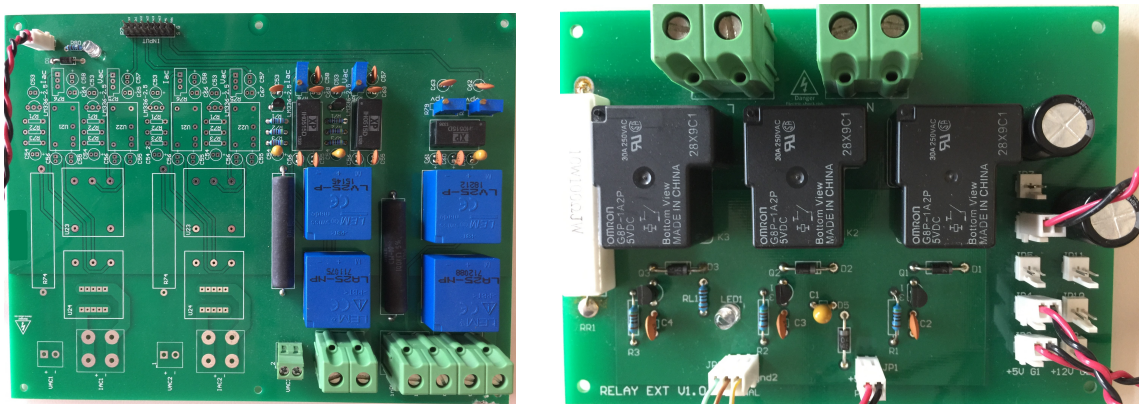
```
%%% 2. Open Loop Frequency Response Analysis for non-ideal PR Controller
       Using Selected Values

%%-------------------------------------------------------------------------

% Defined controller parameters
Kp = 0.5;     % Proportional gain constant for non-ideal PR controller
Ki = 1000;    % Integral gain constant for non-ideal PR controller
wo = 2*pi*50;  % Angular frequency
wc = 0.1;      % Cutt-off frequency
num = [0.5 200.1 49348];  % Numerator of non-ideal transfer function
den = [1 0.2 98696];      % Denominator of non-ideal transfer function
G = tf(num, den);         % Transfer function of non-ideal PR controller
bode(G),grid


%%% 3. Open Loop Frequency Response Analysis for non-ideal PR Controller
       Using Auto Optimization Values

%%-------------------------------------------------------------------------

% Defined controller parameters
Kp = 0.4856;       % Proportional gain constant
Ki = 14164;        %Integral gain constant
wo = 2*pi*50;      % Angular frequency
wc = 0.1;      % Cutt-off frequency
num = [0.4856 2832.89712 47926.79897]; % Numerator of transfer function of
non-ideal PR controller
den = [1 0.2 98696];  % Denominator of transfer function of non-ideal PR
controller
G = tf(num, den);      % Transfer function of non-ideal PR controller
bode(G),grid


%%% 4. Frequency Response of Closed-Loop Transfer Function Using PI and PR
       Controller

%%-------------------------------------------------------------------------

num1 = [0 0 0.5 200];         % Numerator of closed-loop PI controller
den2 = [1.1e-9 1e-4 1.5 200];  % Denominator of closed-loop PI controller
G_PI= tf(num1, den2);        % Closed-loop transfer function of PI controller
num3 = [0 0 0.5 200.1 49298];  % Numerator of closed-loop PR controller
den4 = [1.1e-9 1.0000022e-4 1.5001284 210.1596 147994];  % Denominator of
closed-loop PR controller
G_PR= tf(num1, den2);      % Closed-loop transfer function of PR controller
G = tf(G_PI, G_PR);   % Frequency response of closed-loop PI and PR controller

bode(G),grid
```

```
%%% 5. Frequency Response of Closed-Loop Transfer Function of PI and
       PR Controller Using Auto Optimization
%%-----------------------------------------------------------------

% Defined controller parameters
Kp = 0.4856;     % Proportional gain constant
Ki = 14164;      % Integral gain constant for PI controller
wo = 2*pi*50;    % Angular frequency
wc = 0.1;        % Cutt-off frequency

% Defined filer parameters and load resistor

Lf = 5 mH;      % Filter inductor
Cf = 0.22 uF;   % Filter capacitor
RL = 50 Ω;      % Load resistor

% Defined co-efficients of denominator for PR controller
λ4 = 1.1e-9;
λ3 = 1.0000022e-4;
λ2 = 1.485728;
λ1 = 2842.96672;
λo = 146622.7776;

% Defined numerator and denominator of closed-loop PI and PR
  controller

num1 = [0 0 0.4856 14164];  % Numerator of closed loop PI controller
den2 = [1.1e-9 1e-4 1.4856 14164]; % Denominator of closed
loop PI controller
G_PI = tf(num1, den2); % Closed-loop transfer function of PI controller
num3 = [0 0 0.4856 2832.89712 47926.7776]; % Numerator of closed loop PR
controller
num4 = [1.1e-4 1.0000022e-4 1.485728566 2842.96672 146622.7776]; %
Denominator of closed loop PR controller
G_PR = tf(num3, den4); % Closed-loop transfer function of PR controller
G = tf(G_PI, G_PR); % Frequency response of closed-loop PI and PR controller
bode(G),grid
```

Appendix B

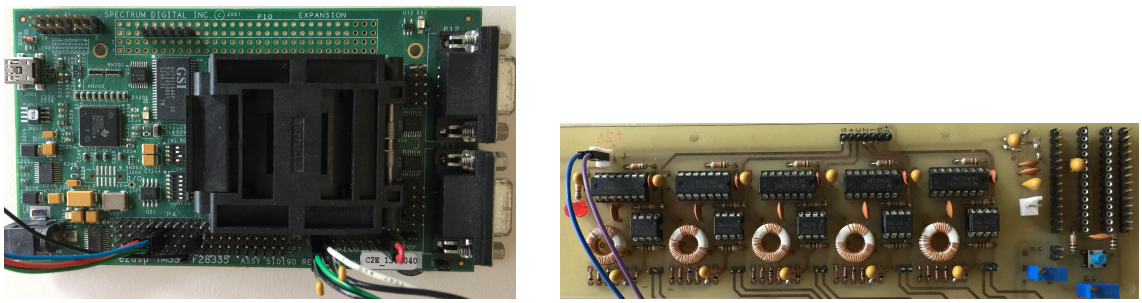
Hardware Configurations

The experimental tests have been implemented with the prototype illustrated in Chapter 4. The hardware prototype configurations are shown in Figures B.1 and B.2.



(a) (b)

Figure B.1: (a) Sensor circuit, and (b) Protection circuit.



(a) (b)

Figure B.2: (a) TMS320F28335 eZdsp development board, and (b) Gate driver circuit.

The voltage and current sensor are used to accurately sense the grid voltage and inverter output current as shown in Figure B.1 (a). The inverter output current is

sensed and fed back to a comparator which compares with reference current. The reference current is obtained by sensing the grid voltage. This is done to ensure the inverter output current is in phase with grid voltage. The phase-locked-loop (PLL) module is used to measurement the grid voltage.

To protect the inverter circuit against sudden overload or short circuit condition, an extra relay circuit can be added to limit the output current between the load and the generated output voltage as shown in Figure B.1 (b). An effective overcurrent limiter, the system can return to normal operation as soon as the fault is cleared.

For operating the structure of an IGBT/power MOSFET as a switch, a voltage sufficiently larger than the threshold voltage (V_{TH}) should be applied between the gate to source terminal. Consider a digital logic system with a Texas microcontroller/TMS320F28335 eZdsp development board that can output a PWM signal of 0 V to 5 V on one of its I/O pins as shown in Figure B.2 (c). This PWM would not be enough to fully turn on a power device used in power systems. Thus, an interface such as driver circuit is needed between the microcontroller and the power device as shown in Figure B.2 (d), which can be increased the PWM voltage level sufficiently around 7 to 8 V.

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Biography

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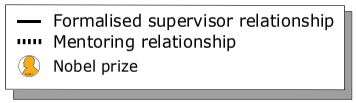
Scientifc Genealogy of Mohammad Parvez



1668 – MA, University of Cambridge, Isaac Newton

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