CURRENT IMPULSE DISPLACEMENT

THYRISTOR COMMUTATION

B.W. WILLIAMS Dip. Eng., B.Sc., B.E. (Hons.).

Being a thesis submitted

for the

Degree of Master of Engineering Science

in the

Department of Electrical Engineering

The University of Adelaide

September 1978

THE UNIVERSITY OF ADELAIDE Awarded February 1979

This thesis embodies the
results of supervised
project work which made up
All of the work for the degree.

DECLARATION

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university, and to the best of the author's knowledge and belief contains no material previously published or written by another person, except where due reference is made in the text of the thesis.

B.W.Williams

LIST OF PUBLICATIONS BY THE AUTHOR 1977-1978

1. "Impulse Commutated Thyristor Chopper."

IEE Proc., Vol. 124 No. 9 September 1977 pp 793-795

2. "State-Space Thyristor Computer Model."

IEE Proc., Vol. 124 No. 9 September 1977 pp 743-746

3. "State-Space Computer Triac Model."

IEE Proc., Vol. 125 No. 5 May 1978 pp 413-415

4. "Complete State-Space Digital Computer Simulation of Chopper Fed DC Motors."

IEEE Trans. Vol. IECI-25 No. 3 Aug. 1978 pp

5. "Asymmetrically Modulated AC Chopper."

to be published, IEEE Trans. Vol. IECI

6. & A.M. Parker "The Modelling of Thyristor Drives."

IEA Electric Energy Conference 1978 No. 78/3 pp 249-251

7. & A.L. Davis "Microprocessor Control of Inverter Drives."

IEA Microprocessor Systems Conference 1978 Pub. No. 78/

8. "Current-Impulse Commutated Thyristor Chopper."

to be published, IEE Proc.

ACKNOWLEDGEMENTS

The author is grateful to Dr. A.M. Parker of the University of Adelaide for his guidance and helpful discussions and suggestions during the research period and in the preparation of this thesis.

Thanks are also due to the Papua-New Guinea University of Technology, The University of Adelaide and The South Australian Institute of Technology for making available computing and experimental facilities during the research period.

The financial support of General Motors-Holden and the Electric Research Board is also gratefully acknowledged.

ABSTRACT

The thesis analyses and examines the theoretical and practical design aspects of a simple and efficient current-impulse displacement thyristor commutation technique of original design.

This commutation technique results in a thyristor chopper circuit which is inherently self priming, reliable and allows commutation after an "un-commutatable" overload current is reduced. The basic circuit is employed in different thyristor applications where forced thyristor turn-off is required, using both silicon controlled rectifiers and triacs. In each case, analytical results from the resulting circuits are shown to be in excellent agreement with experimental performance.

A three-phase inverter employing the above technique is shown to be an ideal vehicle for a microprocessor-based controlled-slip drive for an induction motor, and programming details for such a scheme are presented.

LIST of CONTENTS

contents :- continued

Chapter 2

a	damping coefficient, seconds^{-1}
C	commutation capacitance, uF
Dc	commutation diode
Df	freewheeling diode
Dr	energy return diode
E	direct current supply voltage, V
f	time constant, seconds
Ia	instantaneous load current, A
Ic	instantaneous capacitor current, A
Im	maximum load current, A
L	commutation inductance, uH
P	commutation cycle interval
R	representative of circuit losses, ohms
Ta	auxiliary bypass element
Tc	commutation circuit thyristor
Tm	main bypass circuit thyristor
t	instantaneous time, seconds
tq	thyristor circuit turn-off time, us
Va	load voltage, V
Vc	capacitor voltage, V
Vo	boost voltage, V
w	damped frequency, rad/sec
wo	natural resonant frequency, rad/sec
Xc	capacitive reactance, ohms
XL	inductive reactance, ohms
Zo	characteristic impedance, ohms
Ø	phase delay angle
π	pi, 3.14159

a	phase turn-on delay angle
b	phase turn-off angle before π
Em	peak supply voltage, V
Es	rms supply voltage, V
Ia, Ib	boundary load current levels, A
Iai, Ibi	ith Fourier load current component, A
Io	maximum load current, A
Is	supply current, A
i	instantaneous load current, A
Isa1, Isb1	fundamental supply current Fourier components, A
Isrms	rms supply current, A
Q	load Q
Tc	commutation triac
Tf	freewheeling triac
Tm	main bypass triac
Ts	circuit set triac
Z	fundamental load impedance, ohms
ZL	harmonic load impedance, ohms
Vai, Vbi	ith Fourier load voltage component, V
Vo	load voltage, V
cos u	supply displacement factor
k	supply power factor
η	load efficiency
y	supply distortion factor
R, L	load circuit, ohms & Henries
n	integer
w	supply frequency, rad/sec
tq	Triac circuit turn-off time, us
Øi	phase angle of ith harmonic

Tci	ith commutating bridge thyristor
Tc,even	commutation thyristor, for i even
Tc,odd	commutation thyristor for i odd
Tmi	ith main bridge thyristor
Ts	commutation circuit set thyristor
t	time, seconds
tq	thyristor circuit turn-off time, us
Vrn	line to neutral output voltage, V
Vry	line to line output voltage, V
w	fundamental frequency

CHAPTER 1

INTRODUCTION

Alternating current sources allow natural commutation of a conducting thyristor when the principal anode current decreases to zero each half cycle. In direct current applications, a conducting thyristor must be force commutated and it is in the method of commutation that the distinguishing features exist between the various power thyristor direct current chopper or inverter circuits.

Two basic thyristor commutation techniques [1] exist for circuits operating from direct current sources:

i. applied reverse voltage commutation, and

ii. current impulse displacement commutation.

In both methods an inductor-capacitor auxiliary circuit - called the commutation circuit - supplies load energy bypassing the main conducting thyristor thereby allowing it to regain a high impedance blocking state after reverse recovery.

Chapter 1
Introduction

Current impulse displacement commutation occurs if a conducting thyristor's principal current is reduced to zero by a bypassing current pulse of sufficient magnitude and duration to allow turn-off.

Applied reverse voltage commutation occurs if a conducting thyristor is reverse biased by a voltage pulse of sufficient duration to allow reverse recovery and then turn-off.

Both commutation techniques exhibit certain inherent electrical features.

Features of current impulse displacement commutation include a short and efficient commutating cycle, allowing a high operating frequency and wide control on the output voltage range. The use of feedback diodes yields circuits which provide inherently good output voltage regulation and the ability to handle wide variation in load magnitude and frequency. These diodes increase efficiency, enabling reverse power flow when the load is overhauled.

The frequency of the current pulse used for commutation is the same over the full load range, thereby allowing accurate specification of commutating component requirements. Characteristically, the commutating capacitor voltage is increased in proportion to the load current and the value of this capacitor and the commutating inductor may be chosen to optimise a given set of rating and cost constraints.

The mean current imposed on the commutation circuit semiconductors is low in comparison with the maximum load current and current rating selection need only be based on peak current ability.

A penalty incurred by current impulse displacement commutation is high thyristor dv/dt dynamic stress. Immediately after thyristor turn-off, imposed re-applied dv/dt levels can cause false turn-on, unless controlled by snubber circuits.

One of the inherent features of applied reverse voltage commutation is the control of imposed re-applied dv/dt stress levels. The high reverse voltage applied to achieve turn-off is conducive to shorter circuit turn-off time, at the sacrifice of large uncontrolled reverse recovery current.

Undoubtedly, the applied reverse voltage commutation technique is unsurpassed in low supply voltage applications [2], where smaller capacitance values are required. No capacitor voltage boosting is produced by these circuits and no power reversal is possible as would be required for motor regeneration.

Both commutation methods share the disadvantage of high initial di/dt stressing at main thyristor turn-on, but this can be remedied by one or more of the following techniques:

i. employing a hard, low impedance gate drive.

ii. using fast recovery diodes in the commutation circuit and for the freewheeling diodes.

iii. adding a saturable reactor in series with the stressed device.

Methods have been proposed to reduce disadvantages or incorporate desirable features of both basic techniques. Jones [3] uses an applied reverse voltage commutation technique which facilitates capacitor voltage boosting dependent on load current magnitude; and Humphrey [4] combines various inverter circuit techniques in order to incorporate wanted features.

The author has not attempted to define which is the better basic approach but has developed a novel current impulse displacement commutation technique [5], which is presented in Chapter 2. This commutation technique developed as a result of an investigation seeking a thyristor commutation method that would be suitable to both triacs and silicon controlled rectifiers, and yet be adaptable to any general application where forced thyristor commutation was required. The commutation technique forms the basis and linking element of the chapters to follow.

The basic commutation circuit is suitable for implementation in silicon controlled rectifier circuits as developed in Chapter 2 on the direct current silicon controlled rectifier chopper and Chapter 4 on the variable frequency silicon controlled rectifier inverter. The same commutation technique is implemented in a triac circuit as presented in Chapter 3 on the alternating current triac chopper.

In the case of the variable frequency inverter, the relevant chapter also includes details of its use in a microprocessor-controlled induction motor drive.

Each chapter in this thesis is based on a seperately published paper by the author. This natural segmentation allows the following chapter format to be used:- firstly the main text, then the references, followed by the appendix and finally all diagrams as lift-out figures at the end of that chapter. This format affords the convenience of direct observation of all figures while reading any section of that chapter. For the sake of continuity, the reading of the appendix to each chapter can be omitted.

REFERENCES

1 G.E. "SCR Manual" 5th. Edition 1972
Chapter 13, pp 351-408.

2 MAZDA F.F., "Thyristor Control" 1973
Newnes-Butterworths. Chapter 5, pp 94-105.

3 G.E. "SCR Manual" 5th. Edition 1972
Chapter 13, pp 369-382.

4 HUMPHREY A.J., "Inverter Commutation Circuits"
IEEE Trans. Vol. IGA-4, pp 104-110, Jan./Feb. 1968.

5 WILLIAMS B.W., "Impulse-commutated Thyristor Chopper",
IEE Proc. Vol. 124 No. 9 Sept. 1977 pp 793-795.

CHAPTER 2

A d.c. THYRISTOR CHOPPER

This chapter discusses a direct current thyristor chopper [1] which employs an L-C series resonant circuit in parallel with the load to provide a current impulse which will force commutate the main conducting thyristor. The circuit exhibits the usual features associated with current impulse displacement commutation, as well as the unusual inherent properties of self-priming and commutation after an "un-commutatable" overload current is reduced.

The rigorous mathematical derivation of all equations of this chapter is presented in the appendix at the end of the chapter.

2.1 BASIC CIRCUIT and OPERATION

The basic circuit of a current impulse commutated d.c. thyristor chopper is shown in the lift-out figure 2.1 at the end of this chapter, and the associated commutation capacitor voltage and current waveforms revealing three distinct cycle intervals are given in figure 2.2.

In the analysis of this chapter, the following electrical assumptions are made:

i. The load current is constant during commutation; this implies that the commutation period is small compared with the electrical load time constant.

ii. Source impedance is neglected and therefore does not affect the L-C circuit resonant frequency or time constant.

iii. Commutation circuit losses can be accounted for by including resistance R into the L-C circuit analysis.

iv. Thyristor turn-on is instantaneous.

v. Current flow through the voltage source is reversible.

The first commutation cycle occurs without capacitor voltage boosting and is therefore analysed separately from the subsequent voltage boosted cycles.

2.1(a) First Cycle Operation

The main thyristor Tm is conducting a load current Ia with the supply voltage E applied across the load. The commutation capacitor C holds no charge.

Period "P1" :

The commutation cycle is initiated by triggering the commutation thyristor Tc which allows a voltage across C to build sinusoidally. The capacitor voltage at any time t is given by

$$Vc(wt) = E*\{1 - (wo/w) \exp(-at) \cos(wt-\emptyset)\} \qquad (2.1)$$

where $a = R/2*L$

$w = \text{sqrt}(wo^2 - a^2)$

$wo = \text{sqrt}(1/L*C)$

and $\emptyset = \arctan(a/w)$

The commutation thyristor and capacitor current is given by

$$Ic(wt) = -\{E/XL\} \exp(-at) \sin(wt) \qquad (2.2)$$

where $XL = w*L$

When the current reduces to zero as the capacitor attains a maximum voltage of almost 2*E, thyristor Tc blocks and current oscillation continues through the diode Dc into the load.

Gradually the capacitor current builds up to exceed the magnitude of the load current and the current through the main thyristor decreases to zero. The L-C resonant circuit current in excess of the load current Ia is diverted through the return diode Dr to the supply thereby applying a reverse bias voltage across the main thyristor. The return diode must conduct this excess current for a period long enough to provide the necessary recovery time to allow the main thyristor to attain forward blocking capability.

Period "P2" :

The load, via the main thyristor, is now isolated from the supply and the capacitor maintains the constant load current. In achieving this the load is clamped to the capacitor voltage, which falls linearly to zero at a rate dependent on the magnitude of the load current.

Period "P3" :

When the capacitor voltage reaches zero the energy stored in the magnetic field of the commutation inductor L will transfer to C in the form of a voltage that will assist the next commutation cycle.

The capacitor voltage and current change according to $Vc(wt) = -\{Ia*Xc\} \exp(-at) \sin(wt)$ (2.3)

and $Ic(wt) = \{Ia*(wo/w)\} \exp(-at) \cos(wt+\emptyset)$ (2.4)

for $0 \leq wt \leq \pi/2 - \emptyset$

where $Xc = 1/w*C$

As the L-C circuit current decreases from Ia, the load deficit is maintained through the freewheeling diode Df which clamps the load to zero volts.

Finally when wt = (π/2) - Ø the freewheeling diode conducts all the load current and the capacitor retains a voltage-

$$Vo = - Ia*Zo$$

where $Zo = sqrt(L/C)$

-ready for the next commutation cycle. The main thyristor may now be triggered to re-apply supply voltage to the load.

2.1(b) Capacitor Voltage Boosted Cycles

The capacitor will have retained a voltage Vo depending on the magnitude of the load current during the previous commutation cycle. Accordingly, subsequent circuit voltage and current magnitudes are increased, as shown in figure 2.2. The capacitor voltage and current waveforms for each of the three distinct periods are now defined by:

Period "P1" :

$$Vc(wt) = E + (Vo-E)*(wo/w) \exp(-at) \cos(wt-Ø) \quad (2.5)$$

$$Ic(wt) = \{(Vo-E)/XL\} \exp(-at) \sin(wt) \quad (2.6)$$

Period "P2" :

$$Vc(wt) = -IaXc*wt + Vc(t1) \quad (2.7)$$

where t1 is the time of Period P1.

The voltage across the load decreases linearly according to

$$Va(wt) = -Ia*(t + f)/C + Vc(t1) \qquad (2.8)$$

where $f = C*R$

Period "P3" : (as for the first cycle)

$$Vc(wt) = -\{Ia*Xc\} \exp(-at) \sin(wt)$$

$$Ic(wt) = \{Ia*(wo/w)\} \exp(-at) \cos(wt+\emptyset)$$

2.2 CIRCUIT COMPONENT VALUES and ELECTRICAL RATINGS

The optimum commutation pulse shape is that which requires least energy. This is satisfied when the peak resonant current is 1.5 times the maximum load current [2], whence $wo = 0.535*\pi/tq$, where tq is the main thyristor turn-off time.

2.2(a) Inductor and Capacitor Values

In satisfying the peak current requirement of equation (2.6) at $wt = 3*\pi/2$ for a maximum load current Im, the following no loss expressions and ratings for L and C result:

without boosting	with boosting	electrical rating
$Lmin=0.397tqE/Im$	$Lmax=1.188tqE/Im$	$2(E/Zo+Im)$ A p-p
$Cmax=0.893tqIm/E$	$Cmin=0.297tqIm/E$	$2(E+ImZo)$ V p-p

Both L and C have a low duty cycle. The voltage waveform magnitude is reduced if resistance losses are considered. The effect of circuit resistance losses in reducing peak current levels is shown clearly on the peak capacitor current waveform

magnitudes in figure 2.2. It is therefore important to use a high Q resonant circuit in order to achieve the maximum level of current commutation ability for a given set of L-C values.

2.2(b) Semiconductor Electrical Ratings

Figure 2.3 shows various circuit voltage and current waveforms and hence the necessary information for determining electrical requirements. Table 1 shows the electrical requirements of all circuit semiconductors, in particular forward and reverse voltages limits and initial di/dt stresses, peak and mean forward current.

	Voltage		di/dt		Current	
	forward	reverse	forward	reverse	peak	mean
Tm	E	≃0	-	E/L+Im*wo	Im	Im
Tc	E+Im*Zo	≃0	E/L+Im*wo		Im+E/Zo	≃0
Df	-	E	-		Im	Im
Dc	-	E+Im*Zo	E/L+Im*wo	-	Im+E/Zo	≃0
Dr	-	E	E/L+Im*wo	-	Im+E/Zo	≃0

TABLE 1

SEMICONDUCTOR ELECTRICAL REQUIREMENTS

As may be seen, the actual commutating circuit semiconductors may have low mean current ratings, provided peak circuit requirements are met. Thyristor re-applied dv/dt levels are not defined and the commutation thyristor Tc experiences the higher dv/dt stress.

2.3 GENERAL CIRCUIT PROPERTIES

Current impulse displacement commutation fosters circuit turn-off conditions which are conducive to reducing the main thyristor's rated turn-off time. The necessary recovery interval is significantly reduced because the conducting current is zero when the reverse bias is applied. Also the maximum reverse di/dt is controlled and relatively low, resulting in a low recovery charge which reduces the reverse recovery interval.

Since the main thyristor forward blocking voltage requirement is modest at E volts, a much higher thyristor dv/dt capability can be attained by choosing a thyristor with a higher breakdown voltage rating. This precaution, coupled with the use of a snubber circuit would provide ample protection against false turn-on due to too high a re-applied dv/dt.

The chopper circuit developed has the following inherent basic features:

i. The main thyristor:

(a) does not carry any current associated with the commutation cycle, so its current rating is determined solely by the maximum load current requirement,

(b) has low forward and reverse blocking voltage requirements,

(c) experiences controlled hole storage reverse currents,

(d) need not necessarily have a fast turn-off time.

ii. The commutation circuit thyristor has a low mean current rating, modest voltage requirements and may have a turn-off time of up to 1.866 times that of the main thyristor.

iii. Thyristor triggering requirements are simple and either a variable frequency or a fixed frequency variable mark-space ratio mode of operation is possible. The later type of control was employed for prototype evaluation, as shown in the circuit of figure 2.4.

iv. The return diode Dr enables power reversal into the supply if the load is overhauled, as well as during the commutation cycle.

v. The capacitor voltage increases with increased load current thereby aiding commutation. Between commutation cycles the energy stored by the capacitor is minimal and varies from near zero at low load current to a maximum of $L*Im^2/2$ at full load current. Thus

possible capacitor losses are minimized, thereby producing a high efficiency chopper.

vi. One snubber circuit across the commutation thyristor affords maximum protection against dv/dt failure for both thyristors. The initial di/dt requirement of the main thyristor is not influenced by snubber discharge, but the snubber capacitance should be negligible compared with the commutation capacitance value to avoid any significant charge transfer.

2.4 IMPROVED COMMUTATION PERFORMANCE

The single undesirable feature of the presented commutation circuit is the dependence of the commutation cycle time upon the load current magnitude. Equation 2.7 shows that the interval of period P2 is inversely proportional to the load current. That is, under very light load conditions the length of the tail of the commutation cycle is large and will reduce the output voltage regulation. This also severely limits the upper operating frequency since the main thyristor should not be triggered until period P2 is complete. Interval P3 need not be complete.

Figure 2.5 shows the effect of different load current levels on the commutation capacitor current tail waveform. Since the main thyristor will always have regained blocking capability for any load current level to Im at the time wt=3.3*tq, X on figure 2.5, the tail is of no consequence to successful circuit commutation operation and could be shunted by an auxiliary circuit. Then, not only will the length of the commutation cycle be fixed for all allowable load currents thus improving output regulation and upper operational frequency limit, but the capacitor voltage and hence commutating pulse can be built up to their maximum value, even under no load conditions. Thus subsequent cycles after the first, may commutate the maximum load current with maximum boosting on the capacitor, independent of the load or rate of change of load current.

One such auxiliary circuit appears in reference [1], but a simpler method exists as shown in figure 2.6. Here the transistor (or thyristor Ta) is turned-on for 0.933*tq seconds, 3.3*tq seconds after the commutation cycle has commenced, thus allowing the capacitor voltage to oscillate and reverse through the L-C resonant circuit formed. Under such conditions the capacitor voltage boost is theoretically, neglecting losses, E*(3-sqrt(5))/(3+sqrt(5)) volts.

Commutation is continuously attempted into open circuits and during overloads, with the current pulse at a maximum until the load is reduced and the commutation circuit regains control of the main thyristor.

2.5 PERFORMANCE RESULTS

The basic commutation technique presented has been incorporated in d.c. choppers, controlling loads in excess of 1.6kW. Typical load voltage and current oscillograms for an R-L load are shown in figure 2.7.

All circuit diodes need to be a fast recovery type. This significantly reduces commutation losses during diode recovery since with normal rectifying diodes the reverse recovery current may be high in relation to the magnitude of the load current and the recovery time may represent a significant portion of the commutation cycle. A fast recovery freewheeling diode also reduces initial di/dt stressing at main thyristor turn-on.

A main objective, while investigating the current-impulse displacement commuatation technique in d.c. chopper applications, was to assess its adaptability for direct current to three phase variable frequency inverter implementation. The basic features presented in this chapter are demonstrated by a successful 50kVA inverter, which uses the modified commutation technique, as detailed in chapter 4.

2.6 CONCLUSIONS on CURRENT IMPULSE COMMUTATION

The basic features of a current impulse displacement commutated thyristor chopper have been considered. The modified version of the basic chopper enhances these basic features as discussed.

Since the commutation circuit components have relatively low mean current ratings in comparison to the maximum load current to be commutated, and modest voltage ratings, the resultant chopper is cheap, small and light. The basic chopper is simple, efficient, reliable and extremely versatile.

Any imposed high dynamic stresses on semiconductors can be simply and effectively eliminated and the problems often associated with current impulse commutation in this area thereby removed.

REFERENCES

1 WILLIAMS B.W. "Impulse-Commutated Thyristor Chopper". IEE Proc. Vol. 124, No.9, Sept. 1977 pp 793-795.

2 BEDFORD B.D. and HOFT R.G. "Principles of Inverter Circuits". J.WILEY. Chapter 7. pp 165-230.

APPENDIX

2.7 MATHEMATICAL DERIVATION of

(i) Commutation Cycle Waveforms

(ii) L and C Component Values and Ratings

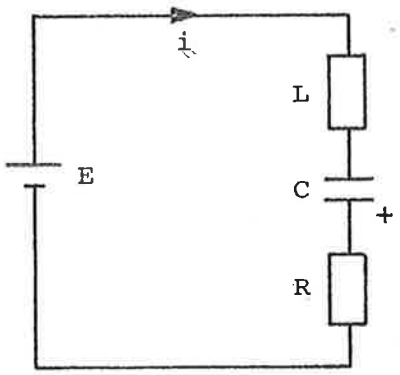
(a) without capacitor voltage boosting

(b) with voltage boosting

(i) Commutation Cycle Waveforms

The current impulse displacement commutation cycle may be treated mathematically as three distinct periods.

Period "P1" :



The capacitor is initially charged to Vo as shown. The initial circuit current is zero. The differential equation for the circuit of Period P1 is

$$E = L*di/dt + R*i + q/C$$

Where R represents commutation circuit losses.

The Laplace Transform of this differential equation is

$$E/s = L*\{s^2*q(s)-s*Qo-Q'o\} + R*\{s*q(s)-Qo\} + q(s)/C$$

solving for q(s) yields:

$$q(s) = \frac{E*C}{s} + \frac{[Qo-E*C]\ (s + 2*a)}{((s + a)^2 + w^2)}$$

where $w = \text{sqrt}(wo^2 - a^2)$

$wo = \text{sqrt}(1/L*C)$

$a = R/2*L$

The inverse Laplace Transform of q(s) yields the capacitor charge equation Q(t),

$$Q(t) = E*C + [Qo-E*C]*(wo/w)\ \exp(-at)\ \cos(wt-\emptyset)$$

where $\emptyset = \arctan(a/w)$

dividing Q(t) by capacitance C gives the capacitor voltage

$$Vc(wt) = E + [Vo-E]*(wo/w)\ \exp(-at)\ \cos(wt-\emptyset) \qquad (2.5)$$

For the first cycle when Vo = 0 for no voltage boosting

$$Vc(wt) = E*\{1 - (wo/w)\ \exp(-at)\ \cos(wt-\emptyset)\} \qquad (2.1)$$

The differential of Q(t) gives the capacitor current

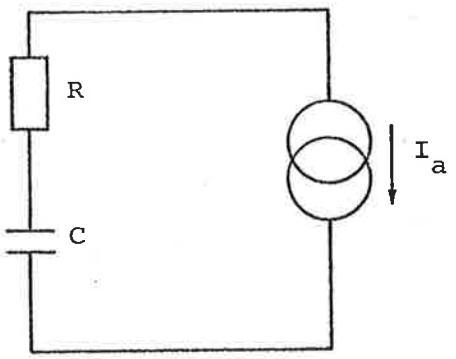
$$Ic(wt) = \{(Vo-E)/XL\}\ \exp(-at)\ \sin(wt) \qquad (2.6)$$

where $XL = w*L$

and the capacitor current for the first cycle is

$$Ic(wt) = -\{E/XL\}\ \exp(-at)\ \sin(wt) \qquad (2.2)$$

Period "P2" :



During this period of the commutation cycle, the capacitor maintains a constant load current, therefore the inductor supports no voltage, i.e.

$$Ic(wt) = Ia$$

Integrating the capacitor current gives the charge:

$$Q(t) = -Ia*t + Q(t1)$$

hence the capacitor voltage is

$$Vc(wt) = -IaXc*wt + Vc(t1) \qquad (2.7)$$

where $Xc = 1/w*C$

where t1 is the time of Period P1. The load voltage is given by

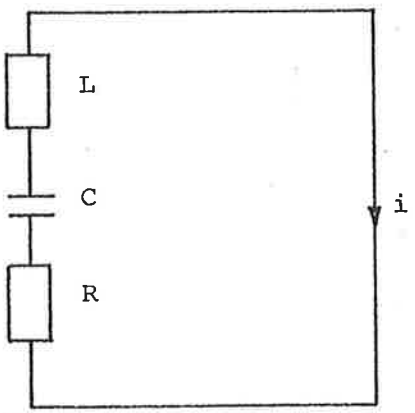
$$Va(wt) = Vc(wt) + Ia*R$$

hence

$$Va(wt) = -Ia*(t + f)/C + Vc(t1) \qquad (2.8)$$

where $f = R*C$

Period "P3" :



During this interval, the energy stored by the inductor is transferred to the capacitor. The inductor carries the load current Ia as an initial current. The capacitor holds no initial charge.

The differential equation for Period P3 is

$$0 = L*di/dt + R*i + q/C$$

The Laplace Transform of this differential equation yields q(s):

$$q(s) = -(Ia/w)\frac{w}{((s + a)^2 + w^2)}$$

The inverse Laplace Transform of q(s) gives the capacitor charge

$$Q(t) = -(Ia/w)\ \exp(-at)\ \sin(wt)$$

The capacitor voltage is given by dividing Q(t) by capacitance

i.e. $$Vc(wt) = -\{Ia*Xc\}\ \exp(-at)\ \sin(wt) \qquad (2.3)$$

where $$Xc = 1/w*C$$

The capacitor current is given by the differential of Q(t),

i.e. $$Ic(wt) = Ia*(wo/w)\ \exp(-at)\ \cos(wt+\emptyset) \qquad (2.4)$$

where $$\emptyset = \arctan(a/w)$$

The commutation capacitor waveforms are completely specified by equations 2.1 to 2.8

(ii) Determination of L and C values

The first commutation cycle occurs without any capacitor voltage boosting, hence the maximum load current that can be commutated during the first cycle will be less than subsequent cycles, as shown on figure 2.2. Hence distinct sets of commutating inductor L and capacitor C values will exist; without voltage boosting through to the case of maximum boosting.

(a) Assuming

i. Ipeak = 1.5*Im [2] then

$$\pi * \mathrm{sqrt}(L*C) = 1.866*tq \qquad (1)$$

ii. R = 0, hence exp(-at) = 1 and Xc = XL = Zo

The capacitor current waveform given by equation 2.2 becomes:

$$Ic(wt) = -(E/Zo)\ \sin wt$$

where $Zo = \mathrm{sqrt}(L/C)$

This equation for capacitor current must satisfy Ipeak = 1.5*Im at wt = $3*\pi/2$

i.e. $$1.5*Im = E*\mathrm{sqrt}(C/L) \qquad (2)$$

Solving (1) and (2) for L and C in terms of E, Im and tq yields:

$$Lmin = 0.397*tq*E/Im$$

$$Cmax = 0.893*tq*Im/E$$

(b) The maximum value of capacitor voltage boosting, ignoring losses, is -Im*Zo as given by equation 2.3 when wt = 0.5*π.

Substituting the boosting voltage value into equation 2.6 when wt = 1.5*π and Ic = 1.5*Im yields:

$$1.5*Im = (Im*Zo+E)/Zo$$

i.e. $$0.5*Im = E*sqrt(C/L) \quad (3)$$

Solving equations (1) and (3) for L and C again in terms of E, Im and tq yields:

$$Lmax = 1.188*tq*E/Im$$

$$Cmin = 0.297*tq*Im/E$$

which completes the set of L and C equations presented in section 2.2.

The maximum inductor current flows when wt = 0.5*π in equation 2.6. i.e. Ipeak = Im + E/Zo

The maximum capacitor voltage swing is from the maximum voltage boosting level, given by equation 2.3 when wt = 0.5*π, to the maximum voltage during commutation, given by equation 2.5 when wt = π:

$$\{Im*Zo\} + \{E + (E + Im*Zo)\}$$

i.e. Vc rating = 2*{E + Im*Zo}

The maximum commutation circuit di/dt stressing occurs when the differential of the commutation circuit current, equation 2.6, is evaluated at wt = 0, which gives:

di/dt max = E/L + Im*wo

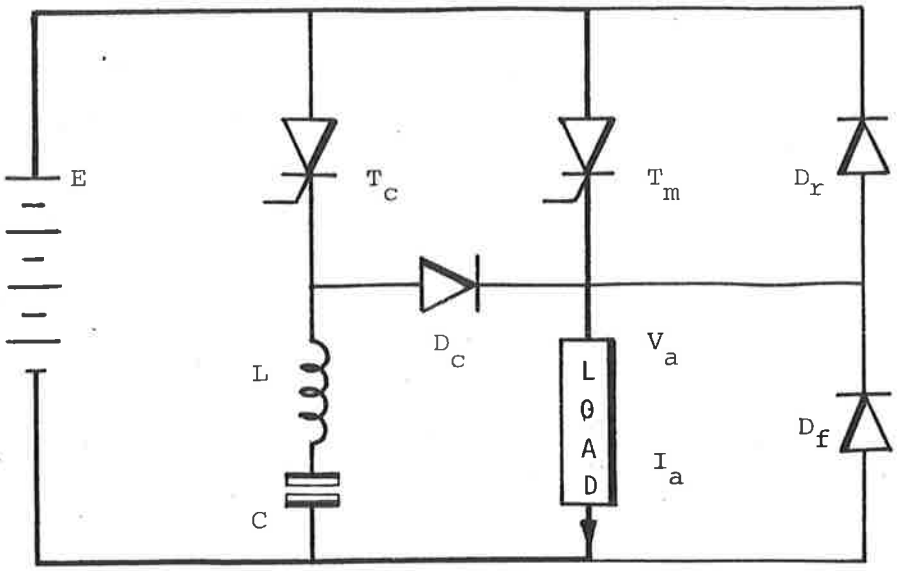


FIGURE 2.1 Basic Circuit

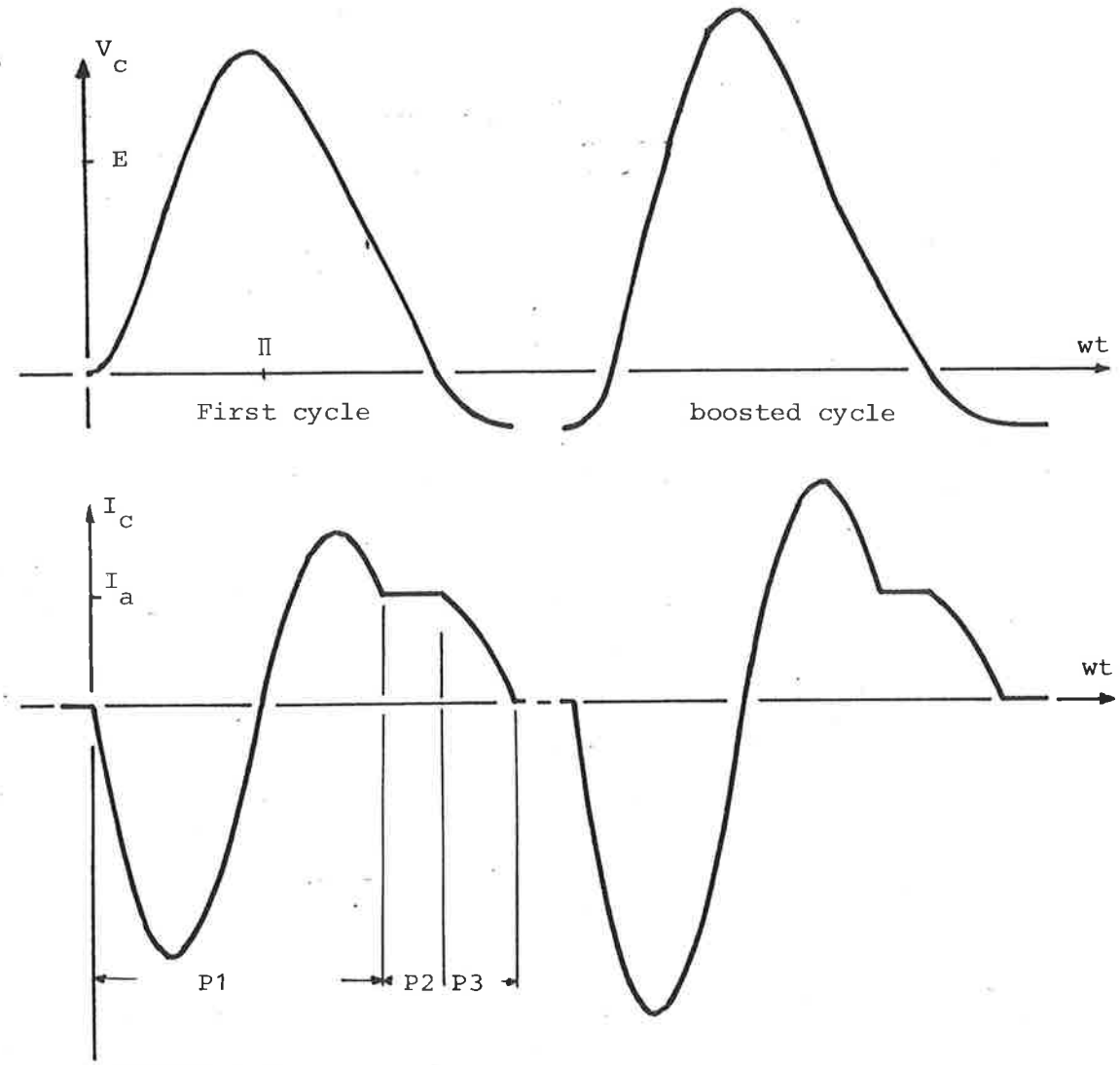


FIGURE 2.2

Commutation Capacitor voltage and current waveforms.

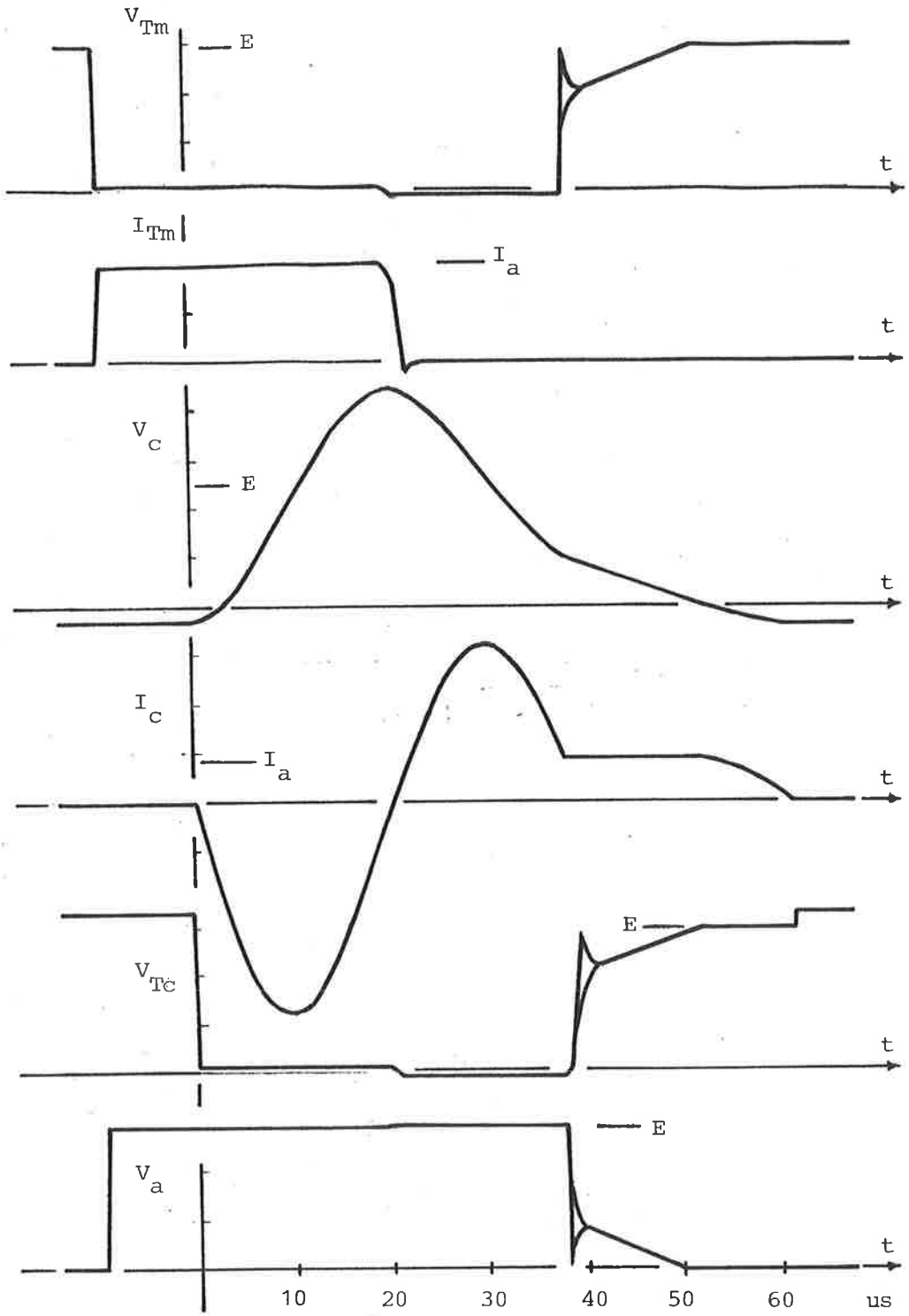


FIGURE 2.3

Chopper Circuit Waveforms

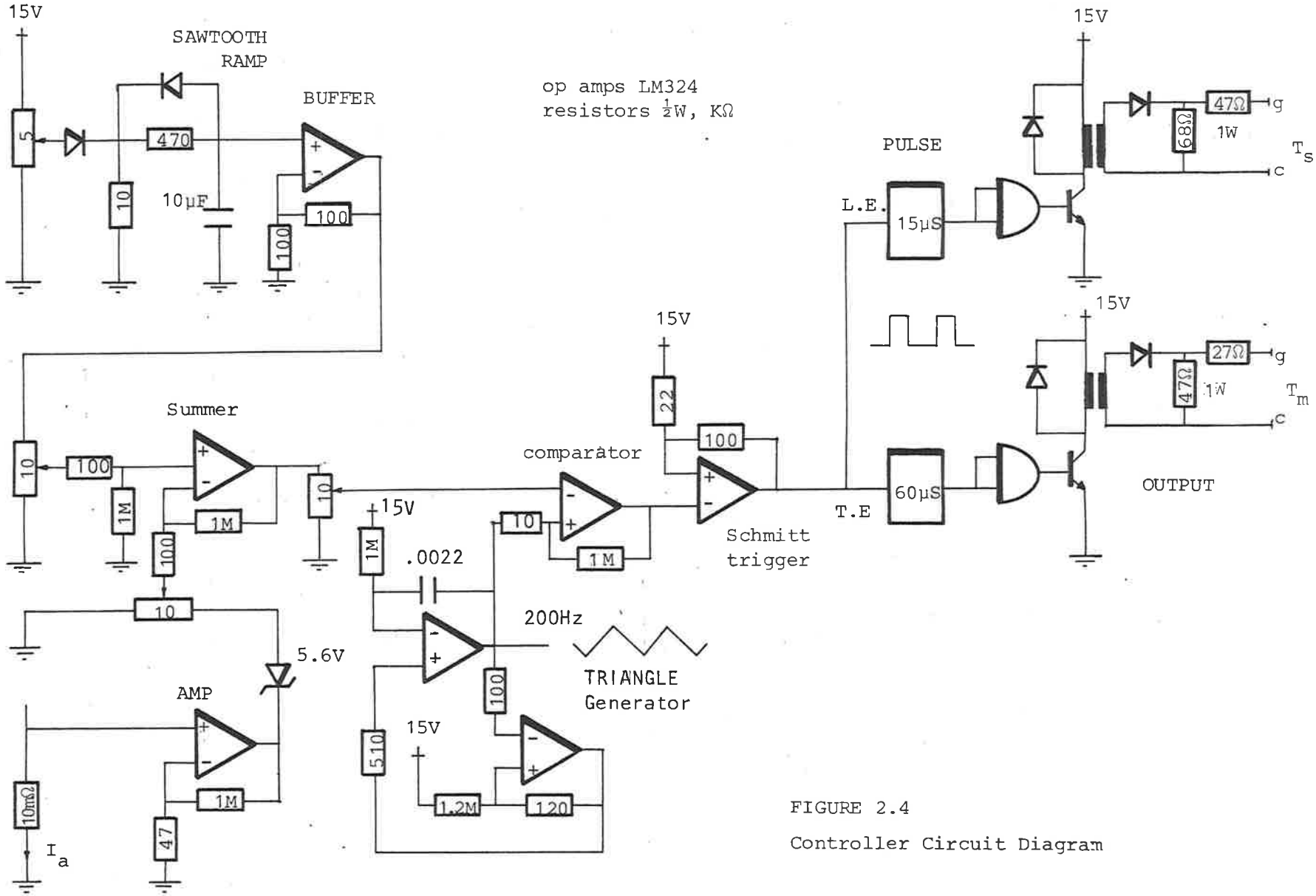


FIGURE 2.4

Controller Circuit Diagram

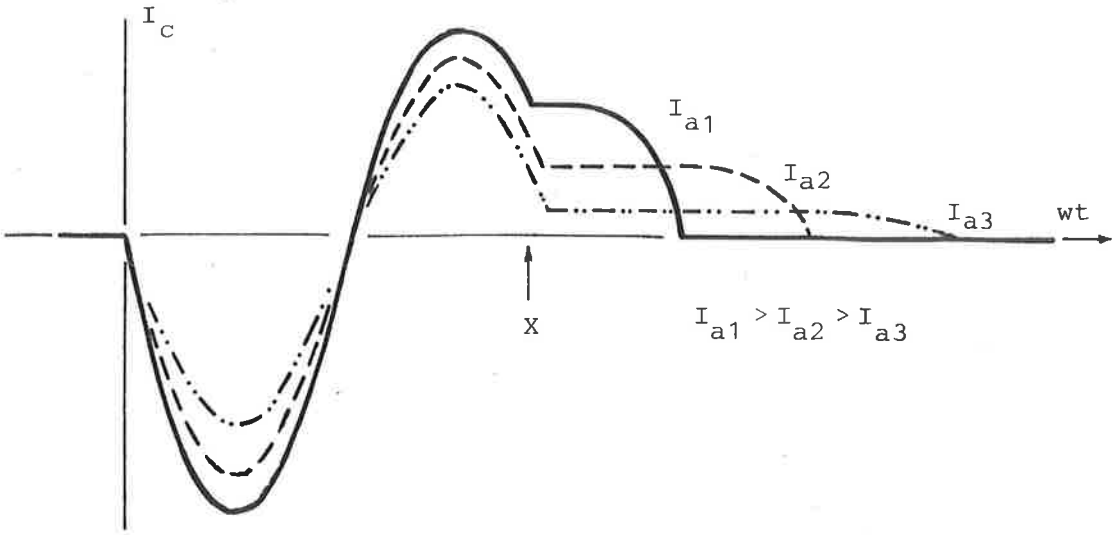


FIGURE 2.5 Load Dependent, Capacitor Current Tail

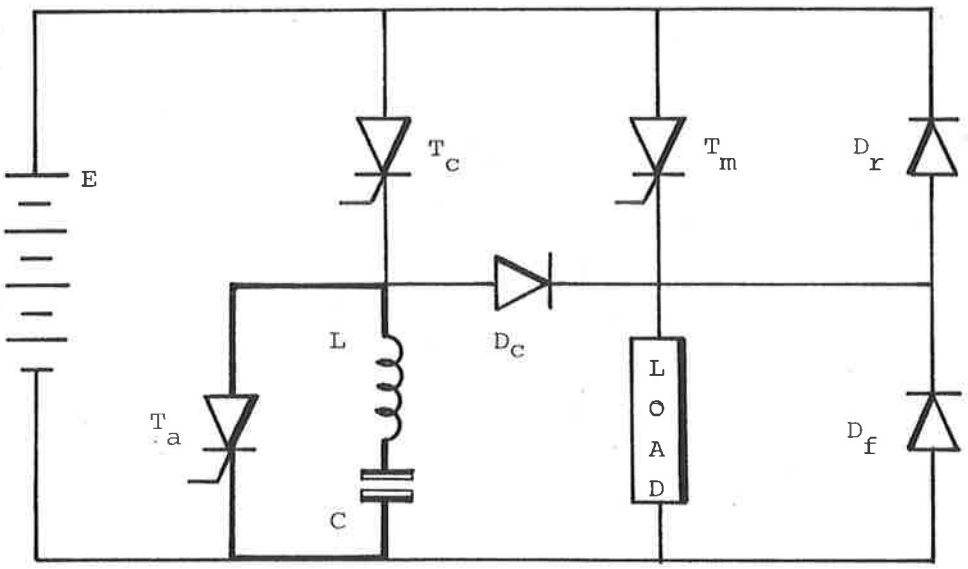
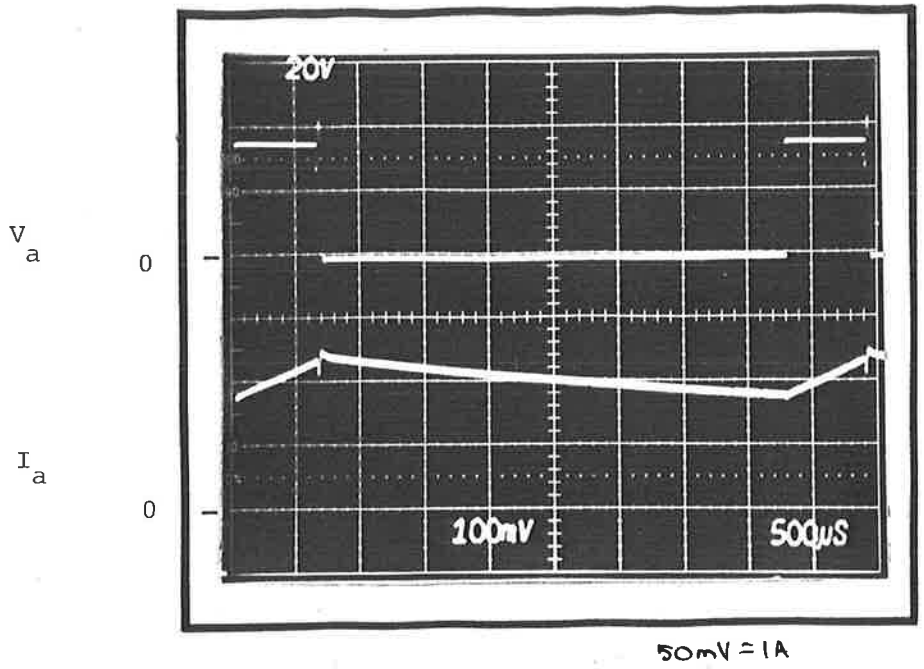


FIGURE 2.6 Commutation Speed-up circuit modification.



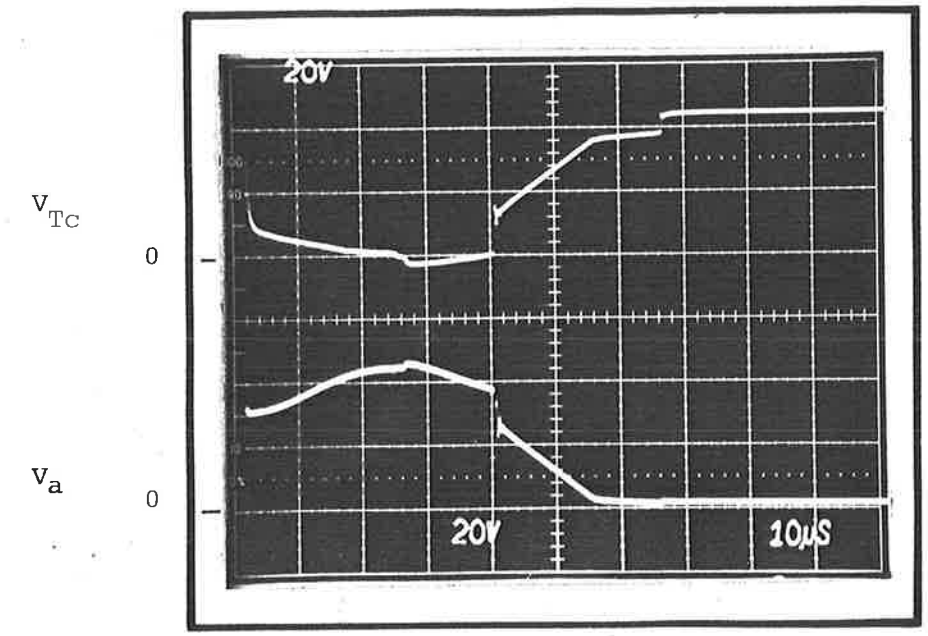


FIGURE 2.7

Chopper load oscillograms

CHAPTER 3

An a.c. TRIAC CHOPPER

This chapter describes the adaptation of the current impulse displacement commutation technique to a triac forced turn-off alternating current application. Commutation requirements of triacs are similar to those of silicon controlled rectifiers, except that triacs generally have lower static and dynamic electrical stress limits.

An alternating current triac chopper is employed to attain optimum supply power factor correction for any given reactive load, by selective chopping of the alternating current supply voltage waveform. This can result in improved displacement and distortion factors of the supply and also better load efficiency than conventional alternating current phase control techniques [1] [2] [3].

3.1 The ALTERNATING CURRENT CHOPPER and CIRCUIT OPERATION

The basic alternating current triac chopper circuit is shown in figure 3.1 and is employed to achieve an output voltage and hence current waveform as in figure 3.2. The L-C resonant circuit provides a current impulse which force commutates both the main triac Tm and the freewheeling triac Tf. For analysis, the 50 Hertz supply voltage Es is assumed a constant direct current voltage source during the relatively short commutation period. Circuit operation is similar to that of the previously analysed d.c. chopper and is as follows:

The main triac Tm is conducting a load current i , with the supply voltage Es applied across the load. The set triac Ts is triggered at the a.c. supply voltage peak value, Em, allowing the commutation capacitor C to charge to a maximum voltage 2*Em, then Ts blocks and turns-off.

To isolate the load from the supply, the commutating triac Tc is triggered, allowing C to discharge into the load. Gradually the sinusoidal capacitor current displaces the load current through the main triac, eventually reverse biasing Tm as C discharges at a constant rate into the load.

The freewheeling triac Tf is triggered $0.75*\pi*\mathrm{sqrt}(L*C)$ seconds after Tc, which allows C to discharge independent of the load current. With the capacitor current oscillation complete, Tc blocks and continuous triggering of Tf allows the load current to freewheel through Tf.

Triac Ts is fired to reset the commutating capacitor to a polarity that will enable the freewheeling triac to be force commutated by triggering Tc. Tc is fired π*sqrt(L*C) seconds before the main triac Tm is triggered to commence the next cycle.

Figure 3.3 shows typical circuit voltage and current oscillograms at various circuit nodes.

3.2 CIRCUIT PROPERTIES and COMPONENT ELECTRICAL RATINGS

The typical inherent features of current impulse displacement commutation as described in the previous chapters, are displayed by the basic circuit of figure 3.1. These included the properties of self-priming and no need of any special starting sequence. The commutation cycle current does not flow through the main triac, thus the current rating of Tm is determined and thus selected solely based on the maximum load current requirement.

The electrical requirements and ratings of the various circuit elements are primarily determined by the maximum load current level and the maximum capacitor voltage attained. The peak and hence maximum possible load current Io is Em/Z where Z is the load impedance at the fundamental supply frequency, while the maximum capacitor voltage attained is almost 2*Em.

3.2.1 Capacitor and Inductor ratings.

It has been shown in chapter 2.7 that the commutation components L and C, considering voltage boosting effects, are given by

$$Lmax \leq 1.188*tq*Z$$

$$Cmin \geq 0.293*tq/Z$$

where tq is the circuit turn-off time of the main triac Tm, such that $1.866*tq = \pi*sqrt(L*C)$.

3.2.2 triac electrical ratings

The main triac Tm must have an rms current rating of at least 0.7071*Io and a breakdown voltage rating in excess of 2*Em. The initial di/dt and re-applied dv/dt conditions are uncontrolled.

The freewheeling triac Tf requirements are similar to those imposed on the main triac. Both require snubber circuit protection against false dv/dt triggering effects.

The commutating triacs Ts and Tc both have a low rms current requirement and a voltage rating in excess of 2*Em, depending on the magnitude of the voltage across the commutating capacitor. Both triacs have a controlled initial di/dt condition of less than Em/L + Io/sqrt(L*C).

3.3 WAVEFORM ANALYSIS

Typical load and supply current and voltage waveforms are shown in figure 3.2. Since the load voltage waveform is not sinusoidal, load current harmonics result which reduce the load efficiency. Both load efficiency and resultant supply power factor can be determined mathematically, as outlined below. Consider the case of a delay turn-on phase angle "a" and delay turn-off phase angle "π - b". Firstly, the output voltage waveform is analysed to determine load efficiency and then the input current waveform is considered in calculating supply power factor.

The derivation of the mathematical expressions to follow are presented in the appendix at the end of this chapter.

3.3.1 Output Waveforms

The output voltage of the asymmetrical alternating current chopper shown in figure 3.2 is defined by

$$Vo = Em*\sin wt \qquad \text{for} \quad a \leq wt \leq \pi - b$$

$$\pi + a \leq wt \leq 2*\pi - b$$

$$= 0 \qquad \text{elsewhere :} \quad wt < 2*\pi \qquad (1)$$

The Fourier co-efficients of the output voltage are

$$Va1 = (Em/2*\pi)*(\cos 2*a - \cos 2*b) \qquad (2)$$

$$Vb1 = (Em/2*\pi)*\{2*(\pi-b-a) + \sin 2*a + \sin 2*b\} \qquad (3)$$

and

$$Van = \frac{Em}{\pi}\left\{\frac{\cos(n+1)a - \cos(n+1)b}{n+1} + \frac{\cos(n-1)a - \cos(n-1)b}{n-1}\right\} \quad (4)$$

$$Vbn = \frac{Em}{\pi}\left\{\frac{\sin(n+1)a + \sin(n+1)b}{n+1} - \frac{\sin(n-1)a + \sin(n-1)b}{n-1}\right\} \quad (5)$$

where n = 3,5,7..

The load current i, for a simple R-L load, may be evaluated by solving:

$$R*i + L*di/dt = Em*\sin wt \qquad \text{for} \quad a \leq wt \leq \pi - b$$

$$= 0 \qquad \text{for} \quad \pi - b < wt < \pi + a \quad (6)$$

with initial conditions $i(a) = Ia$ and $i(\pi-b) = Ib$ (7)

Equations (6) and (7) yield the solution

$$i = \{Ia - Io*\sin(a-\emptyset)\}*\exp((a-wt)/Q) + Io*\sin(wt-\emptyset)$$

$$\text{for} \quad a \leq wt \leq \pi - b \quad (8a)$$

$$= Ib*\exp((\pi-b-wt)/Q)$$

$$\text{for} \quad \pi - b \leq wt \leq \pi + a \quad (8b)$$

where $\emptyset = \arctan(Q)$

$Q = w*L/R$

$Io = Em/Z$

$Z = \sqrt{R^2 + w^2L^2}$

The boundary currents Ia and Ib may be solved, yielding

$$Ia = Io*\left[\frac{\exp(-\pi/Q)\sin(a-\emptyset) - \exp(-(a+b)/Q)\sin(b+\emptyset)}{1 + \exp(-\pi/Q)}\right] \quad (9)$$

$$Ib = -Ia*\exp((a+b)/Q) \quad (10)$$

The Fourier co-efficients for the load current harmonics are given by:

$$Ian = (Van/R)*\cos\emptyset n \text{ and } Ibn = (Vbn/R)*\cos\emptyset n \quad (11)$$

where $\emptyset n = \arctan(n*Q)$

The load current is thus given by:

$$i = \sum_n [Ian*\cos(n*wt-\emptyset n) + Ibn*\sin(n*wt-\emptyset n)] \quad (12)$$

where n = 1,3,5,

The load efficiency η can be defined as the ratio of the fundamental active power to the total active power, that is:

$$\eta = (Ia1^2 + Ib1^2) / \sum_n (Ian^2 + Ibn^2) \quad (13)$$

where n = 1,3,5,

For the case of a symmetrical load voltage waveform, a = b, the cosine term co-efficients become identically zero, whence

$$\eta = Ib1^2 / \sum_n Ibn^2$$

3.3.2 Supply Waveforms

The supply voltage waveform is assumed sinusoidal. The supply current waveform shown in figure 3.2 is defined by:

$$Is = [Ia-Io*\sin(a-\emptyset)]*\exp((a-wt)/Q) + Io*\sin(wt-\emptyset) \quad \text{for} \quad a \leq wt \leq \pi - b$$

$$= 0 \quad \text{for} \quad 0 \leq wt < a$$

$$\pi - b < wt < \pi + a \qquad (14)$$

The fundamental Fourier co-efficients of the supply current are given by:

$$Isa1 = (2/\pi)[A1*\{\exp(-a/Q)\cos(\emptyset+a) + \exp((-\pi+b)/Q)\cos(\emptyset-b)\} -(Io/2)*[(\pi-b-a)*\sin\emptyset+(1/2)*\{\cos(\emptyset+2b)-\cos(\emptyset-2a)\}]] \qquad (15)$$

$$Isb1 = (2/\pi)[A1*\{\exp(-a/Q)\sin(\emptyset+a) + \exp((-\pi+b)/Q)\sin(\emptyset-b)\} +(Io/2)*[(\pi-b-a)*\cos\emptyset+(1/2)*\{\sin(\emptyset+2b)-\sin(\emptyset-2a)\}]] \qquad (16)$$

where $A1 = [Ia - Io*\sin(a-\emptyset)]*\exp(a/Q)/\mathrm{sqrt}(1+1/Q^2)$

The supply displacement factor, distortion factor and power factor can be expressed in terms of the fundamental Fourier co-efficients of the supply. The displacement factor, cosu is the fundamental power factor, that is

$$cosu = \cos(-\arctan(Isa1/Isb1)) \qquad (17)$$

The ratio of real to apparent power is called total power factor, k

$$k = [\mathrm{sqrt}\{(Isa1^2 + Isb1^2)/2\}/Isrms]*cosu$$

$$= y*\cos u \qquad (18)$$

where y is called the distortion factor and is the ratio of the fundamental rms current to the total rms current, Isrms. The total rms current is given by:

$$Isrms^2 = (1/\pi)[-A1^2*((Q^2+1)/(2*Q))*(\exp(-2*(\pi-b)/Q) - \exp(-2*a/Q))$$

$$+2*A1*Io*[\exp(((-\pi+b)/Q)\sin b + \exp(-a/Q)\sin a]$$

$$+(Io^2/2)*[\pi-b-a + (1/2)*\{\sin 2*(a-\emptyset)+\sin 2*(b+\emptyset)\}]] \qquad (19)$$

These equations were used to derive the theoretical results to follow, and their complete mathematical derivation is given in the appendix 3.6 at the end of this chapter.

3.4 COMPARISON of CHARACTERISTICS

Digital computer analysis of the supply current results in the supply power factor characteristics shown in figure 3.4a. In particular, this figure enables a comparison between the resultant supply power factor attained for the a.c. phase control (b = 0) and symmetrical a.c. chopping (a = b). It is seen that input power factor levels in excess of the load fundamental power factor (a = b = 0) can be attained if symmetrical a.c. chopping is employed. Figure 3.4b shows the corresponding resultant improvement in load efficiency resulting from symmetrical chopping.

Generally, the supply power factor increases to a maximum with increasing phase angle "a" and then drops away. It would therefore be feasible that a set (a,b) exists that maximises the input power factor for a given load Q. To this end, iterative computer analysis yields figure 3.5, which for a given load Q gives maximum possible supply power factor for the computed optimum value set of "a" and "b".

The optimal set (a,b) produces only a slight improvement in maximum supply power factor when compared to the corresponding maximum power factor attained with symmetrical chopping (a = b). This small improvement in maximum supply power factor would not generally warrant the introduction of an asymmetrical a.c. chopper over the symmetrical a.c. chopper.

3.5 PERFORMANCE, APPLICATIONS and CONCLUSIONS.

A 1kVA control capability version of the basic a.c. chopper was used to control a 400W R-L load. The triggering and control circuitry is shown in figure 3.6. Load efficiency and supply power factor were measured for two different symmetrical chopping angles, and results correlated excellently with theoretically predicted values, as shown in table 2 to follow.

ANGLE a = b degrees	POWER input Watts	output	INPUT Esrms Volts	Isrms Amps	POWER FACTOR k pract	theor	EFFICIENCY η pract	theor
45	280	262.5	120	3.1	0.75	0.76	0.94	0.97
60	114	102.5	120	1.5	0.64	0.66	0.90	0.91

TABLE 2

RESULTS COMPARISON

A limitation of reliable operation is normally found in high power triac applications and can be due to poor triac dynamic electrical characteristics, in particular low re-applied dv/dt rating. Most other types of a.c. triac choppers [2] have been limited to low power applications, of the order of 20W. The presented commutating technique coupled with two antiparallel SCR's back to back instead of triacs would be most suitable for high power a.c. chopper applications of over 1kVA.

Such a chopper could then be employed industrially for adjustable supply power factor correction and improvement where electricity authorities imposed penalty rates for low power factor conditions. This power factor improvement would be traded for induced source harmonics.

In conclusion, an a.c. chopper will give an improved load power factor condition compared to an uncorrected load condition, while a symmetrical a.c. chopper gives improved load efficiency and supply power factor characteristics over conventional phase control. Marginal improvement in supply power factor is attained by employing an asymmetrical triggering version of the basic a.c. chopper. Load efficiency is not significantly reduced.

REFERENCES

1 WILLIAMS B.W., "Asymmetrically Modulated A.C. Chopper", to be published, IEEE Trans. Vol. IECI

2 REVANKAR G.N., et al. "Symmetrically Pulse Width Modulated A.C. Chopper"
IEEE trans. Vol. IECI-24, No. 1. Feb. 1977. pp 39-44.

3 KRISHNAMURTHY K.A. et al. "A.C. Power Control of an R-L load."
IEEE trans. Vol. IECI-24 No. 1 Feb. 1977. pp 138-141.

APPENDIX

3.6 MATHEMATICAL DERIVATION of

(i) LOAD EFFICIENCY

(ii) SUPPLY POWER FACTOR

The Fourier co-efficients for any function f(wt) can be determined by evaluating the following integrals

$$Vo = (1/T) \int_0^T f(wt)\ dwt$$

The cosine harmonic co-efficient terms are given by

$$Van = (2/T) \int_0^T f(wt)\ \cos(n*wt)\ dwt$$

while the sine harmonic co-efficients are

$$Vbn = (2/T) \int_0^T f(wt)\ \sin(n*wt)\ dwt$$

where T is the period of the function f(wt). These equations are used and evaluated extensively in the analysis to follow, where f(wt) = sin(wt) and T = $2*\pi$.

3.6(i) Determination of load efficiency.

The output voltage applied across the load, as shown in figure 3.2, is defined by

$Vo = Em*\sin wt$ for $a \leq wt \leq \pi - b$

$\pi + a \leq wt \leq 2*\pi - b$

$= 0$ elsewhere : $wt < 2*\pi$

The offset term Vo is given by evaluating

$$Vo = (1/2*\pi) \int_{a}^{\Pi-b} Em*\sin(wt)\ dwt$$

$$= (Em/2*\pi)*[\ -\cos wt\ ]_{a}^{\Pi-b}$$

$$= (Em/2*\pi)*[\cos(a)+\cos(\pi+a)-\cos(\pi-b)-\cos(2*\pi-b)]$$

$$= 0$$

The co-sine Fourier co-efficients result by evaluating

$$Van = (Em/\pi) \int \cos(n*wt)\ \sin(wt)\ dwt$$

$$= (Em/2*\pi) \int \{\sin((n+1)wt)+\sin((n-1)wt)\}\ dwt \quad n\neq 1$$

$$= -(Em/2*\pi)*\left[\frac{\cos((n+1)wt)}{n+1} + \frac{\cos((n-1)wt)}{n-1}\right]_{a}^{\Pi-b}$$

$$= \frac{Em}{2\pi}*\{1-\cos(\pi*n)\}*\left[\frac{\cos(n+1)a - \cos(n+1)b}{n+1} + \frac{\cos(n-1)a - \cos(n-1)b}{n-1}\right]$$

when n is even, $\{1-\cos(\pi*n)\}$ is identically zero thus

$$Van = 0$$

for $n = 2,4,6.....$

$$Van = (Em/\pi)*\left\{\frac{\cos(n+1)a - \cos(n+1)b}{n+1} + \frac{\cos(n-1)a - \cos(n-1)b}{n-1}\right\}$$

for $n = 3,5,7.....$ (4)

The case n = 1 is treated separately:

$$Va1 = (Em/\pi) \int \cos wt\ \sin(wt)\ dwt$$

$$= (Em/2*\pi) \int \sin(2*wt)\ dwt$$

$$= (Em/4*\pi)*[\cos(2*wt)]_{a}^{\Pi-b}$$

$$= (Em/2*\pi)*[\cos(2*b) - \cos(2*a)] \qquad (2)$$

The sine Fourier co-efficients result by evaluating

$$Vbn = (Em/\pi) \int \sin(wt)\ \sin(n*wt)\ dwt$$

$$= (Em/2*\pi) \int \{\cos((n-1)wt)-\cos((n+1)wt)\}\ dwt \quad n \neq 1$$

$$= (Em/2*\pi)*\left[\frac{\sin((n-1)wt)}{n-1} - \frac{\sin((n+1)wt)}{n+1}\right]_{a}^{\Pi-b}$$

$$= \frac{Em}{2\pi}*\{1-\cos(\pi*n)\}*\left[\frac{\sin(n+1)a + \sin(n+1)b}{n+1} - \frac{\sin(n-1)a + \sin(n-1)b}{n-1}\right]$$

for n even, $\{1-\cos(\pi*n)\} = 0$, that is:

$$Vbn = 0$$

for n = 2,4,6.....

$$Vbn = (Em/\pi)\left[\frac{\sin(n+1)a + \sin(n+1)b}{n+1} - \frac{\sin(n-1)a + \sin(n-1)b}{n-1}\right]$$

for n = 3,5,7..... (5)

when n = 1

$$Vb1 = (Em/\pi) \int \sin(wt)\ \sin(wt)\ dwt$$

$$= (Em/2*\pi) \int (1 - \cos(2*wt))\ dwt$$

$$= (Em/2*\pi)*[wt - (1/2)\sin(2*wt)]_{a}^{\Pi-b}$$

$$= (Em/2*\pi)*[2*(\pi-b-a) + \sin 2a + \sin 2b] \qquad (3)$$

The load current as shown in figure 3.2 is given by solving the following differential equations.

(1) When the supply voltage is applied across the R-L load;

$$R*i + L*di/dt = Em*\sin(wt) \qquad \text{for} \qquad a \leq wt \leq \pi - b \qquad i.$$

(2) When the freewheeling triac conducts, clamping the load to zero volts,

$$R*i + L*di/dt = 0 \qquad \text{for} \qquad \pi - b < wt < \pi + a \qquad ii.$$

Case (1)

Considering the first load condition and taking the Laplace transform of equation i yields:

$$i1(s) = \{(w*Em/L)/(s^2 + w^2)*(s+R/L)\} + Ii/(s+R/L)$$

i.e. $$i1(wt) = (Ii + w*L*Io/Z)*\exp(-wt/Q) + Io*\sin(wt-\emptyset)$$

where $$Z = \text{sqrt}(R^2 + w^2L^2)$$

$$Q = w*L/R$$

$$\emptyset = \arctan(Q)$$

$$Io = Em/Z$$

and Ii is the initial current. To evaluate Ii we substitute i1(a) = Ia, that is:

$$Ia = (Ii + w*L*Io/Z)*\exp(-a/Q) + Io*\sin(a-\emptyset)$$

isolating Ii yields:

$$Ii = \{Ia - Io*\sin(a-\emptyset)\}*\exp(a/Q) - w*L*Io/Z$$

substituting this expression for Ii into the equation for i1(wt) yields:

$$i1(wt) = \{Ia - Io*\sin(a-\emptyset)\}*\exp((-wt+a)/Q) + Io*\sin(wt-\emptyset)$$

$$\text{for} \quad a \leq wt \leq \pi - b \qquad (8a)$$

Case (2)

Taking the Laplace transform of equation ii. gives

$$i2(s) = io/(s+R/L)$$

i.e. $i2(wt) = io*\exp(-wt/Q)$

substituting the condition i2(n-b) = Ib yields:

$$io = Ib*\exp((-\pi+b)/Q)$$

replacing io in the expression for i2(wt) results in

$$i2(wt) = Ib*\exp((\pi-b-wt)/Q) \qquad (8b)$$

Expressions are now required for the boundary conditions; namely Ia and Ib.

By load symmetry,

$$i2(\pi+a) = -i1(a) \quad \text{i.e.}$$

$$Ib*\exp(-(a+b)/Q) = -\{(Ia - Io*\sin(a-\emptyset)) + Io*\sin(a-\emptyset)\}$$

and thus $Ib = -Ia*\exp((a+b)/Q) \qquad (10)$

Since the load current is continuous, at the boundary wt = π - b,

$$i2(\pi-b) = i1(\pi-b)$$

where $i2(\pi-b) = Ib = -Ia*\exp((a+b)/Q)$ thus

$$-Ia*\exp((a+b)/Q) = i1(\pi-b)$$

$$= \{Ia-Io*\sin(a-\emptyset)\}*\exp((a+b-\pi)/Q)+Io*\sin(\pi-b-\emptyset)$$

yielding

$$Ia = Io*\{\frac{\exp(-\pi/Q)\sin(a-\emptyset) - \exp(-(a+b)/Q)\sin(\emptyset+b)}{1 - \exp(-\pi/Q)}\} \quad (9)$$

Thus the load current is fully specified by equations 8a, 8b, 9 and 10.

The load current harmonics can be derived either by Fourier analysis of the load current waveform given by equations 8a and 8b, or by dividing each load voltage harmonic component, as defined by equations 2 to 5, by the appropriate load impedance presented at that frequency. The later concept results in a simpler mathematical derivation, yielding:

$$I = \sum_{n} [Ian*\cos(n*wt-\emptyset n) + Ibn*\sin(n*wt-\emptyset n)] \quad (12)$$

for n = 1,3,5,...

The load impedance is frequency dependent, according to

$$ZL = R+j*w*n*L$$

that is,

$$ZL = R/\cos\emptyset n$$

where

$$\tan(\emptyset n) = \tan(n*w*L/R)$$

$$= \tan(n*Q)$$

Thus Ian = Van/ZL(n) and Ibn = Vbn/ZL(n)

that is Ian = (Van/R)*cosØn and Ibn = (Vbn/R)*cosØn (11)

Efficiency, η is defined as the ratio of the fundamental active power to the total active power fed to the load. Real power can only be dissipated by the purely resistive component of the load. Hence

$$\eta = (Ia1^2*R + Ib1^2*R) / \sum_n (Ian^2*R + Ibn^2*R)$$

$$= (Ia1^2 + Ib1^2) / \sum_n (Ian^2 + Ibn^2) \quad (13)$$

for n = 1,3,5,..

3.6(ii) Determination of Supply Power Factor

The supply current waveform Is, as shown in figure 3.2 is given by equation 8a.

$$Is(wt) = \{Ia - Io*\sin(a-Ø)\}\exp((a-wt)/Q) + Io*\sin(wt-Ø)$$

$$= A*\exp(-wt/Q) + Io*\sin(wt-Ø)$$

for $a \leq wt \leq \pi - b$

$$= 0 \qquad \text{elsewhere : } wt < \pi \quad (14)$$

where $A = \{Ia - Io*\sin(a-Ø)\}*\exp(a/Q)$

The non-fundamental frequency components of the supply current waveform result in waveform distortion. A measure of this distortion, called supply current distortion factor y, is defined in terms of the supply current fundamental Fourier components and the rms supply current.

The supply current cosine fundamental Fourier co-efficient magnitude is given from

$$Isa1 = (2/\pi) \int \{A*\exp(-wt/Q) + Io*\sin(wt-\emptyset)\} \cos wt \, dwt$$

$$= \frac{2}{\pi}*[A1*\exp(-wt/Q)\cos(wt+\emptyset) - \frac{Io}{2}\{wt*\sin\emptyset+\frac{1}{2}\cos((2*wt)-\emptyset)\}]_{a}^{\Pi-b}$$

$$= (2/n)[A1*\{\exp(-a/Q)\cos(\emptyset+a) + \exp((-\pi+b)/Q)\cos(\emptyset-b)\}$$

$$-(Io/2)[(\pi-b-a)\sin\emptyset + (1/2)\{\cos(\emptyset+2b)-\cos(\emptyset-2a)\}] \quad (15)$$

where $A1 = A/\mathrm{sqrt}(1+1/Q^2)$

The fundamental sine Fourier co-efficient is given by

$$Isb1 = (2/\pi) \int \{A*\exp(-wt/Q) + Io*\sin(wt-\emptyset)\} \sin wt \, dwt$$

$$= \frac{2}{\pi}*[A1*\exp(-wt/Q)\sin(wt+\emptyset) + \frac{Io}{2}\{wt*\cos\emptyset-\frac{1}{2}\sin((2*wt)-\emptyset)\}]_{a}^{\Pi-b}$$

$$= (2/\pi)[A1*\{\exp(-a/Q)\sin(a+\emptyset) + \exp((-\pi+b)/Q)\sin(\emptyset-b)\}$$

$$+(Io/2)*[(\pi-b-a)\cos\emptyset + (1/2)\{\sin(\emptyset+2b)-\sin(\emptyset-2a)\}] \quad (16)$$

The fundamental Fourier co-efficients define the fundamental supply power factor, cosu, that is

$$cosu = \cos(-\arctan(Isa1/Isb1)) \qquad (17)$$

The rms supply current is found by solving:

$$Isrms^2 = (1/\pi) \int Is(wt)^2 dwt$$

$$= (1/\pi) \int \{A*\exp(-wt/Q) + Io*\sin(wt-\emptyset)\}^2 dwt$$

$$= (1/\pi) \int (A^2\exp(-(2*wt)/Q) + 2*A*Io*\exp(-wt/Q)\sin(wt-\emptyset) + Io^2*\sin^2(wt-\emptyset)\} dwt$$

$$= (1/\pi)[-(A^2Q/2)\exp(-(2*wt)/Q)-2*A1*Io**\exp(-wt/Q)\sin(wt) + (Io^2/2)\{wt-(1/2)\ \sin(2(wt-\emptyset))\}]_a^{\Pi-b}$$

$$= (1/\pi)[-(A^2Q/2)\{\exp(-2(\pi-b)/Q) - \exp(-2a/Q\} +2*A1*Io*\{\exp(-(\pi-b)/Q)\sin(b) + \exp(-a/Q)\sin(a)\} + (Io^2/2)\{(\pi-b-a)+(1/2)[\sin(2(b+\emptyset))+\sin(2(a-\emptyset))]\}] \qquad (19)$$

The current distortion factor is defined as the ratio of the fundamental rms current to the total rms current that is $y = sqrt\{(Isa1^2 + Isb1^2)/2\}/Isrms$

The fundamental real power is given by

$$Es*sqrt\{(Isa1^2+ Isb1^2)/2\}*cosu$$

while the total apparent power is given by

$$Es*Isrms$$

The ratio of real to apparent power is called total power factor k, that is

$$k = [Es*sqrt\{(Isa1^2+ Isb1^2)/2\}*cosu]/(Es*Isrms)$$

$$= y*cosu \qquad (18)$$

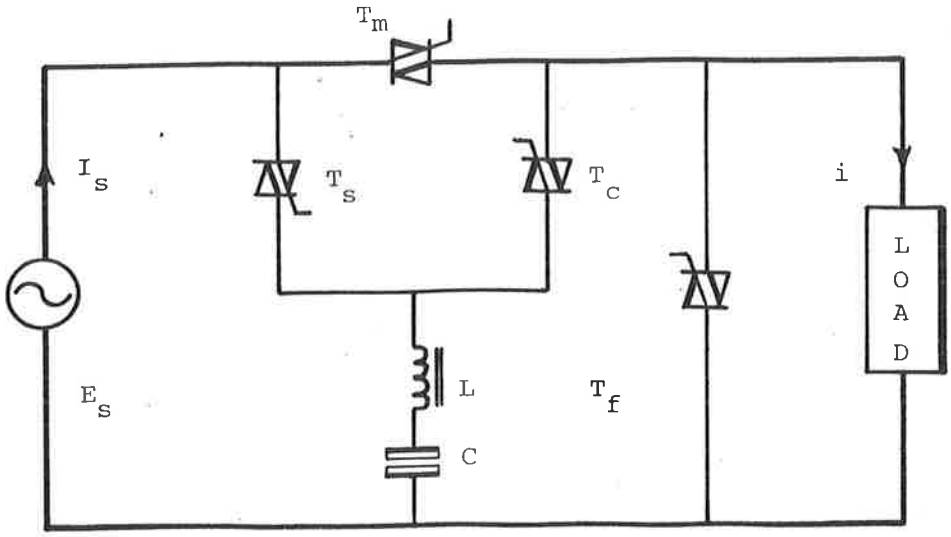


FIGURE 3.1 A.C. Chopper Circuit

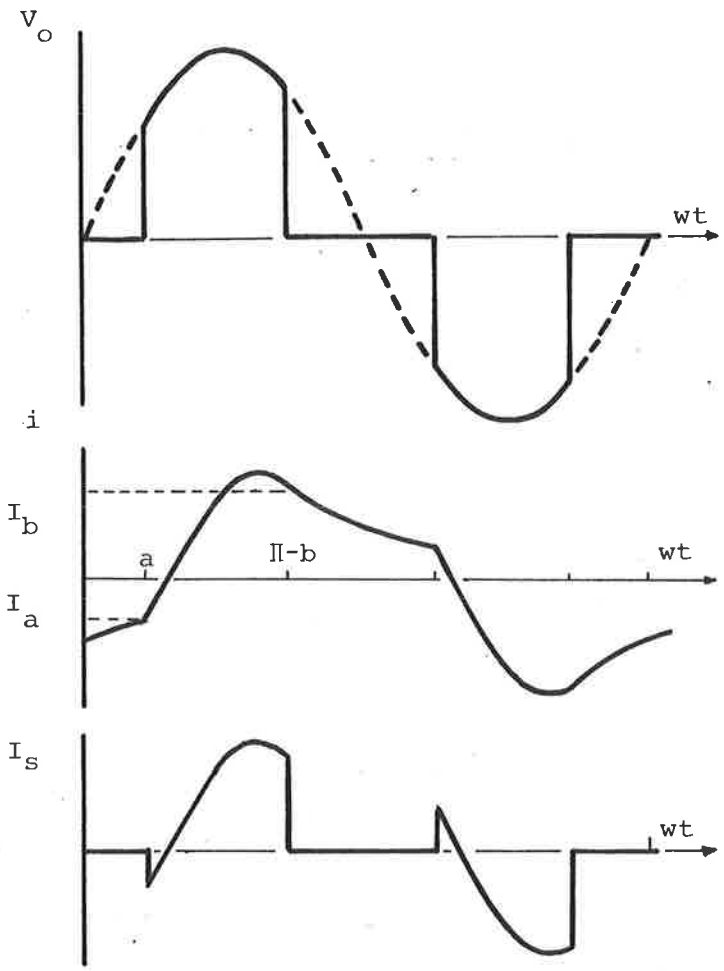
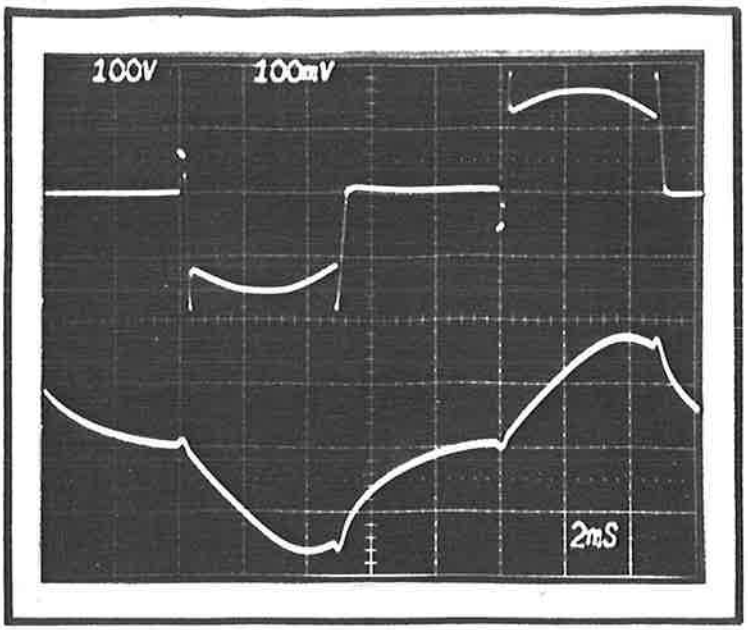


FIGURE 3.2 Asymmetrical A.C. chopper supply and load waveforms



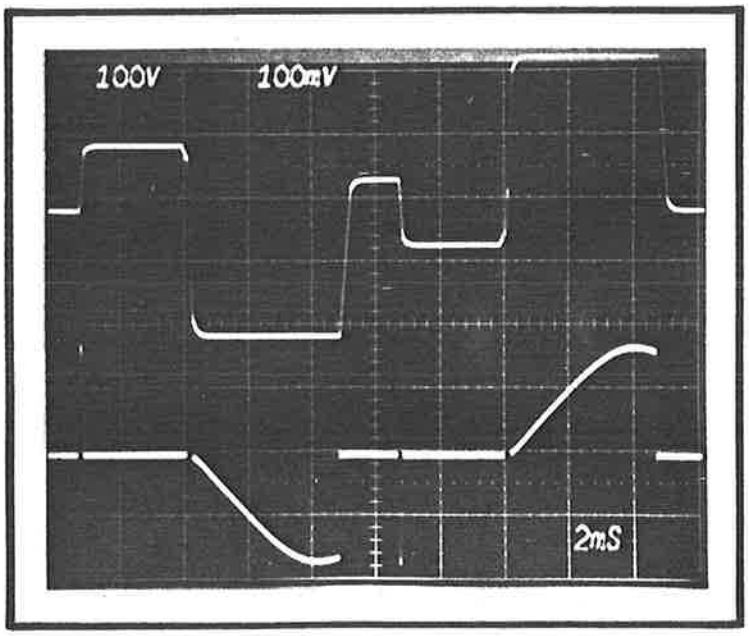
V_o

I

load: Z = 43Ω, Q = 1 at 50 Hz

I : 50 mV ≡ 1A

(a)



V_c

I_s

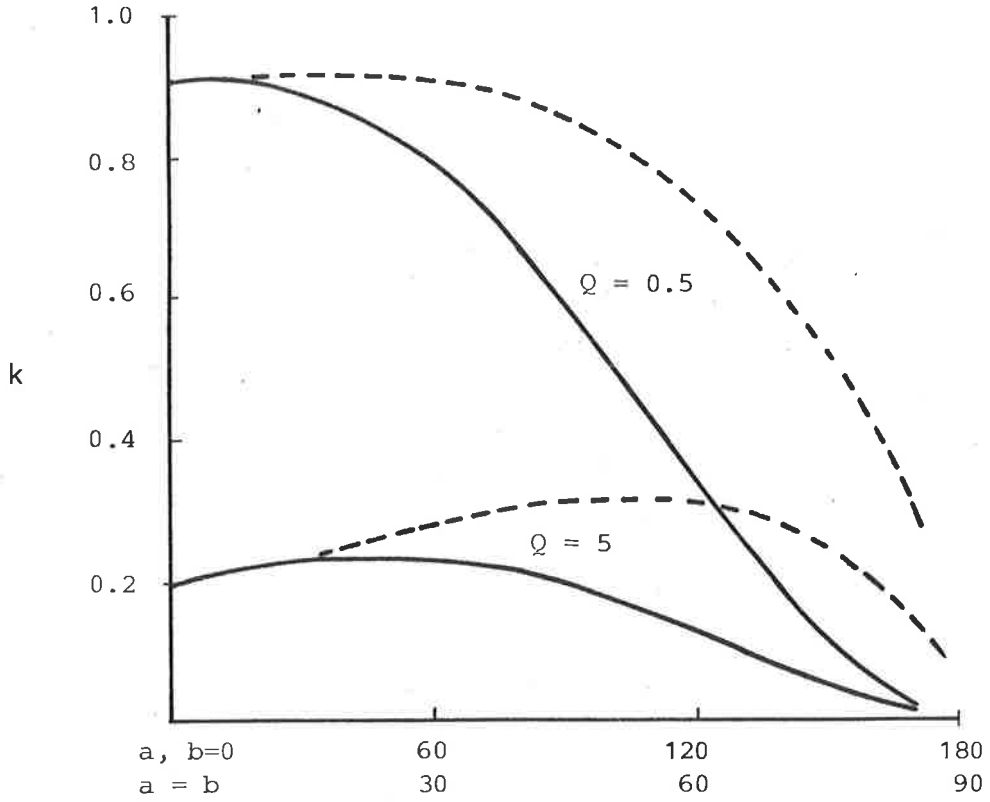
(b)

FIGURE 3.3

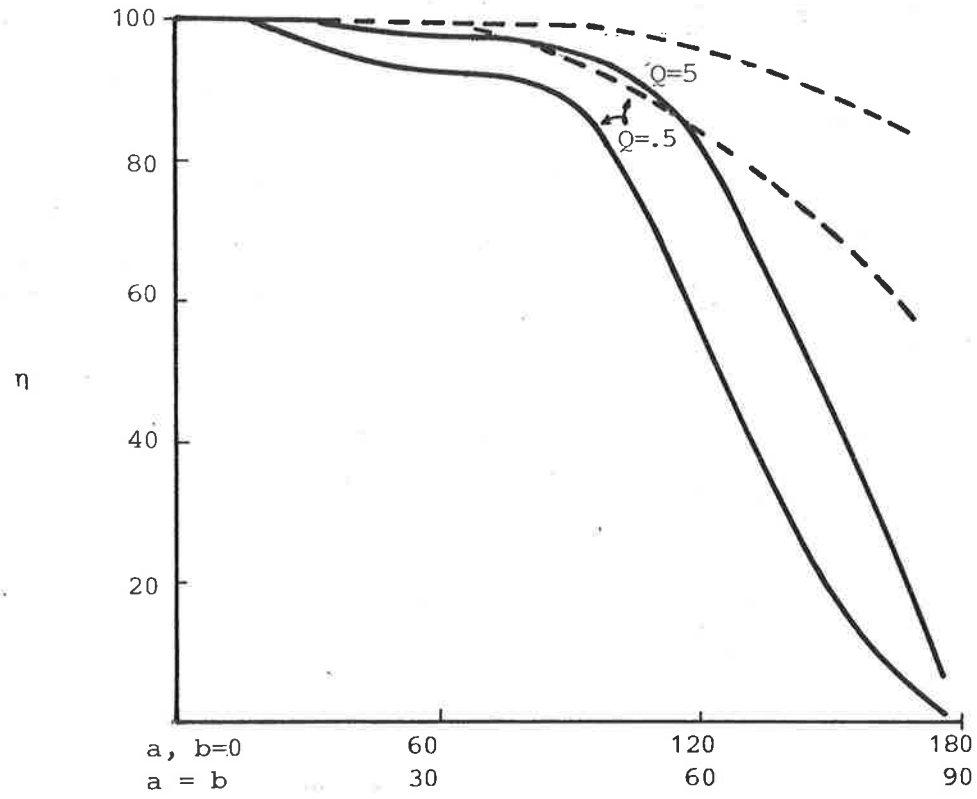
Experimental waveforms of

(a) load voltage and current

(b) capacitor voltage and supply current



(a)



(b)

FIGURE 3.4

Load Characteristics Comparison

—— a.c. phase control (b = 0)
--- symmetrical a.c. chopping (a=b)

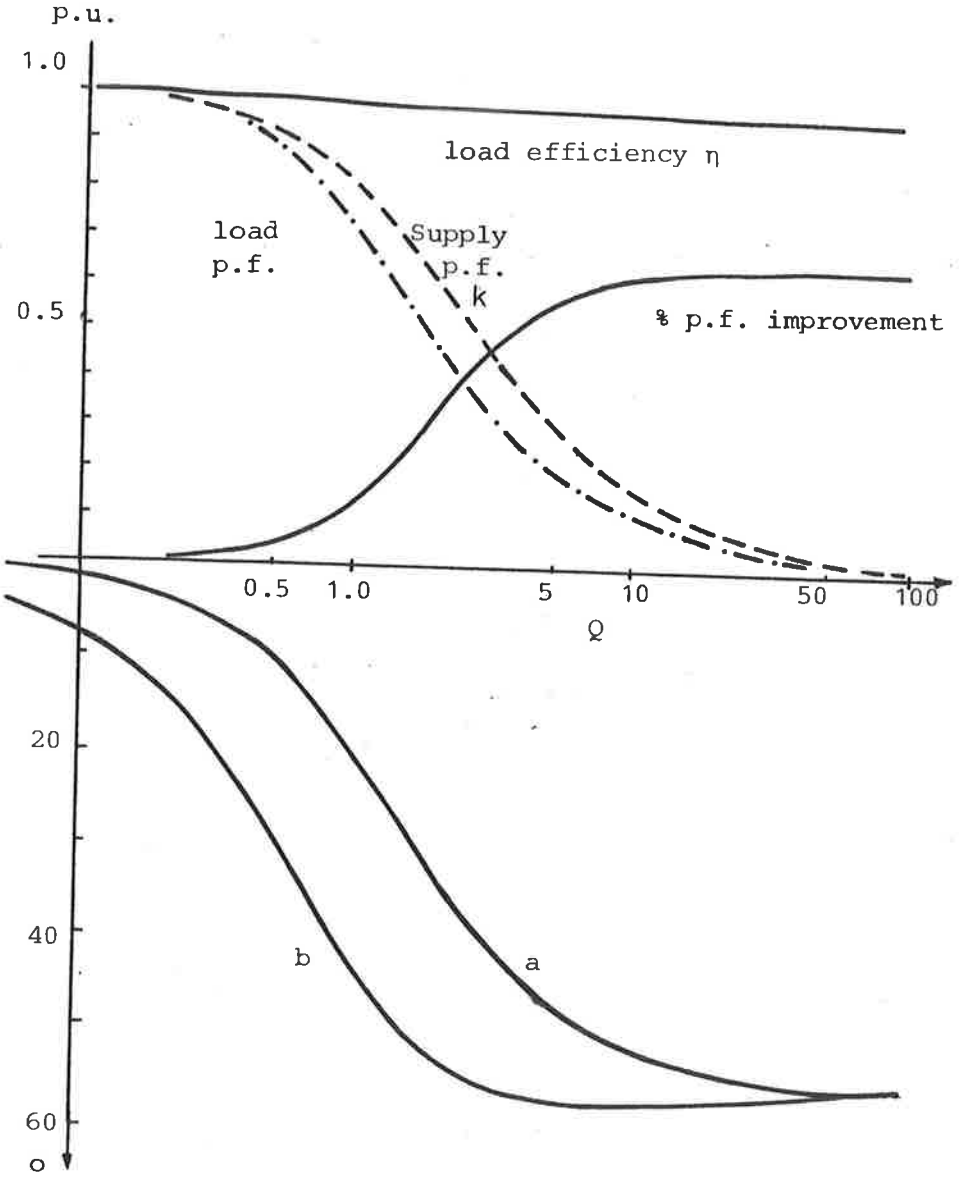


FIGURE 3.5

Optimised asymmetrical A.C. chopper characteristics

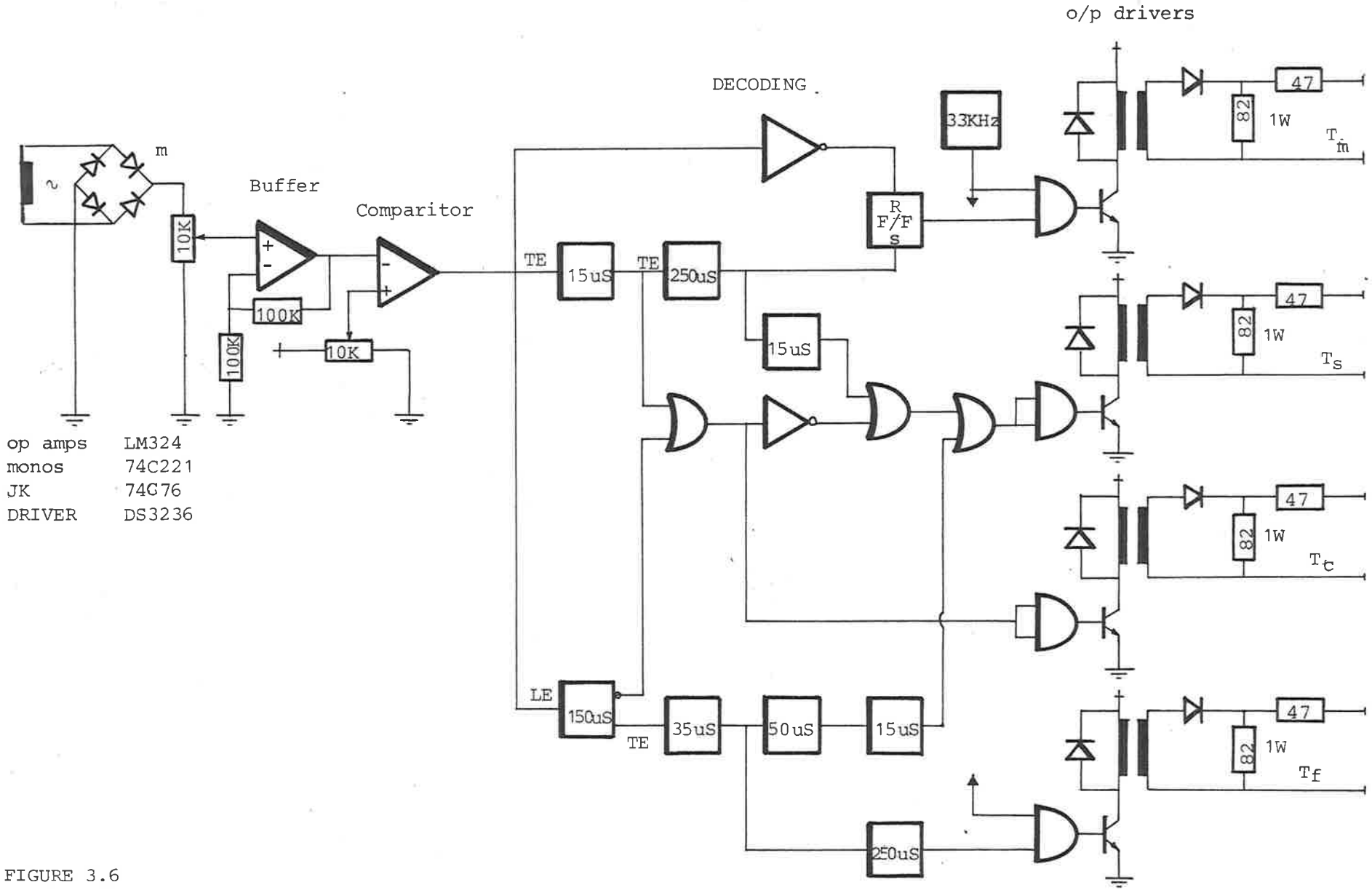


FIGURE 3.6

Symmetrical A.C. chopper triggering circuit

CHAPTER 4

A d.c. - THREE-PHASE INVERTER

This chapter discusses the adaptation of the current impulse displacement thyristor commutation technique of Chapter 2, to a direct current to three phase variable frequency thyristor inverter. A novel feature of the implementation is the use of only one inductor-capacitor bridge resonant circuit for commutation, instead of three as normally required to commutate the six main bridge thyristors. This is achieved by using a directed bridge commutation technique.

A microprocessor is used to derive thyristor triggering signals and to facilitate all feedback, input and output signal control [1],[2]. A squirrel cage induction machine load is used in a programmed controlled-slip mode of operation. In this dedicated application, the use of the microprocessor reduces the chip count to less than half that required for conventionally used analogue and digital circuitry and provides a more versatile system for no extra cost. Other electrical machine

control modes can be incorporated by different software.

The features of the microprocessor program used will be discussed, and the actual program is presented in the appendix at the end of this chapter.

4.1 The DIRECTED BRIDGE INVERTER

The thyristor inverter circuit and associated thyristor commutation bridge are shown in figure 4.1. By sequentially turning the main thyristors Tm numbers one to six on and off according to the timing diagram of figure 4.2, a six step quasi-square three phase waveform is generated at the output terminals R-B-Y on figure 4.1.

The output line to line voltage waveform is defined by

$$Vry = \frac{2*\sqrt{3}*E}{\pi}\left(\sin wt - \frac{1}{5}*\sin 5wt - \frac{1}{7}*\sin 7wt + \frac{1}{11}*\sin 11wt + \right.$$

while the line to neutral voltage is given by

$$Vrn = \frac{3*E}{\pi}\left(\sin wt + \frac{1}{5}*\sin 5wt + \frac{1}{7}*\sin 7wt + \frac{1}{11}*\sin 11wt + \ldots\right.$$

This operation of the main bridge is familiar and well documented; a more detailed discussion on the waveforms along with related effects on motor performance due to the non-fundamental supply voltage components is found in reference [3].

In this application each thyristor in the main bridge, for example Tm1, has an associated commutating bridge thyristor Tc1.

Consider the case when main thyristor Tm1 is to be force commutated. This is achieved as follows:

Initially the commutation capacitor C holds an assisting charge, resulting from voltage boosting during the last commutating cycle.

The capacitor set thyristors Ts are triggered which allows C to charge to a voltage of over 2*E due to L-C resonant circuit action. This complete, the commutation thyristors Tc1 and Tc,odd are triggered, which allows a sinusoidal current impulse to displace the load current through Tm1. Provided the displacement current in excess of the load current Ia, flows through bridge diode D1 for a time in excess of the circuit turn-off time tq of thyristor Tm1, it will regain forward voltage blocking ability.

Once the commutation circuit displacement current has ceased, the complementary main bridge thyristor Tm4 may be triggered. The thyristor Tm4 is commutated by triggering thyristors Ts, followed by Tc4 and Tc,even simultaneously.

The circuit modification of section 2.4 can be incorporated to make the commutation cycle interval load current magnitude independent. This modification will allow an operating frequency of up to 100/tq kHz, which would be suitable for pulse width modulation applications.

All the equations and formulae as well as basic operating principles of Chapter 2 are applicable to the circuit operation discussed above.

4.2 The CONTROLLED-SLIP DRIVE

A squirrel cage induction machine is said to be operating in a controlled-slip mode if, independent of the rotor speed, the rotor slip frequency is maintained and controlled at less than the breakdown value.

If the actual rotor speed is less than the required speed, a calculated stator frequency slightly greater than the rotating frequency is applied, and the machine develops a motor torque which accelerates the rotor to the desired speed. When the actual rotor speed is greater than the required speed, the stator is fed with a calculated frequency less than the rotational frequency. Now, the machine operates as an induction generator, returning energy to the supply, thus regeneratively decelerating the machine.

The difference between the rotor and stator speed is limited and can never exceed the breakdown slip value in the motoring or generating regions. As a first order approximation, this maximum slip frequency variation limit is a constant frequency over the usable stator frequency range [3]. This feature is shown on the torque-slip curves of figure 4.3.

Line current magnitude may be taken into account and, if the current is to be reduced, the stator frequency is brought closer to the rotating frequency thereby reducing the developed torque level and hence current.

The house-keeping of required speed, rotor speed and line current can be dedicated to a microprocessor, which can perform all slip control calculations based on the various input parameter magnitudes.

4.3 The PROGRAM and FEATURES of the MICROPROCESSOR CONTROLLER

All input and output functions are assigned and controlled by software execution, which provides a sophisticated and comprehensive primary building block upon which control strategies can be developed and modified without hardware changes.

The basic linear system flow chart for the slip-control algorithm is shown in figure 4.4. The actual program appears in the appendix at the end of this chapter. The main features of the program algorithm, as shown on the flow chart, are as follows:

The required commutation bridge and main bridge triggering sequence is stored in non-volatile memory, and stepping through this sequence at a defined rate varies the bridge output frequency. The output logic sequence is shown in figure 4.5.

A program cycle commences with the input of the various feedback and control signals, such as required speed, rotor speed and line current. These values are stored and used in calculations as determined by the control strategy. A conversion from period to frequency is performed, by division or repeated subtraction, to give a delay related to the output frequency requirement. This delay complete, a commutation cycle occurs, and if a continuation is required the next sequence set is transmitted. This output sequence is then incremented by one set. Machine reversing is achieved by stepping in the opposite direction through the stored output sequence.

An important application limitation occurs because all operations, i.e. input, calculations and output, must be performed in real time. The operation time around the closed loop of the flow chart, except the division process, is fixed. The time delay by repeated subtraction is shortened by a factor equivalent to this time, thus all operations are performed and adjusted for in real time. Naturally the highest possible bridge output frequency will be restricted to the reciprocal of the loop time. Therefore the more complicated the control strategy, the lower the possible bridge output frequency for a given microprocessor.

The use of a fixed operation cycle loop time is only possible because the commutation cycle of the proposed directed bridged is load current independent, thus taking a known and accountable length of time.

4.4 MICROPROCESSOR PERFORMANCE and STRATEGY CRITERIA

An Intel 8085 8-bit general purpose N-MOS microprocessor was employed to perform all input and output control supervision and calculations. A controlled-slip strategy program was developed which allowed a maximum possible bridge frequency in excess of 660Hz. This upper frequency limit can be extended by using a microprocessor with a faster clock frequency and/or instruction cycle time. Programmed application features include:

Note:- The parameters below evolved from the requirements of the a.c. motor being used in this application.

i. Simple motor direction changing. This is achieved by stepping through the stored output sequence in the opposite direction. A change in direction will not be executed until the rotor speed falls below an adjustable limit. Default is set at 60rpm.

ii. Stop/start frequency hysteresis. The minimum starting frequency is adjustable and set to 4Hz by default. The minimum frequency for circuit shutdown is adjustable down to 0.8Hz and is set to this value by default. That is, motor regeneration is possible down to 48rpm for a 2-pole squirrel cage induction machine.

iii. Programmable output frequency range of over two decades. The default range is 0.8Hz to 88Hz.

iv. Current limiting band and absolute upper limit current turn-off priority control. At a value less than the designed maximum commutation current, the stator frequency is made equal to the rotational frequency. This reduces the line current to zero. The default current limit value is 30A and the cut in point is adjustable or set to 20A by default. That is, as the line current increase from 20A to 30A, slip is progressively reduced from unaffected at 20A to zero at 30A.

v. Adjustable maximum slip limit. The maximum allowable slip frequency, as determined by the particular rotor characteristics is adjustable from 0 to the maximum frequency.

The maximum slip for motoring may be set differently to that for regeneration. Default is for both to be set equal to 5Hz, i.e. slip 0.1 at 50Hz.

vi. Programmable torque profile rate. When the difference between the required speed and the rotor speed exceeds an adjustable limit, maximum allowable slip is applied. The slip is reduced linearly from the maximum value to zero at synchronous speed. The default maximum slip is

applied when the rotor and required speed difference equals or exceeds half the maximum speed range.

vii. Auxiliary regenerative braking. At low stator frequencies, during regeneration at low shaft speeds, only small slip can be attained because of the strategy outlined in point 6 above. Thus, to facilitate maximum braking torque down to minimum stator frequency, an override braking control, linearly increases the slip until adjusted to the maximum slip frequency. By default this facility commences at half the frequency range and operates down to 0.8 Hz.

viii. Four quadrant machine operation. From points 1 and 5 it is apparent that motoring and generating are possible both in the forward and reverse direction. Most importantly, this is acheived by static power means.

ix. Linear speed control. Linear control is made possible by the division process performed within the program. Without this linearising, interfacing to process controllers would be non-linear, in fact reciprocal controllers would be required. This would generally be unacceptable.

As is illustrated by the above list of features, the limitations lie with the programmer's imagination and not available hardware restrictions. The circuit diagram, including analog to digital interfacing and tachometer-filtering, of the microprocessor controller is shown in figure 4.6. This system can be used for 8 or 12 bit operation. With an 8 bit system the operating frequency range will have 256 discrete output frequencies, while a 12 bit system will provide a finer step controller of 4096 individual frequency levels. The only system differences will be in the control program, which does not involve any hardware changes.

4.5 SYSTEM PERFORMANCE and CONCLUSIONS

The load was a 120V, 5HP squirrel cage induction machine, which was controlled over the complete speed range of 0 to 3000rpm with stable shaft rotation. Typical line to line and line to neutral voltage oscillograms are shown in figure 4.7.

In general, it was found that the controlled-slip induction machine provided a highly efficient drive with precise control of torque over a wide speed range down to standstill. A large torque can be obtained at high power factor and high efficiency by operating at rotor slip frequencies below the breakdown value. The controlled-slip strategy thus provides a stable control system from standstill to maximum speed in both the motoring and generating regions of four quadrant operation.

The overall system characteristics can be tailored and adjusted, to suit the particular application, by means of programming. Other possible modes of control strategy programming include, pulse width modulation, constant current, constant horsepower etc., where the micro-processor can control all data transfer, triggering outputs and any d.c. voltage link.

The prototype controller program does not maintain a constant V/f ratio although existing software and hardware features would facilitate a d.c. link. A pulse width modulation inverting software strategy would be employed in the final system, if control of this ratio were required.

REFERENCES

1 WILLIAMS. B.W. "Microprocessor Control of dc-3 phase Thyristor Inverter Circuits."
to be published, IEEE Trans. Vol. IECI.

2 WILLIAMS. B. et al., "Microprocessor Control of Inverter Drives."
to be presented, IEA Microprocessor Systems Conference 1978

3 MURPHY. J.M.D. "Thyristor Control of A.C. Motors."
Pergamon Press. Chapters 3,5,6 and 7. 1975.

```
 1                              TITLE   '3-PHASE VAR FREQ GEN'
 2                             ;
 3                             ;
 4                             ;DEFINE SYMBOLS
 5                             ;
 6  2800            RDIRN:       EQU     2800H   ;REQD DIRECTN ADDR
 7  07F0            BITA:        EQU     7F0H    ;1ST WORD ADDR
 8  2900            SPA:         EQU     2900H   ;STACK POINTER ADDR
 9  0010            SHYS:        EQU     10H     ;HYSTERESIS SPEED
10  2802            PTSAV:       EQU     2802H   ;PORT 00 SAVE LOCN
11  0003            SMIN:        EQU     3H      ;MINIMUM SPEED
12                             ;-----------------------------------------------
13                             ;
14  0000  C34000                 JMP     START   ;LEAVE SPACE FOR INTS
10                             ;
16  002C                         ORG     2CH     ;ENTRY POINT FOR RST 5.5
17  002C  C3FD02                 JMP     INT5    ;BRANCH TO 5.5 SERV ROUT
18                             ;
19  0034                         ORG     34H     ;ENTRY POINT FOR RST 6.5
20  0034  C30203                 JMP     INT6    ;BRANCH TO 6.5 SERV ROUT
21                             ;-----------------------------------------------
22                             ;INITIALIZATION OF PORTS
23                             ;
24  0040                         ORG     40H     ;START OF INITIALIZATION
25  0040  3E0D      START:       MVI     A,0DH   ;PROG PORTS OF BASIC RAM
26  0042  D328                   OUT     28H     ;PORTS 29,2B-O/P,PORT 2A-I/P
27  0044  3E01                   MVI     A,1H    ;PROG PORTS OF EXP RAM
28  0046  D318                   OUT     18H     ;PORT 19-O/P,PORTS 1A,1B-I/P
29  0048  97                     SUB     A       ;PROG PORTS OF ROM
30  0049  D302                   OUT     2H      ;PORTS 00,01-I/P
31  004B  D303                   OUT     3H
32                             ;-----------------------------------------------
33                             ;OUTPUT EXTERNAL START PULSE
34                             ;TO CURRENT A/D
35                             ;
36  004D  D32B                   OUT     2BH     ;OUTPUT A '0'
37  004F  3E10                   MVI     A,10H
38  0051  D32B                   OUT     2BH     ;OUTPUT A '1'
39  0053  97                     SUB     A
40  0054  D32B                   OUT     2BH     ;OUTPUT A '0'
41                             ;-----------------------------------------------
42                             ;INITIALIZE REQUIRED DIRECTION
43                             ;DEFAULT=01H (FORWARD)
44                             ;
45  0056  3E01                   MVI     A,1H
46  0058  320028                 STA     RDIRN
47                             ;-----------------------------------------------
48                             ;INITIALIZE H,L AND S,P
49                             ;H,L CONTAIN ADDRESS OF BIT PATTERN
50                             ;
51  005B  21F007                 LXI     H,BITA
52  005E            BEGIN:
53  005E  310029                 LXI     SP,SPA
54                             ;-----------------------------------------------
55                             ;SET UP RESTART INTERRUPTS
```

```
                                ;
0061  3E0C                      MVI     A,0CH   ;SET UP INTERRUPTS
0063  30                        SIM             ;RST5.5-SWITCH TURN-OFF
                                                ;RST6.5-CURRENT OVERLOAD
                                ;-----------------------------------------
                                ;POLL TO START
                                ;
0064  F3                        DI              ;DISABLE SYSTEM INTERRUPT
0065                    WAIT:
0065  20                        RIM             ;READ INTERRUPT MASKS
0066  E610                      ANI     10H     ;TEST FOR INTERRUPTS PENDING
0068  C26500                    JNZ     WAIT    ;SWITCH OFF - WAIT
                                ;-----------------------------------------
                                ;OUTPUT A PULSE TO START
                                ;REQD-SPEED A/D.
                                ;
006B  DB2B                      IN      2BH     ;READ PORT
006D  47                        MOV     B,A     ;SAVE IN B
006E  E6EF                      ANI     0EFH
0070  D32B                      OUT     2BH     ;OUTPUT '0' TO REQD
0072  78                        MOV     A,B     ;SPEED A/D START BIT
0073  0E10                      MVI     C,10H
0075  B1                        ORA     C
0076  D32B                      OUT     2BH     ;OUTPUT '1' TO REQD
                                                ;SPEED A/D START BIT
                                ;-----------------------------------------
                                ;START CONV FOR ROTOR-SPEED
                                ; A/D.
                                ;
0078  78                        MOV     A,B
0079  E6CF                      ANI     0CFH
007B  D32B                      OUT     2BH     ;RESET REQD- & ROTOR-
                                                ;SPEED A/D START BITS
                                ;
007D  3E0E                      MVI     A,0EH   ;DELAY VALUE
007F  CDF802                    CALL    DELAY   ;DELAY=73USEC
                                ;
0082  78                        MOV     A,B
0083  0E20                      MVI     C,20H
0085  B1                        ORA     C
0086  D32B                      OUT     2BH     ;OUTPUT '1' TO ROTOR
                                                ;SPEED A/D START BIT
                                ;
0088  3E38                      MVI     A,38H   ;DELAY VALUE
008A  CDF802                    CALL    DELAY   ;DELAY=261USEC
                                ;-----------------------------------------
                                ;TEST REQD & ACTUAL DIRNS. IF SAME,
                                ;CONT. OTHERWISE CHECK ROTOR SPEED
                                ;IS BELOW MIN SPEED, SMIN. IF NOT,
                                ;RETURN TO 'BEGIN'.
                                ;
008D  0600                      MVI     B,00H
008F  CDFA01                    CALL    TEST
                                ;-----------------------------------------
                                ;LIMIT INITIAL ROTOR SPEED.
```

```
111                             ;
112  0092  7B                    MOV     A,E
113  0093  D605                  SUI     5H
114  0095  D25E00                JNC     BEGIN
115                             ;-------------------------------------------------
116                             ;CHECK REQD SPEED IS GREATER THAN
117                             ;SHYS. OTHERWISE RETURN TO 'BEGIN'.
118                             ;
119  0098  3E10                  MVI     A,SHYS
120  009A  92                    SUB     D
121  009B  D25E00                JNC     BEGIN
122                             ;-------------------------------------------------
123                             ;OUTPUT A WORD FROM BIT PATTERN
124                             ;INTE IS ENABLED TO ALLOW TURN-OFF
125                             ;BY SWITCH OR CURRENT OVERLOAD
126                             ;
127  009E  7E                    MOV     A,M
128  009F  D329                  OUT     29H     ;OUTPUT A WORD
129                             ;
130  00A1              LOOP:
131  00A1  FB                    EI              ;ENABLE INTE FLAG
132                             ;-------------------------------------------------
133                             ;READ VALUE FROM PORT 00
134                             ;AND SAVE IT.
135                             ;
136  00A2  DB00                  IN      0H      ;READ PORT 00
137  00A4  320228                STA     PTSAV   ;SAVE IN LOC PTSAV
138                             ;-------------------------------------------------
139                             ;TEST REQD & ACTUAL DIRNS. IF SAME,
140                             ;CONT. OTHERWISE CHECK ROTOR SPEED
141                             ;IS BELOW MIN SPEED, SMIN. IF NOT
142                             ;BRANCH TO TURN-OFF.
143                             ;
144  00A7  0680                  MVI     B,80H
145  00A9  CDFA01                CALL    TEST
146                             ;-------------------------------------------------
147                             ;READ CURRENT.
148                             ;
149  00AC  DB01                  IN      1H      ;INPUT CURRENT
150  00AE  0F                    RRC             ;SHIFT RIGHT
151  00AF  E67F                  ANI     7FH     ;MASK OUT MSB
152  00B1  4F                    MOV     C,A     ;SAVE IN C
153                             ;-------------------------------------------------
154                             ;RESET ROTOR SPEED A/D
155                             ;
156  00B2  DB2B                  IN      2BH
157  00B4  E61F                  ANI     1FH
158  00B6  D32B                  OUT     2BH
159                             ;-------------------------------------------------
160                             ;TEST FOR REVERSAL OF DIRECTION.
161                             ;ALLOW DIRN CHANGE ONLY IF ROTOR
162                             ;SPEED IS BELOW SMIN.
163                             ;
164  00B8              DIRN:
165  00B8  DB1B                  IN      1BH     ;READ REQD DIRN
```

```
166  00BA  E602            ANI     2H
167  00BC  0F              RRC
168  00BD  47              MOV     B,A     ;SAVE IN B
169  00BE  7B              MOV     A,E     ;GET ROTOR SPEED
170  00BF  D603            SUI     3H      ;SUBTRACT 03
171  00C1  D2D400          JNC     CONT    ;ROTOR SPEED GREATER?
172  00C4  3A0028          LDA     RDIRN   ;NO - GET PRESENT DIRN
173  00C7  90              SUB     B       ;COMPARE WITH NEW DIRN
174  00C8  C2DF00          JNZ     CHANGE  ;DIRECTIONS SAME?
175  00CB  3E02            MVI     A,2H    ;YES - DELAY
176  00CD  CDF802          CALL    DELAY
177  00D0  C0              RNZ             ;DUMMY INSTR.
178  00D1  C3E200          JMP     TESTOP
179  00D4          CONT:
180  00D4  3E03            MVI     A,3H    ;NO CHANGE OF DIRN
181  00D6  CDF802          CALL    DELAY     ;DELAY
182  00D9  3AFFFF          LDA     0FFFFH  ;DUMMY INSTR
183  00DC  C3E200          JMP     TESTOP
184  00DF          CHANGE:
185  00DF  CDE301          CALL    ADJUST  ;DIRNS DIFFERENT -
186                                        ;ADJUST BIT ADDR &
187                                        ;UPDATE REQD DIRN.
188                        ;-----------------------------------------------
189                        ;CHECK ROTOR & REQD SPEEDS ARE ABOVE SMIN.
190                        ;IF NOT, GO TO TURN-OFF SEQUENCE.
191                        ;
192  00E2          TESTOP:
193  00E2  7B                MOV     A,E     ;GET ROTOR SPEED
194  00E3  D603              SUI     SMIN    ;SUBTRACT MIN SPEED
195  00E5  D2F100            JNC     GO      ;ROTOR SPEED GREATER?
196  00E8  7A                MOV     A,D     ;NO - GET REQUIRED SPEED
197  00E9  D603              SUI     SMIN    ;SUBTRACT MIN SPEED
198  00EB  D2F600            JNC     HERE    ;REQUIRED SPEED GREATER?
199  00EE  C3FD02            JMP     INT5    ;NO - BEGIN TURN-OFF
200  00F1          GO:
201  00F1  00                NOP             ;ROTOR SPEED GREATER -
202  00F2  00                NOP             ;CONTINUE
203  00F3  C3F600            JMP     HERE
204                        ;-----------------------------------------------
205                        ;START CONV FOR REQD- & ROTOR-
206                        ;SPEED A/D'S.
207                        ;
208  00F6          HERE:
209  00F6  DB2B              IN      2BH
210  00F8  0630              MVI     B,30H
211  00FA  B0                ORA     B
212  00FB  D32B              OUT     2BH
213  00FD  DB2B              IN      2BH
214  00FF  E6EF              ANI     0EFH
215  0101  D32B              OUT     2BH     ;RESET REQD SPEED
216                                          ;A/D START BIT
217                        ;-----------------------------------------------
218                        ;SET NUMBER K - 64B
219                        :ADJUSTMENT FOR PROG EXECUTN TIME
220                        ;K DETERMINES FREQUENCY RANGE
```

```
221                             ;
222   0103   CD6602              CALL    FREQ    ;DETERMINE FREQ
223                                             ;REQUIREMT.
224   0106   78                  MOV     A,B     ;GET OUTPUT FREQ
225                                             ;REQUIREMT
226   0107   0F                  RRC             ;ROTATE RIGHT TWICE
227   0108   0F                  RRC
228   0109   57                  MOV     D,A     ;SAVE IN D
229   010A   E63F                ANI     3FH     ;MASK OUT 2 MSB'S
230   010C   5F                  MOV     E,A
231   010D   7A                  MOV     A,D
232   010E   E6C0                ANI     0C0H    ;MASK OUT 6 LSB'S
233   0110   57                  MOV     D,A     ;(E)(D) = 64 X B
234   0111   97                  SUB     A       ;CLEAR ACC
235   0112   92                  SUB     D       ;START 16-BIT SUBTRACTN
236   0113   57                  MOV     D,A
237   0114   D21801              JNC     DONE
238   0117   1C                  INR     E
239   0118              DONE:
240   0118   3EFF                MVI     A,0FFH  ;SETS FREQ RANGE
241   011A   93                  SUB     E
242   011B   5F                  MOV     E,A
243   011C   7A                  MOV     A,D     ;(E)(A)=2**15 - 64(B)
244                             ;-----------------------------------------------
245                             ;TIMING LOOP
246                             ;DELAY = (28 X B) STATES
247                             ;
248   011D              TIME:
249   011D   90                  SUB     B
250   011E   DA2601              JC      DECR1
251   0121   C600                ADI     00H
252   0123   C31D01              JMP     TIME
253   0126              DECR1:
254   0126   1D                  DCR     E
255   0127   C21D01              JNZ     TIME
256                             ;-----------------------------------------------
257                             ;MASTER DELAY ADJUSTMENT
258                             ;COMPENSATES TOTAL LOOP TIME
259                             ;
260   012A   3E01                MVI     A,1H
261   012C              DECR2:
262   012C   3D                  DCR     A
263   012D   C22C01              JNZ     DECR2
264                             ;-----------------------------------------------
265                             ;
266   0130   3E1F                MVI     A,1FH   ;DISABLE INTS DURING
267   0132   30                  SIM             ;THYRISTOR SEQUENCE
268                             ;-----------------------------------------------
269                             ;OUTPUT THYRISTOR SEQUENCE
270                             :OUTPUT 5 WORDS FROM BIT PATTERN
271                             ;
272   0133   CD4202              CALL    ADDR    ;DETERMINE WORD ADDR
273   0136   7E                  MOV     A,M
274   0137   D329                OUT     29H     ;OUTPUT 1ST WORD
275   0139   2C                  INR     L       ;INCREMENT BITA
```

```
276  013A  D602            SUI     2H
277  013C  00              NOP
278  013D  00              NOP
279  013E  00              NOP
280  013F  00              NOP
281  0140  00              NOP
282  0141  D329            OUT     29H     ;OUTPUT 2ND WORD
283  0143  00              NOP
284  0144  47              MOV     B,A
285  0145  3E05            MVI     A,5H    ;DELAY VALUE
286  0147  CDF802          CALL    DELAY   ;DELAY=32.6USEC
287  014A  7E              MOV     A,M
288  014B  D319            OUT     19H     ;OUTPUT 3RD WORD
289  014D  2C              INR     L       ;INCREMENT BITA
290  014E  97              SUB     A
291  014F  00              NOP
292  0150  00              NOP
293  0151  00              NOP
294  0152  00              NOP
295  0153  00              NOP
296  0154  D319            OUT     19H     ;OUTPUT 4TH WORD
297  0156  04              INR     B
298  0157  3E01            MVI     A,1H    ;DELAY VALUE
299  0159  CDF802          CALL    DELAY   ;DELAY=14.7USEC
300  015C  78              MOV     A,B
301  015D  D329            OUT     29H     ;OUTPUT 5TH WORD
302  015F  3E02            MVI     A,2H    ;DELAY VALUE
303  0161  CDF802          CALL    DELAY   ;DELAY=19.2USEC
304  0164  78              MOV     A,B
305  0165  3D              DCR     A
306  0166  D329            OUT     29H     ;OUTPUT '0' WORD
307  0168  3E01            MVI     A,1H    ;DELAY VALUE
308  016A  CDF802          CALL    DELAY   ;DELAY=14.7USEC
309  016D  7E              MOV     A,M
310  016E  D329            OUT     29H     ;OUTPUT NEW WORD
311                        ;
312  0170  3E1C            MVI     A,1CH   ;ENABLE INTERRUPTS
313  0172  30              SIM
314  0173  C3A100          JMP     LOOP    ;REPEAT CYCLE
315                        ;-----------------------------------------------
316                        ;TURN-OFF SEQUENCE
317                        ;
318  0176          TOFF:
319  0176  3E1F            MVI     A,1FH   ;DISABLE INTS DURING
320  0178  30              SIM             ;TURN-OFF
321  0179  0E02            MVI     C,2H    ;INITIALIZE LOOP COUNTER
322  017B          REPEAT:
323  017B  CD4202          CALL    ADDR    ;ADJUST BIT PATTERN ADDR
324  017E  3E02            MVI     A,2H    ;INHIBIT CURRENT A/D
325  0180  D32B            OUT     2BH
326  0182  3E02            MVI     A,2H
327  0184  D329            OUT     29H     ;OUTPUT 1ST WORD
328  0186  2C              INR     L       ;INCREMENT BITA
329  0187  97              SUB     A
330  0188  00              NOP
```

```
331  0189  00              NOP
332  018A  00              NOP
333  018B  00              NOP
334  018C  00              NOP
335  018D  D329            OUT     29H     ;OUTPUT 2ND WORD
336  018F  3E04            MVI     A,4H    ;DELAY VALUE
337  0191  CDF802          CALL    DELAY   ;DELAY=28.2USEC
338  0194  7E              MOV     A,M
339  0195  D319            OUT     19H     ;OUTPUT 3RD WORD
340  0197  2C              INR     L       ;INCREMENT BITA
341  0198  97              SUB     A
342  0199  00              NOP
343  019A  00              NOP
344  019B  00              NOP
345  019C  00              NOP
346  019D  00              NOP
347  019E  D319            OUT     19H     ;OUTPUT 4TH WORD
348  01A0  3E01            MVI     A,1H    ;DELAY VALUE
349  01A2  CDF802          CALL    DELAY   ;DELAY=14.7USEC
350  01A5  3E01            MVI     A,1H
351  01A7  D329            OUT     29H     ;OUTPUT 5TH WORD
352  01A9  97              SUB     A       ;ENABLE CURRENT A/D
353  01AA  D32B            OUT     2BH
354  01AC  3E02            MVI     A,2H    ;DELAY VALUE
355  01AE  CDF802          CALL    DELAY   ;DELAY=19.2USEC
356  01B1  97              SUB     A
357  01B2  D329            OUT     29H     ;OUTPUT A ZERO WORD
358                        ;
359  01B4  79              MOV     A,C     ;GET LOOP COUNT
360  01B5  3D              DCR     A       ;DECRMT LOOP COUNT
361  01B6  4F              MOV     C,A     ;SAVE NEW LOOP COUNT
362  01B7  CABD01          JZ      CAUSE   ;COUNT=0 - CONTINUE
363  01BA  C37B01          JMP     REPEAT  ;COUNT NONZERO-REPEAT
364                        ;-----------------------------------------------
365                        ;DETERMINE CAUSE OF TURN-OFF
366                        ;IF TURN-OFF CAUSED BY CURRENT
367                        ;OVERLOAD, INDICATE FAULT & WAIT
368                        ;FOR SWITCH TO BE TURNED OFF
369                        ;
370  01BD            CAUSE:
371  01BD  3E1C              MVI     A,1CH   ;ENABLE INTS AFTER
372  01BF  30                SIM             ;TURN-OFF SEQUENCE
373  01C0  DB1B              IN      1BH     ;READ REQD DIRN
374  01C2  E602              ANI     2H
375  01C4  0F                RRC
376  01C5  4F                MOV     C,A     ;SAVE IN C
377  01C6  3A0028            LDA     RDIRN   ;GET OLD REQD DIRN
378  01C9  91                SUB     C       ;CHANGE OF DIRN?
379  01CA  C4E301            CNZ     ADJUST  ;YES - ADJUST BITA
380                                          ;NO - CONTINUE
381  01CD  78                MOV     A,B
382  01CE  E601              ANI     1H      ;SWITCH TURN-OFF?
383  01D0  C25E00            JNZ     BEGIN   ;YES - GOTO TO 'BEGIN'
384  01D3  3E04              MVI     A,4H    ;NO - OUTPUT FAULT
385  01D5  D32B              OUT     2BH
```

```
441  0217  C32602          JMP     CHECK  ;CHECK ROTOR SPEED
442  021A          REV:
443  021A  7B              MOV     A,E    ;DIRN REV
444  021B  2F              CMA            ;COMPLEMENT
445  021C  5F              MOV     E,A    ;SAVE IN E
446  021D  C5              PUSH    B      ;SAVE B & C REGS
447  021E  DB2B            IN      2BH    ;GET STATE OF
448                                       ;PORT BITS
449  0220  0608            MVI     B,8H   ;'1'- REVERSE
450  0222  B0              ORA     B      ;OR WITH OTHER BITS
451  0223  D32B            OUT     2BH    ;OUTPUT TO LED
452  0225  C1              POP     B      ;RESTORE B & C
453  0226          CHECK:
454  0226  3A0028          LDA     RDIRN  ;GET REQD DIRN
455  0229  91              SUB     C      ;SUB ACTUAL DIRN
456  022A  CA3C02          JZ      SAME   ;DIRNS SAME?
457  022D  7B              MOV     A,E    ;NO - GET ROTOR SPEED
458  022E  D603            SUI     SMIN   ;SUBTRACT SMIN
459  0230  DA4102          JC      SAVE   ;ROTOR SPEED GREATER?
460  0233  78              MOV     A,B    ;YES - DETERMINE
461                                       ;BRANCH PATH
462  0234  E680            ANI     80H    ;BRANCH TO TURN-OFF?
463  0236  C2FD02          JNZ     INT5   ;YES
464  0239  C35E00          JMP     BEGIN  ;NO-GOTO 'BEGIN'
465  023C          SAME:
466  023C  00              NOP
467  023D  00              NOP
468  023E  C34102          JMP     SAVE
469  0241          SAVE:
470  0241  C9              RET
471                        ;-----------------------------------------------
472                        ;SUBROUTINE ADDR
473                        ;TEST REQD DIRN & ADJUST WORD
474                        ;ADDR ACCORDINGLY
475                        ;
476  0242          ADDR:
477  0242  3A0028          LDA     RDIRN  ;GET DIRN BIT
478  0245  A7              ANA     A
479  0246  CA5702          JZ      SUBT   ;FORWARD?
480  0249  3E00            MVI     A,00H  ;YES - CONTINUE
481  024B  7D              MOV     A,L
482  024C  C604            ADI     4H     ;ADD 4 TO L
483  024E  6F              MOV     L,A    ;SAVE NEW ADDR IN L
484  024F  D6F4            SUI     0F4H
485  0251  C26402          JNZ     RIGHT  ;ADDR WITHIN RANGE?
486  0254  2ED0            MVI     L,0D0H ;NO - LOAD CORRECT
487                                       ;ADDR IN L
488  0256  C9              RET
489  0257          SUBT:
490  0257  00              NOP
491  0258  7D              MOV     A,L
492  0259  D608            SUI     8H     ;SUBTRACT 8 FROM L
493  025B  6F              MOV     L,A
494  025C  D6D0            SUI     0D0H
495  025E  D26402          JNC     RIGHT  ;ADDR WITHIN RANGE?
```

```
0261  2EF1          MVI   L,0F1H ;NO - LOAD CORRECT
                                  ;ADDR IN L
0263  C9            RET
0264          RIGHT:
0264  00            NOP
0265  C9            RET
                    ;-----------------------------------------------
                    ;SUBROUTINE FREQ
                    ;DETERMINES THE OUTPUT FREQ REQUIREMT
                    ;BASED ON ROTOR SPEED, REQD SPEED,
                    ;& LINE CURRENT
                    ;
0266          FREQ:
0266  7A            MOV   A,D     ;GET REQD SPEED
0267  93            SUB   E       ;(REQD-ROTOR) SPEED IN A
0268  DA7D02        JC    NEGSL   ;POSITIVE SLIP?
026B  CD9702        CALL  SLIP    ;YES
026E  03            INX   B       ;DUMMY INSTR
026F  0B            DCX   B       ;DUMMY INSTR
0270  F5            PUSH  PSW     ;DUMMY INSTR
0271  F1            POP   PSW     ;DUMMY INSTR
0272  7B            MOV   A,E     ;SLIP REQUIREMENT IN E
0273  80            ADD   B
0274  47            MOV   B,A     ;OUTPUT FREQ REQUIREMT
0275  D27B02        JNC   RETN    ;FREQ GREATER THAN MAX?
0278  06FF          MVI   B,0FFH ;YES-SET DEFAULT MAX=FFH
027A  C9            RET
027B          RETN:
027B  00            NOP           ;DUMMY INSTR
027C  C9            RET
027D          NEGSL:
027D  7B            MOV   A,E     ;NEGATIVE SLIP
027E  92            SUB   D       ;(ROTOR-REQD) SPEED IN A
027F  CD9702        CALL  SLIP    ;DET SLIP REQUIREMT
0282  90            SUB   B
0283  47            MOV   B,A     ;REQD FREQ, PUT IN A
0284  DA8A02        JC    MIN     ;-VE RESULTANT FREQ?
0287  C38C02        JMP   NEGFRE
028A          MIN:
028A  0603          MVI   B,3H    ;YES-ASSIGN MIN
                                  ;FREQ VALUE (=3)
028C          NEGFRE:
028C  D603          SUI   3H
028E  DA9402        JC    LESS    ;REQD FREQ LESS
                                  ;THAN MIN (=3)?
0291  C39602        JMP   EXIT
0294          LESS:
0294  0603          MVI   B,3H    ;YES-SET DEFAULT MIN
0296          EXIT:
0296  C9            RET
                    ;-----------------------------------------------
                    ;SUBROUTINE SLIP
                    ;DETERMINES THE +VE OR -VE SLIP REQUIREMT
                    ;
0297          SLIP:
```

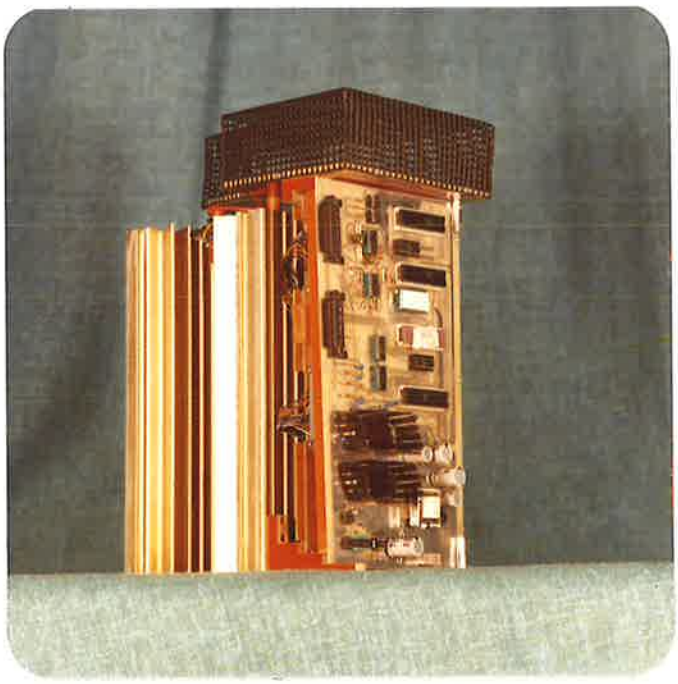
```
0297  47          MOV   B,A
0298  E607        ANI   A,0C0H
029A  CAA502      JZ    ASSIGN ;IS MAX SLIP REQD?
029D  3E11        MVI   A,11H  ;YES-ASSIGN MAX SLIP
                               ;VALUE TO A
029F  CC0000      CZ    0000H  ;DUMMY INSTR
02A2  C3AB02      JMP   CURREN
02A5        ASSIGN:
02A5  78          MOV   A,B    ;ASSIGN SLIP PROPORTNAL
02A6  1F          RAR          ;TO THE ACCELERATN
02A7  1F          RAR          ;REQUIREMT SUCH THAT
                               ;LESS THAN 11H.
02A8  E61F        ANI   1FH    ;MAX SLIP IF GREATER
                               ;THAN 1/4 RANGE
02AA  00          NOP          ;DUMMY INSTR
02AB        CURREN:
02AB  47          MOV   B,A    ;SAVE SLIP REQUIREMT IN B
02AC  79          MOV   A,C    ;MOVE LINE CURRENT TO A
02AD  D62F        SUI   2FH    ;MAX CURRENT VALUE
02AF  D2BC02      JNC   LIMIT  ;CURRENT LIMIT EXCEEDED?
02B2  D0          RNC          ;DUMMY INSTR
02B3  3E00        MVI   A,00H  ;DUMMY INSTR
02B5  3E17        MVI   A,17H  ;DELAY VALUE
02B7  CDF802      CALL  DELAY  ;DELAY
02BA  7B          MOV   A,E    ;YES - SET ZERO SLIP
02BB  C9          RET
02BC        LIMIT:
02BC  4F          MOV   C,A
02BD  3E10        MVI   A,10H  ;CURRENT LIMIT BAND
02BF  91          SUB   C
02C0  4F          MOV   C,A
02C1  E6F0        ANI   0F0H
02C3  CAD102      JZ    MULTI     ;CURRENT LIMITING REQD?
02C6  C8          RZ           ;DUMMY INSTR
02C7  C8          RZ           ;DUMMY INSTR
02C8  3E00        MVI   A,00H  ;DUMMY INSTR
02CA  3E14        MVI   A,14H  ;DELAY VALUE
02CC  CDF802      CALL  DELAY  ;DELAY
02CF  7B          MOV   A,E    ;NO CURRENT LIMITING REQD
02D0  C9          RET
02D1        MULTI:
02D1  D5          PUSH  D      ;SAVE REQD & ACTUAL SPEEDS
                  ;
                  ;START OF TWO 4-BIT WORD MULTIPLICATION -
                  ;ACHIEVED BY REPEATED ADDITION PROCESS
                  ;I.E. D = BXC
                  ;
02D2  1600        MVI   D,00H
02D4  1E04        MVI   E,4H   ;SET LOOP COUNT TO 4
02D6        M1:
02D6  79          MOV   A,C
02D7  0F          RRC
02D8  4F          MOV   C,A
02D9  DAE202      JC    M2
02DC  00          NOP          ;DUMMY INSTR
```

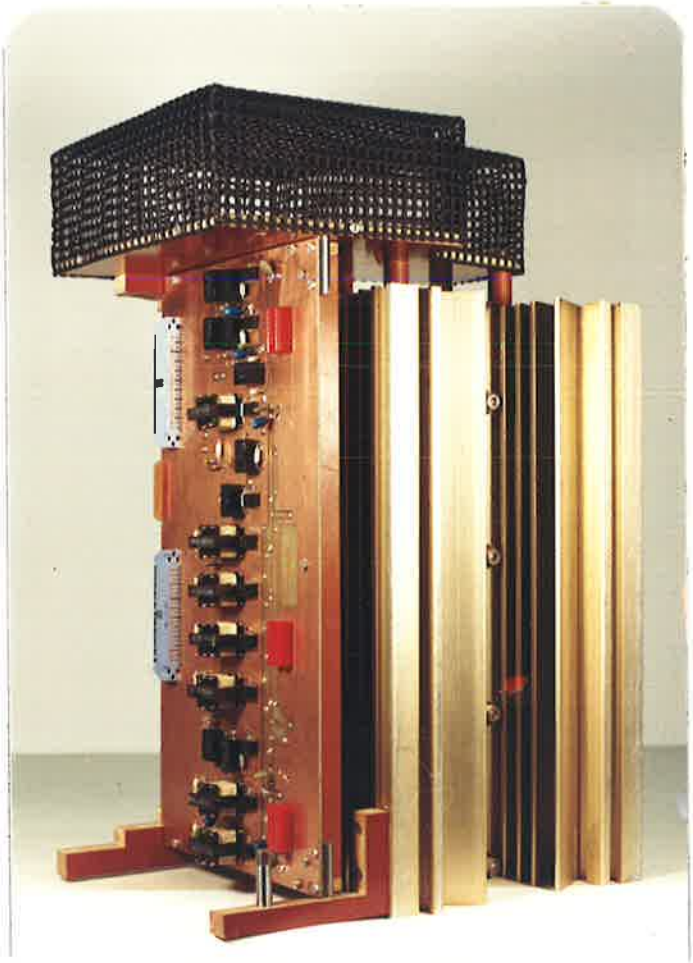
```
606   02DD   3E00            MVI     A,00H  ;DUMMY INSTR
607   02DF   C3E602          JMP     M3
608   02E2           M2:
609   02E2   D0              RNC
610   02E3   7A              MOV     A,D
611   02E4   80              ADD     B
612   02E5   57              MOV     D,A
613   02E6           M3:
614   02E6   78              MOV     A,B
615   02E7   07              RLC
616   02E8   47              MOV     B,A
617   02E9   1D              DCR     E
618   02EA   C2D602          JNZ     M1
619   02ED   7A              MOV     A,D    ;8-BIT RESULT OF
620                                         ;MULTIPLICATN
621   02EE   0F              RRC            ;DIVIDE RESULT BY 16
622   02EF   0F              RRC            ;SO THAT ANSWER IS
623                                         ;ALWAYS LESS THAN 11H.
624   02F0   0F              RRC
625   02F1   0F              RRC
626   02F2   E60F            ANI     0FH    ;MASK OUT UNWANTED H-BYTE
627   02F4   47              MOV     B,A    ;STORE ADJUSTED SLIP IN B
628   02F5   D1              POP     D      ;RESTORE D & E REGISTERS
629   02F6   7B              MOV     A,E
630   02F7   C9              RET
631                         ;-----------------------------------------------
632                         ;SUBROUTINE DELAY
633                         ;TOTAL DELAY IS GIVEN BY
634                         ;TD=[46 + 14(A-1)] STATES
635                         ;
636   02F8           DELAY:
637   02F8   3D              DCR     A
638   02F9   C2F802          JNZ     DELAY
639   02FC   C9              RET
640                         ;-----------------------------------------------
641                         ;SERVICE ROUTINE FOR RST 5.5
642                         ;
643   02FD           INT5:
644   02FD   0601            MVI     B,1H
645   02FF   C37601          JMP     TOFF
646                         ;SERVICE ROUTINE FOR RST 6.5
647                         ;
648   0302           INT6:
649   0302   0600            MVI     B,00H
650   0304   C37601          JMP     TOFF
651                         ;-----------------------------------------------
652                         ;BIT PATTERN
653                         ;
654   07D0                   ORG     7D0H
655   07D0   1A60584A        DB      1AH,60H,58H,4AH,48H,58H
655   07D4   4858
656   07D6   4A846862        DB      4AH,84H,68H,62H,81H,68H
656   07DA   8168
657   07DC   62426426        DB      62H,42H,64H,26H,60H,64H
657   07E0   6064
```

```
658   07E2   2690A486          DB      26H,90H,0A4H,86H,84H,0A4H
658   07E6   84A4
659   07E8   86489492          DB      86H,48H,94H,92H,42H,94H
659   07EC   4294
660   07EE   9281981A          DB      92H,81H,98H,1AH,90H,98H
660   07F2   9098
661                            END
 TOTAL ERRORS =   0
```

********** USER'S SYMBOL TABLE **********

SYMBOL:-VALUE		SYMBOL:-VALUE		SYMBOL:-VALUE		SYMBOL:-VALUE	
A	0007	ADDR	0242	ADJUST	01E3	ASSIGN	02A5
B	0000	BEGIN	005E	BITA	07F0	C	0001
CAUSE	01BD	CHANGE	00DF	CHECK	0226	CONT	00D4
CURREN	02AB	D	0002	DECRM	020B	DECR1	0126
DECR2	012C	DELAY	02F8	DIRN	00B8	DONE	0118
EXIT	0296	E	0003	FORWD	01F0	FREQ	0266
GO	00F1	H	0004	HERE	00F6	INT5	02FD
INT6	0302	LESS	0294	LIMIT	02BC	LOOP	00A1
L	0005	MULTI	02D1	M1	02D6	M2	02E2
M	0006	MIN	028A	M3	02E6	NEGFRE	028C
NEGSL	027D	ON	01D7	PSW	0006	PTSAV	2802
RDIRN	2800	REPEAT	017B	RETN	027B	REV	021A
RIGHT	0264	SAME	023C	SAVE	0241	SHYS	0010
SLIP	0297	SMIN	0003	SP	0006	SPA	2900
START	0040	SUBT	0257	TESTOP	00E2	TEST	01FA
TIME	011D	TOFF	0176	WAIT	0065		





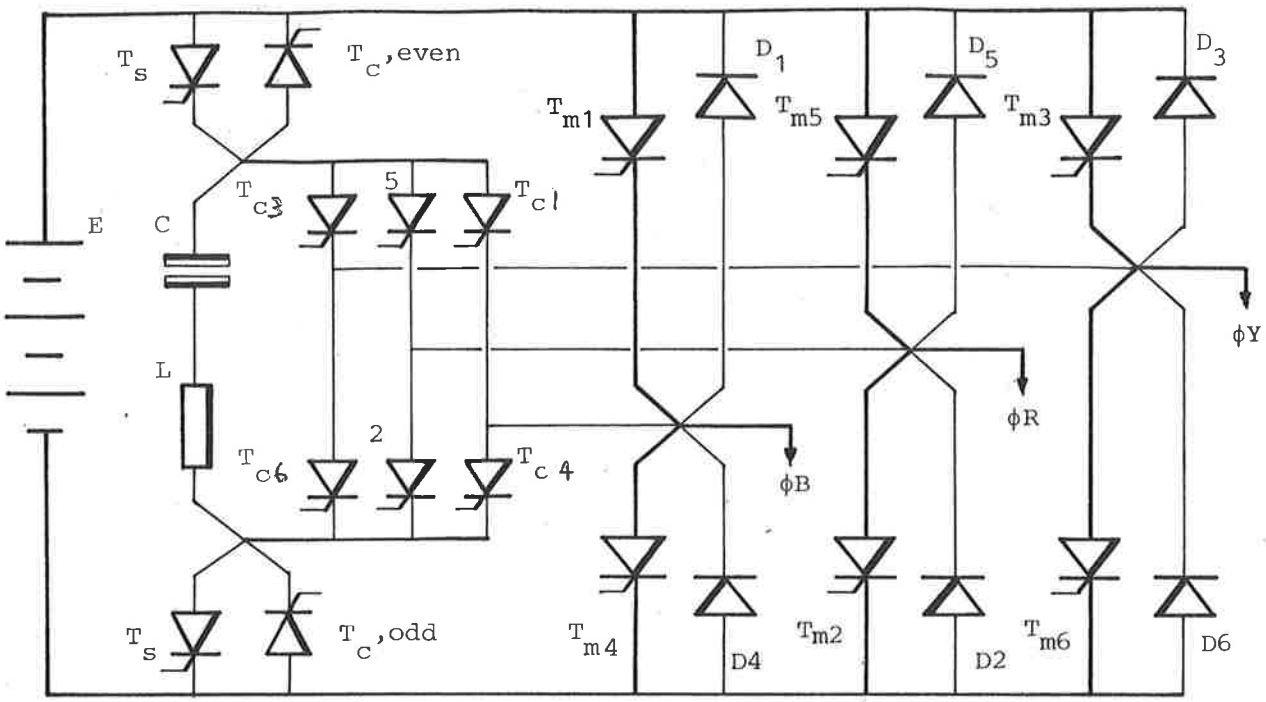


FIGURE 4.1

DC-3ϕ variable frequency static thyristor inverter circuit

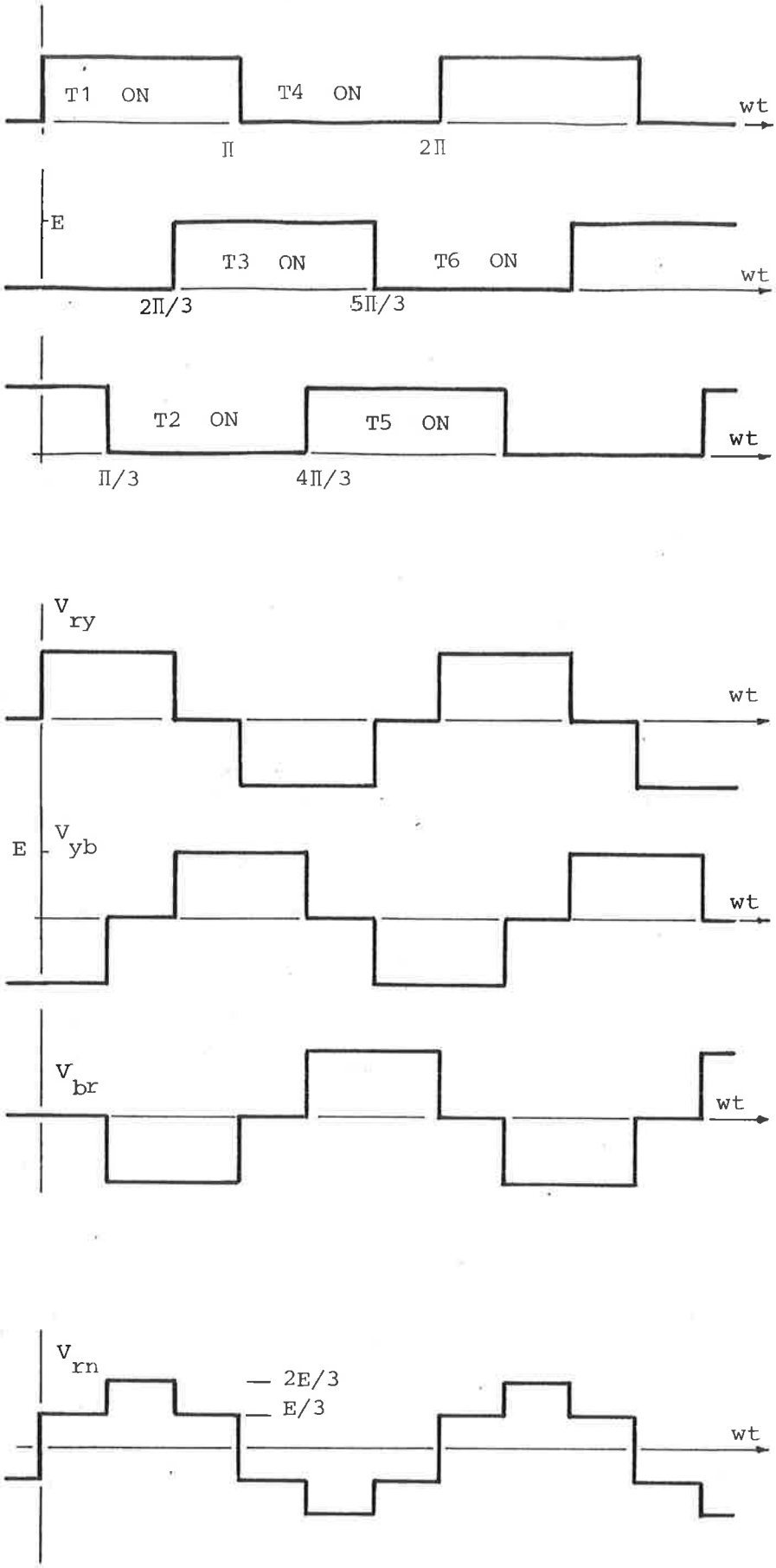


FIGURE 4.2

Gating sequence, line to line and line to neutral bridge waveforms

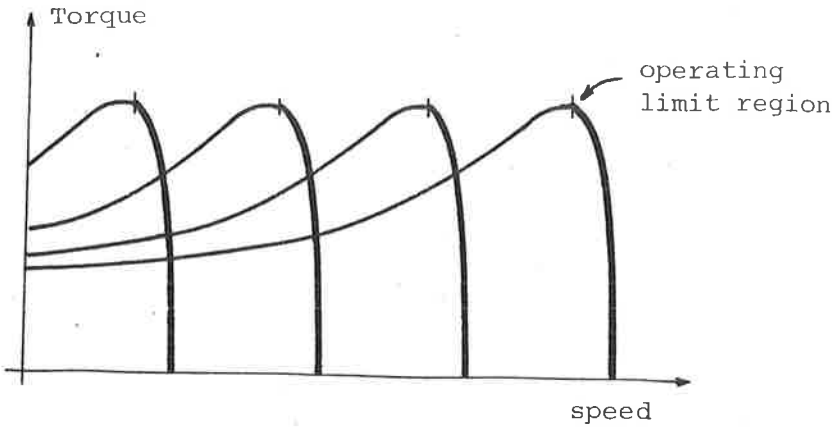


FIGURE 4.3

Induction motor torque characteristics at different frequencies and constant V/f ratio

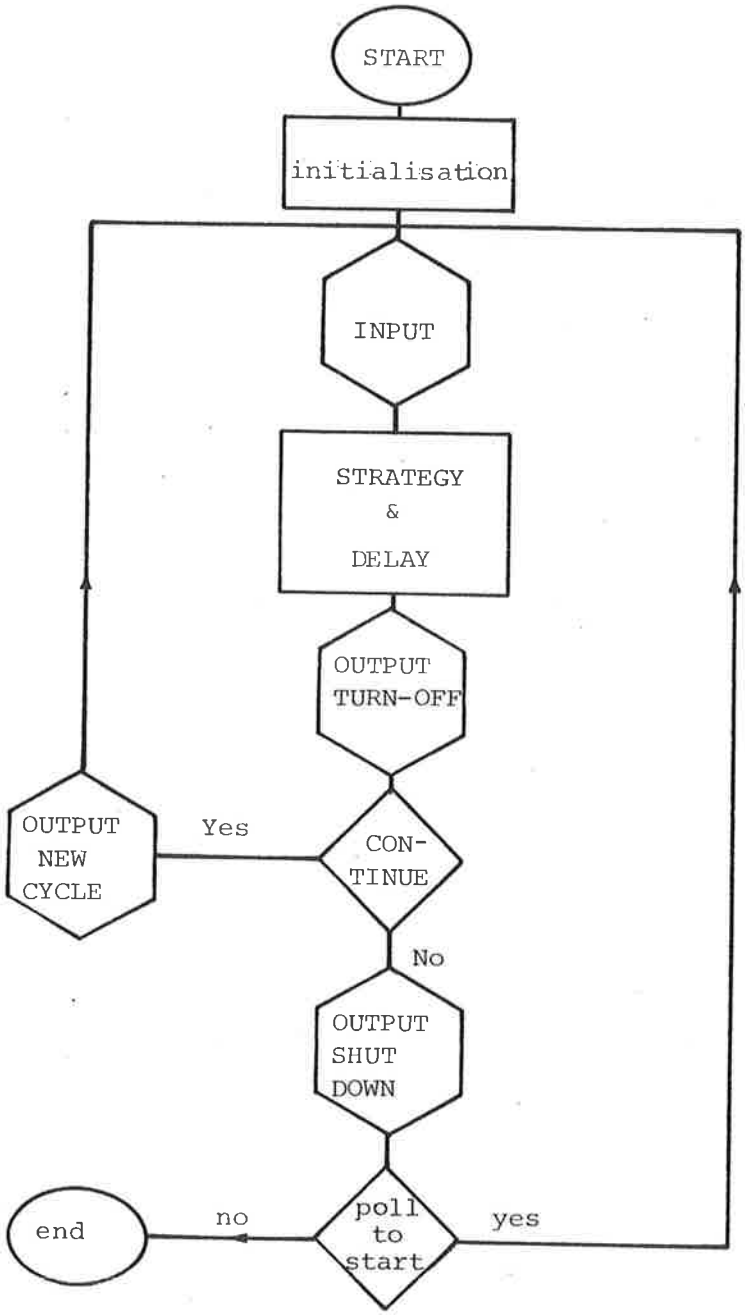
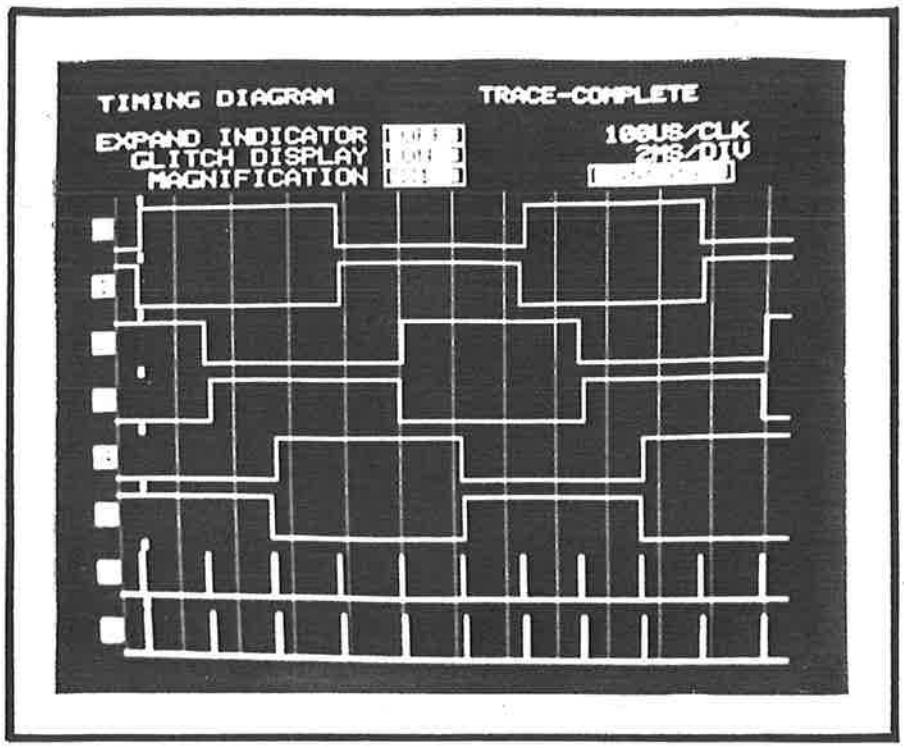


FIGURE 4.4. Program flow chart



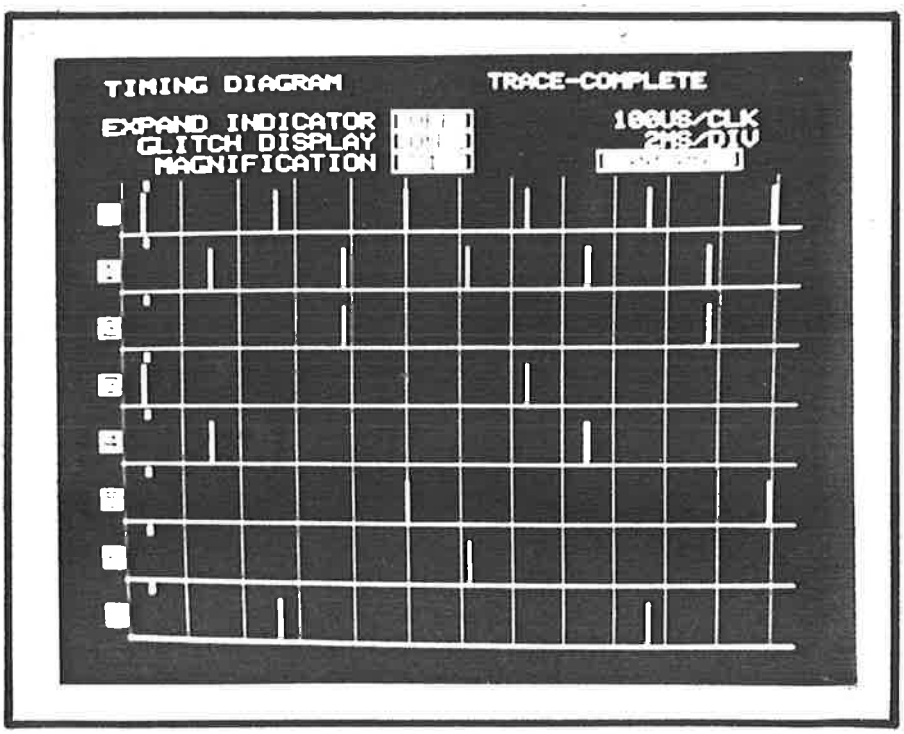


FIGURE 4.5

Bridge thyristor trigger waveforms

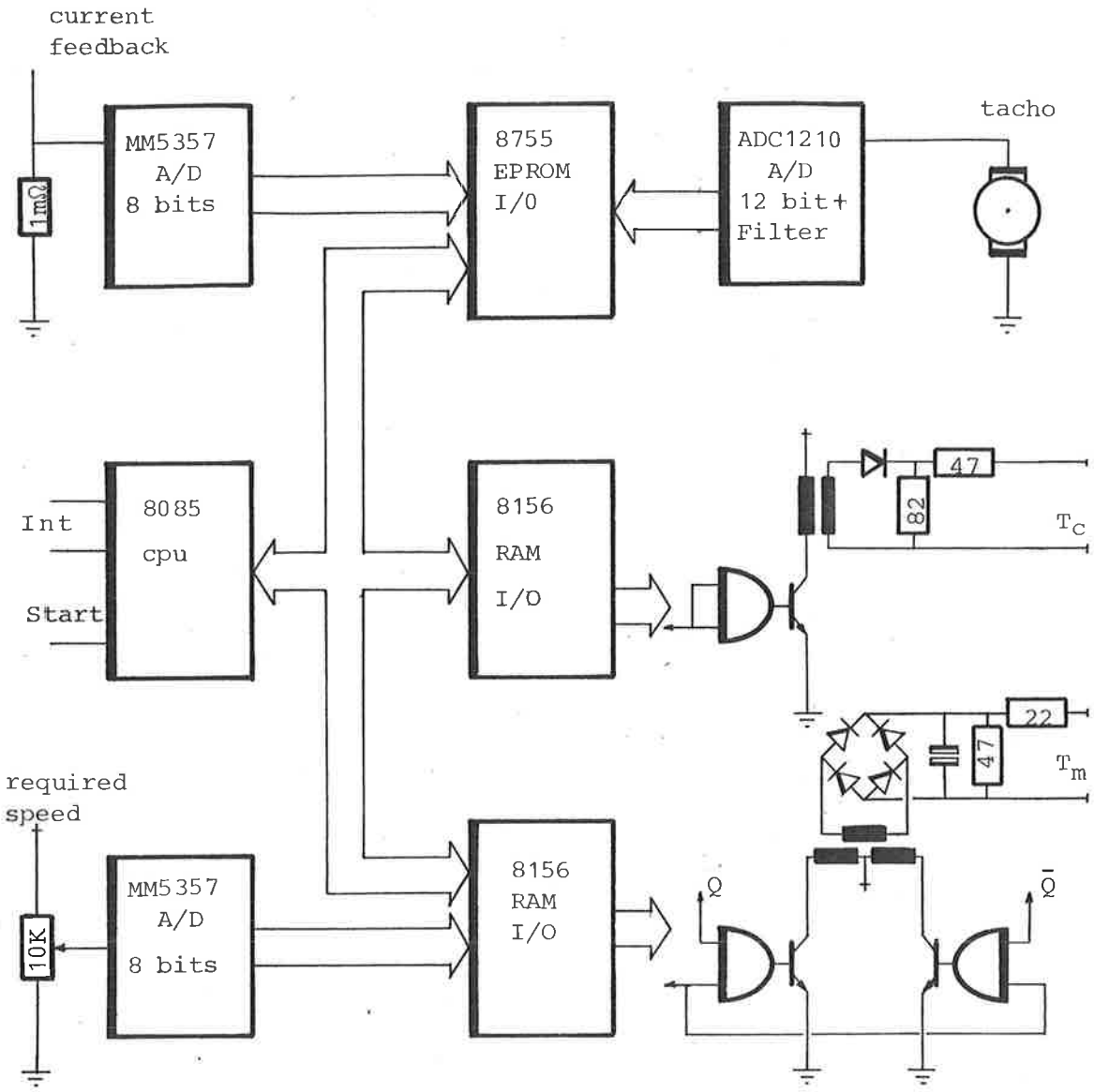
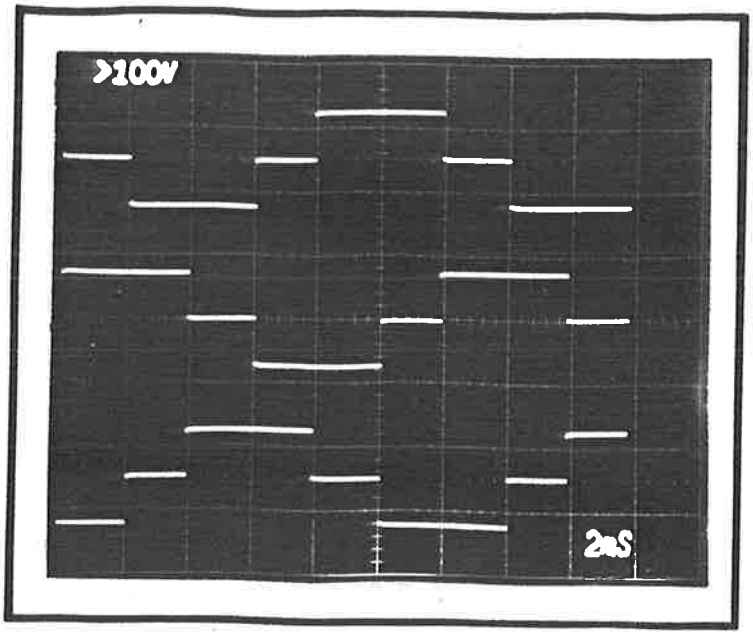
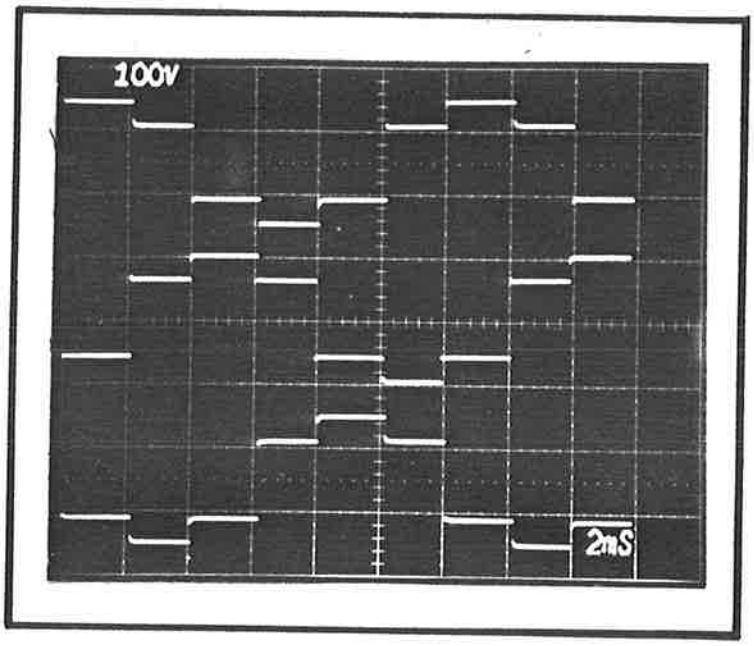


FIGURE 4.6

Microprocessor controller and interfacing



line to neutral voltages



line to line voltages

FIGURE 4.7

Inverter output voltage oscillograms
(uncompensated probes)

CHAPTER 5

CONCLUSIONS on The PRACTICAL COMMUTATION CIRCUIT

The basic thyristor commutation technique presented in this thesis has proven to be reliable, efficient and versatile. The commutating circuitry is simple, producing cheap, small and light inverter equipment. Simple circuit modifications enhance the basic features, improving output voltage regulation, operation frequency range and commutating efficiency, as discussed in Chapter 2.

The versatility and adaptability of the thyristor turn-off circuit have been illustrated by the novel a.c. triac chopper circuit of Chapter 3 and the d.c.-three-phase inverter of Chapter 4.

The unavoidable inherent problem of dynamic thyristor voltage stressing can not be eliminated, but only reduced below the critical level. This limitation of high and uncontrolled circuit re-applied dv/dt stressing is not critical in d.c. chopper applications, where a commutation failure may not be fatal. But in a.c. and inverter circuit applications a turn-off failure will generally result in semiconductor device destruction, since a short circuit across the supply results. In these

situations proper snubber protection is therefore essential.

The inverter circuit employing the above commutation technique has been shown to be an ideal vehicle for a microprocessor-based controlled-slip induction motor drive.