Capacity of Multiple-Input Multiple-Output Wireless Communication Systems Operating in the HF Band

by

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Appendix A

Multi-Channel Receiver Development

Details of the development of the MCR are provided here, and include requirements specifications, architecture of the MCR board, architecture of the full MCR system, and plots of data captures obtained during laboratory testing.

A.1 Requirements Specification

The requirements for the MCR were grouped according to the categories operational requirements, functional requirements, logical requirements, user requirements, system requirements, and subsystem requirements. Operational requirements encompass those requirements that refer to how a system is to be managed and controlled. Logical requirements are those that refer to how functional requirements are distributed amongst sub-systems. User requirements reflect the needs of the end-user in relation to the finished system. System requirements are those relating to measurable parameters of the overall system. Subsystem requirements are those relating to measurable parameters for modules of the system. The MCR requirements are provided in the following subsections.

A.1.1 Operational Requirements

An interface to control and configure characteristics of the MCR shall be implemented.

The interface of each MCR receiver section shall provide access to the selection of mode of operation; at minimum: Power-up, Reset, Configure, Run, Stop/Idle.

A.1.2 User Requirements

A data communication interface shall be implemented to link hardware subsystems to the processing subsystem.

Chirp rates of 100 kHz/s, 200 kHz/s and 400 kHz/s shall be supported by the MCR.

Raw data transmitted from the MCR shall be stored as it arrives.

The MCR shall support multi-channel operations that aim to recover a signal of interest in the presence of more highly powered near-channel interference.

The MCR chirp operation shall handle, as a minimum, FMCW signals transmitted by the LLISP network.

The MCR shall operate in office conditions for standard COTS (commercial off-the-shelf) equipment.

Specialised design and production rules, such as increased robustness or military-based MTBF (mean time between failures) and MTTR (mean time to recovery) shall not be imposed on the MCR.

A.1.3 Logical Requirements

Each MCR channeliser shall implement downconversion, coarse decimation/filtering and chirps.

Specific other functions (fine decimation, filtering and AGC (automatic gain control)) shall be performed by one or more re-programmable hardware devices.

Data serialisation and transmission shall have no mandated partition.

A.1.4 Functional Requirements

Two channelisers shall be used to simultaneously implement HF band sweeps, with one channeliser lagging the other in instantaneous frequency.

Each channeliser shall provide a chirp mode with linear increasing frequency to operate through the HF band.

The operation of each channeliser shall be synchronised to an external sync pulse and run synchronously with an externally supplied clock signal.

Operational commands issued to each channeliser shall begin execution in a predictable timeframe. Immediate commands shall begin execution within 5 ms of issue from the local client. Synchronous commands shall begin execution at the next sync pulse.

The MCR shall provide status for verification of board operations.

A.1.5 System Requirements

The MCR shall simultaneously downconvert signals from at least four synchronised digitised inputs.

The MCR shall downconvert HF signals up to 30 MHz. The sampling clock shall be an integer multiple of the required chirp rates and operate above the Nyquist sampling frequency.

After a synchronisation signal from a known timing source, MCR chirp operation shall start within 1 s.

The antenna inputs shall be $50\ \Omega$ terminated and voltage protected at 1 Vp-p, being the input range of the digitiser.

The distribution of antenna signals to multiple receivers shall be achieved with minimal loss of signal power.

The input signal from the antennas shall have been bandpass filtered, with signals up to 30 MHz not attenuated more than 3 dB, and signals above the sampling frequency attenuated at least 120 dB where aliasing would otherwise interfere with signals up to 30 MHz.

The data output shall be transmitted in a high speed serial format suitable for networking.

A.1.6 Subsystem Requirements

The channeliser shall maintain a SFDR (spur free dynamic range) of at least 120 dB along the signal processing datapaths.

The channeliser shall perform downconversion to baseband of modulated signals at centre frequencies between 2 MHz and 30 MHz and output data streams decimated to around 2 MS/s digital bandwidth.

The programmable hardware device shall be configurable to provide baseband data at sampling rates between approximately 10 kS/s and 2 MS/s per data stream.

The chirp start and end frequencies shall be settable between 2 MHz and 30 MHz to a resolution of 10 Hz and an accuracy within 1 Hz.

The chirp operation shall not accumulate an error in the calculation of current centre frequency of greater than 1 Hz over five minutes of continuous operation.

A method shall exist for selecting either digitised analog inputs or directly supplied digital inputs as the data source for the receiver section.

The MCR control interface shall be bidirectional, fast enough to facilitate both operational commands and status gathering and suited to a single master setup.

A.2 Architecture of the MCR board

The MCR board features two receiver sections, each of which comprises a quad channel DDC chip and a Stratix FPGA [85]. The DDC chips are used to apply down conversion [86] and coarse decimation filtering to the digitized antenna data. Coarse decimation filtering is performed using CIC (cascade integrate comb) filters [87]. The Stratix FPGAs are used to apply fine decimation filtering to the data outputs of the DDC chips, and format the decimated data into packets. Fine decimation filtering is performed using FIR filters. The FIR filters are implemented using cascaded polyphase structures which exploit distributed arithmetic techniques [88]. Multiple channels are interleaved through each FIR in order to save on FPGA resources. The packets of decimated data output from each Stratix FPGA are forwarded to a third Stratix FPGA which is used as a controller for the MCR board. The controller communicates with a PC running Console software via Ethernet, outputting status and decimated data packets, and receiving commands.

A block diagram of the MCR board is shown in Figure A.1.

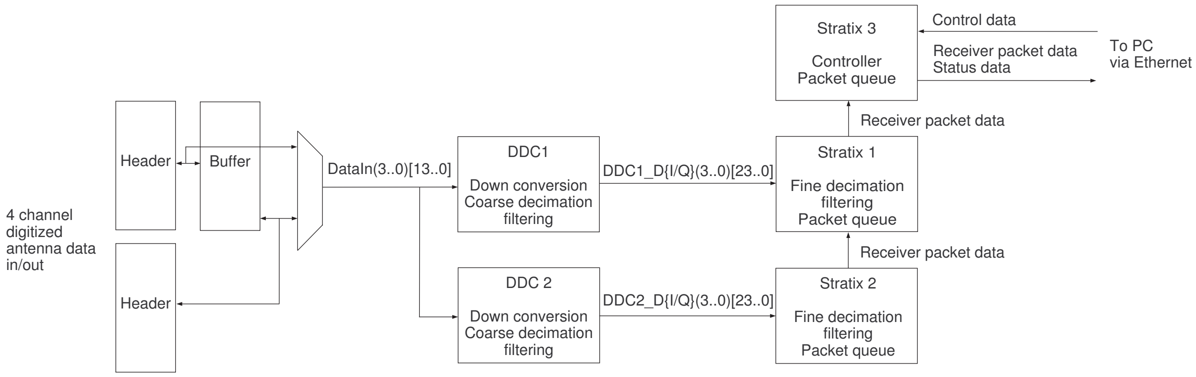

Figure A.1. Block diagram of the MCR board

A list of parts used by the MCR board is shown in Table A.1. Note that resistors, capacitors and inductors have not been included in the list. The DDC chip was designed by Kiet To of CHiPTec, which is based at the University of Adelaide.

Part Number	Description	Quantity
DDC	Quad Digital Down Converter Chip	2
EP1S60B956C7	Stratix FPGA	3
EPM3128ATC100-10	MAX3000 CPLD	1
AM29LV065DU90REI	8 Mb Flash Memory	1
IDT71V416L10PH	4 Mb SRAM	3
LAN91C111-NC	Ethernet MAC/PHY	1
JV011I21	RJ45 with integrated magnetics	1
LTC1326CMS8	Power-On Reset Controller	1
ICS8312AY	3.3 V/1.8 V Clock Buffer	3
CS44L10KZ	Headphone Amplifier	1
MAX3238EAI	RS-232 Transceiver	2
Standard Part	RS-232 DB9 Serial Port	2
IDT74LVCH16245APV	16-Bit Bi-Directional Buffer	5
PI3B16233V	32:16-Bit Mux/Demux	5
50.0MHz IQXO-71B	50 MHz Oscillator	1
MA-406-25.0M-20pF	25 MHz crystal	1
LT1083CP	Adjustable Regulator	3
637-10ABP	Heatsink	3
DIN41612	P1/2 VXI Connector	2
	PGA Socket	2
TX3-80P-D2ST-LN1	80-pin IDC TX3 RA Header	3
TX1-80SD2P1-1D	80-pin IDC TX1 Socket	2
TX1-SR80	TX1 Strain Relief	2
	40-pin Header	3
	JTAG 10-pin Male Header	2
	DC-in connector	1
	Headphone socket	1
	Button	6
	LED, Green	6
	LED, Yellow	3
	LED, Red	2
PBYR745	Diode, 7.5A	3
	Ferrite bead	5

Table A.1. Parts list for the MCR board

A.3 Architecture of the full MCR system

A block diagram of the full MCR system is shown in Figure A.2. The front-end infrastructure, provided by DSTO, includes the antenna array, protection circuitry, bandpass filters and AGC. An ADC (analog-to-digital converter) board, developed by DSTO specifically for this project, is used to digitize the four channels. The raw digital data is passed to the MCR board for down conversion and decimation filtering. The Console is used to issue commands to the MCR board and store receiver data packets. MCR data collection operations are synchronized to GPS time.

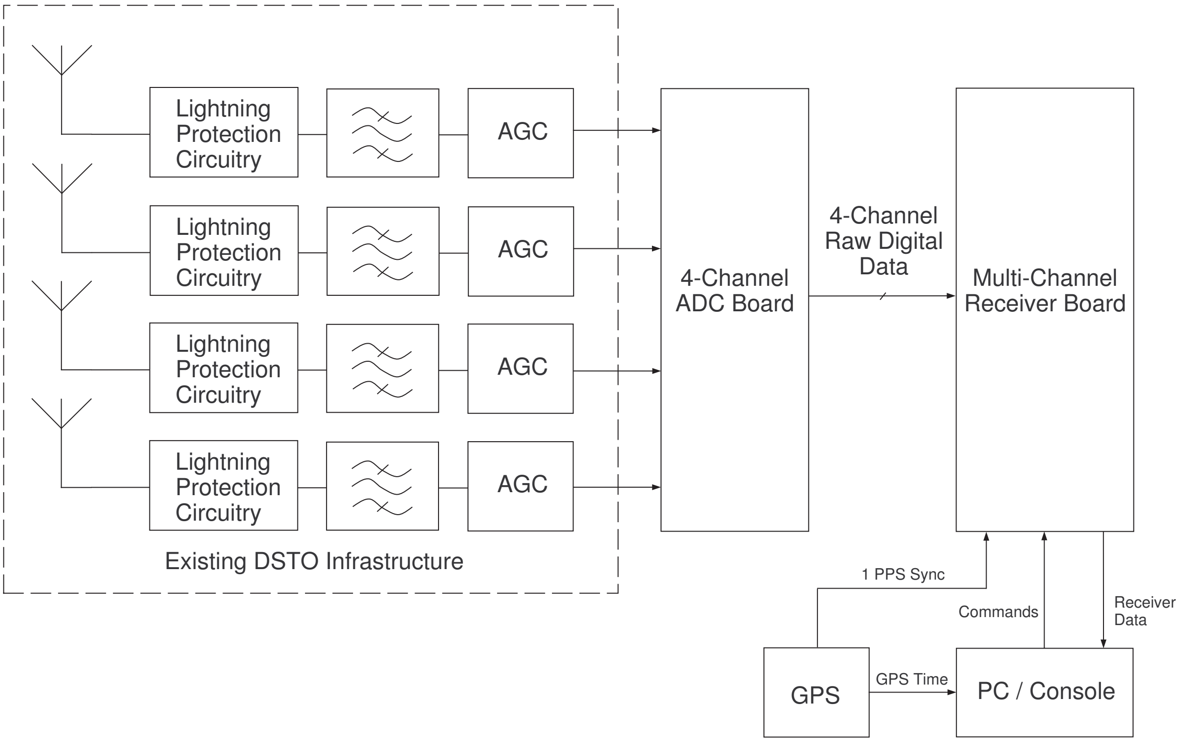

Figure A.2. Block diagram of the full MCR system

A.4 Laboratory Testing

The MCR system was tested in the laboratory with a signal generator used as input stimulus. Waveform types used for testing included fixed and stepped frequency waveforms. The system was also tested with real signals by connecting an active antenna to one of the ADC inputs and tuning to an AM (amplitude modulation) radio station. Recorded radio data was played back using the wavplay function in Matlab.

A power versus frequency plot for a single receive channel when the input signal was set to a fixed frequency, and the receive LO (local oscillator) was swept from 0 to 25 MHz, is shown in Figure A.3. The x-axis of the plot was converted from sample number into frequency by taking the sweep and sampling rates into account.

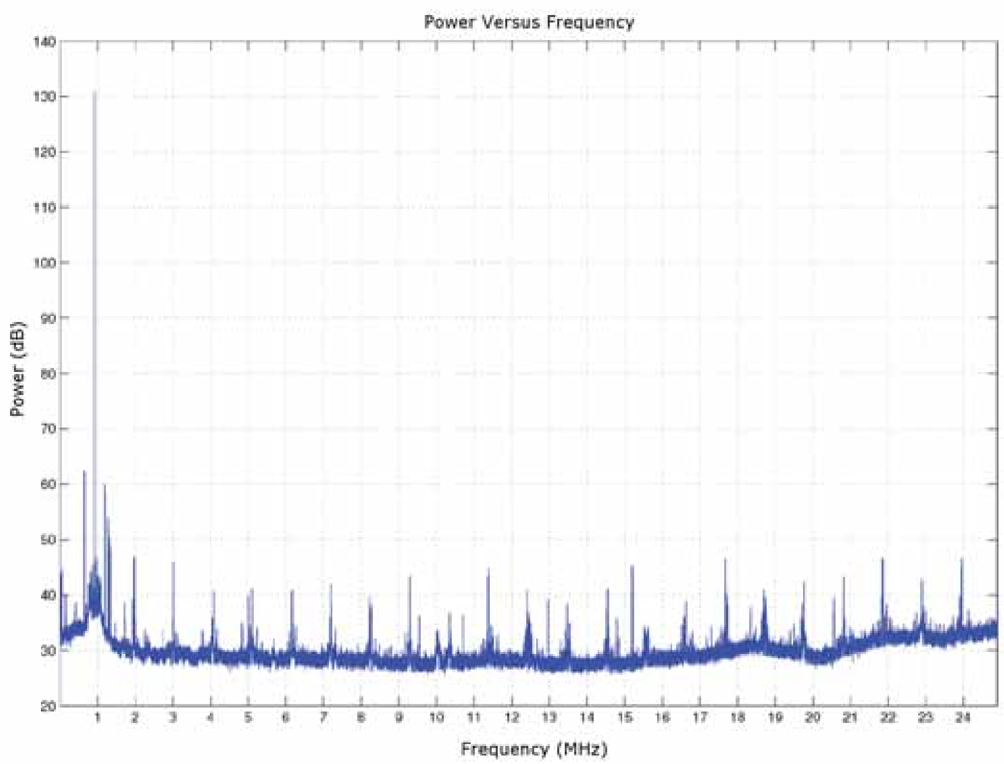

Figure A.3. Power versus frequency plot for a single 10.417 kS/s receive channel when the input signal was set to a fixed frequency and the receive LO was swept from 0 to 25 MHz

A PSD plot for a single receive channel when both the input signal and receive LO were set to fixed frequencies close in value is shown in Figure A.4. The plot shows that the input signal frequency was set approximately 150 Hz higher than the receive LO frequency.

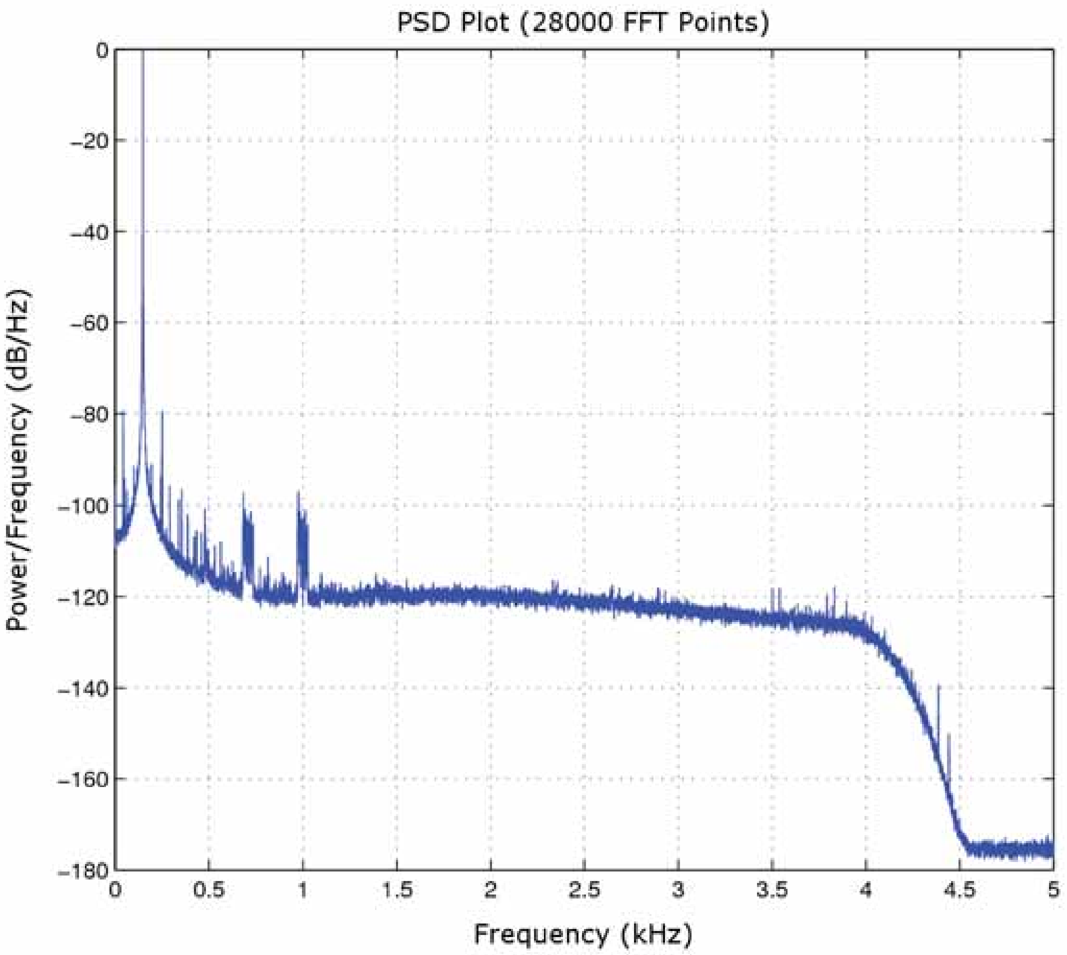

Figure A.4. PSD plot for a single 10.417 kS/s receive channel when both the input signal and receive LO were set to a fixed frequency

Passband ripple and transition band plots were generated from data captured while slowly sweeping the MCR through a fixed frequency input signal, and are shown in Figures A.5 and A.6.

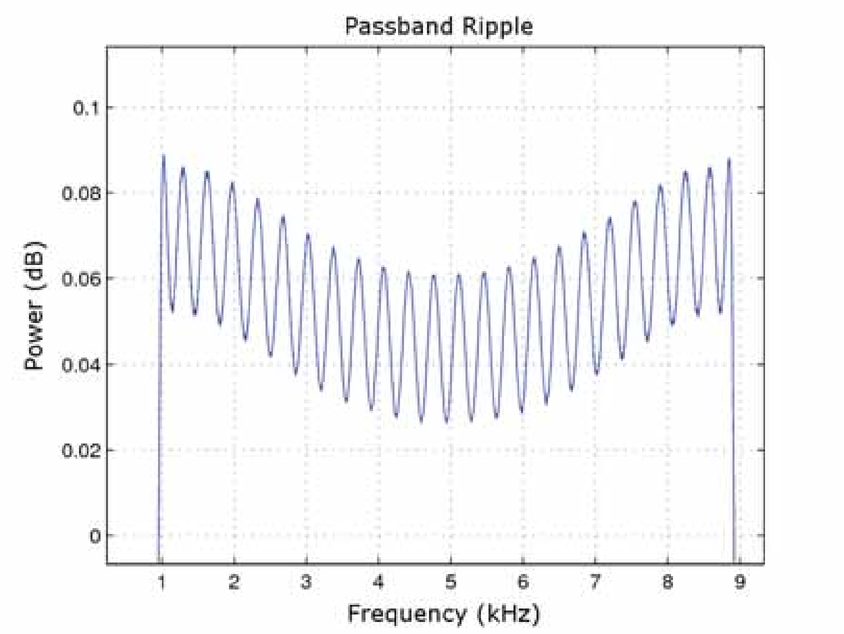

Figure A.5. Plot of the passband ripple for a single 10.417 kS/s receive channel

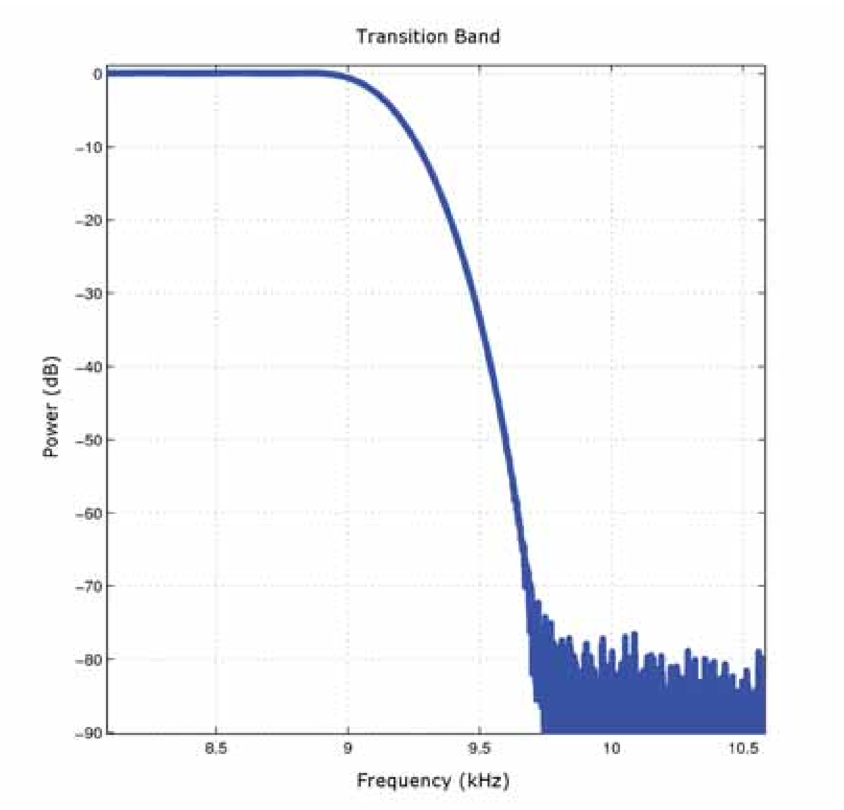

Figure A.6. Plot of the transition band for a single 10.417 kS/s receive channel

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