THE UNIVERSITY OF ADELAIDE

Low-Cost Current-Source 1-ph Photovoltaic Grid-Connected Inverter

by

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APPENDIX A

DC LINK INDUCTOR DESIGN

A.1 Inductor Design for 160 W CSI

The design of the inductor for a grid-connected PV CSI has an important trade-off with regards to its sizing : the larger the energy storage, the lower the current ripple and hence PV average power loss; but the larger the inductor's size, cost and power losses.

Dimensions of the inductor are coded to express some of the calculation formulas clearly beside the preliminary drawing of the designed inductor in Fig. A.1. The value of the inductance L is chosen such that the inductor current ripple peak magnitude is a small fraction of the maximum PV array output current. Therefore core of the inductor has to be quite big and the airgap g is employed should be sufficiently large to prevent saturation of the core by the peak current $I + \Delta I$. For this reasons the inductor consists of four (0.27 mm GOSS) "U" cores and two airgaps. Another trade-off should be noted here amongst copper losses, wire diameter and hence cost of the inductor. Therefore next section provides calculations to obtain an optimum DC link inductor for the required amount of energy storage.

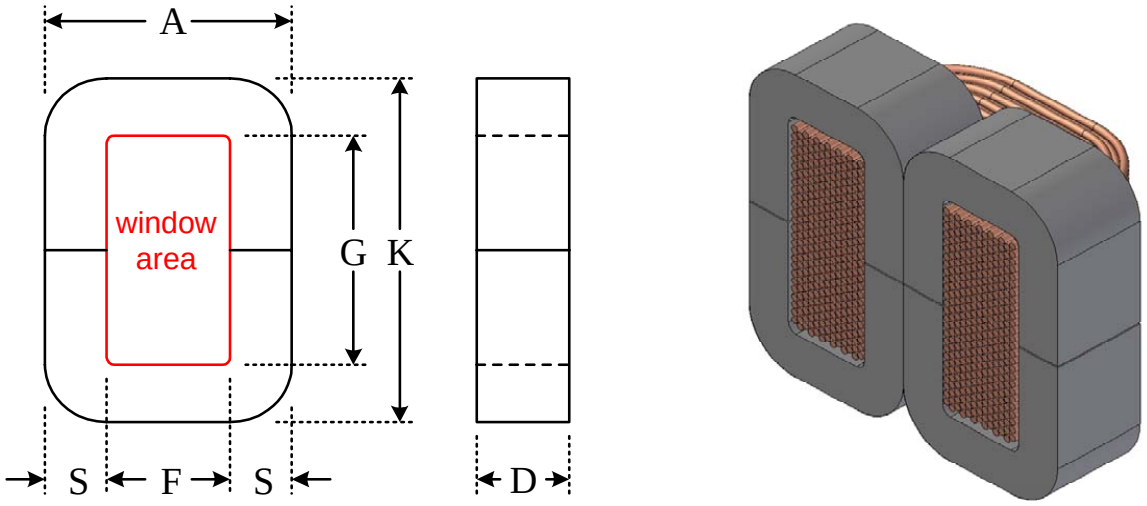


FIGURE A.1: *Dimensions for the designed inductor for calculations and sectioned inductor drawing.*

A.1.1 Inductor Volume Calculations

The energy in the inductor is generated by the current flowing through the inductor and stored in the magnetic field. Energy storage capability is increased with the volume. The volume of the inductor can be calculated if flux density and required energy storage E_0 are known. This can be done using the magnetic energy equation (A.1). The amount of magnetic flux Φ, which is the counterpart of the electric current in an electric circuit, can be expressed for per unit cross-sectional as flux density B.

$$E_0 = \frac{1}{2}\frac{B^2}{\mu_0}V \tag{A.1}$$

A.1.2 Inductor Airgap and Windings

Inductor airgap is critical that usually more energy is stored in airgap than in rest of magnetic circuit. Therefore the core can be defined as equivalent gap g_E. Hence calculation of the total gap g_T will allow us to determine g_E and actual gap value g of the inductor. This can be done using flux density equation (A.2).

$$B = \mu_0 \frac{NI}{g_T} \tag{A.2}$$

where μ_0 is the permeability of free space and N is the number of turns. In (A.2), number of turns need to be presumed as well. The relation amongst size, number of turns and

airgap can be seen here for constant current value. From the total gap value, g_E and g can be obtained in (A.3).

$$g_T = g_E + g \tag{A.3}$$

Mean core magnetic path length l_C, which is a path that follows an average magnetic field line around the interior of the core, can be found by (A.4).

$$l_C = g_E \, \mu_R \tag{A.4}$$

So far dimensions of the inductor airgap and number of turns are predicted and dimensions of the inductor can be calculated from Fig. A.1 based on the mean path length in (A.5).

$$l_C = 2\,(A + K - 2S) \tag{A.5}$$

Determination of the dimensions of the inductor yields other calculations such as packing factor.

A.1.3 Packing Factor

Packing factor pF is one of the most important design constraints of the magnetic devices. pF is the ratio of total winding area A_{WT} to core window area W_A. A_{WT} is proportional to number of turns.

$$A_{WT} = N \, A_W \tag{A.6}$$

where A_W is the radius value of the copper wire. Window area can be calculated using Fig. A.1.

$$W_A = G \, F \tag{A.7}$$

After calculating total winding area and core window area, pF can be determined from (A.8) below.

$$pF = \frac{A_{WT}}{W_A} \tag{A.8}$$

A.1.4 Copper Loss

Although inductor reduces 100 Hz fluctuations it has large copper loss which has a big fraction in the total power loss as seen in Fig. 6.15. To calculate copper loss, the mean length per turn MLT has to be determined.

$$MLT = [D + (2\,F) + (2\,S)]\,2 \tag{A.9}$$

Then it is now possible to calculate the resistance of the inductor winding from (A.10). As total winding area, wire resistance is proportional to the number of turns.

$$R_{CU} = \rho\,\frac{N(MLT)}{A_W} \tag{A.10}$$

where R_{CU} is the inductor copper resistance. As it is mentioned due to the significance of copper loss, temperature effect should be taken into account for accurate loss calculation. Assuming the nominal temperature $T_1 = 25°\text{C}$ and the maximum temperature is $T_2 = 40°\text{C}$. Hence the coil resistance at 40°C ($R_{CU(40°C)}$) can be calculated by (A.11).

$$R_{CU(40°C)} = R_{CU}\,(1 + a\,(T_2 - T_1)) \tag{A.11}$$

where a is the temperature coefficient of the copper. Hence a well-known DC power formula yields to predict possible copper loss in the inductor.

$$P_{CU} = I^2\,R_{CU(40°C)} \tag{A.12}$$

The above procedure represents a way of determining DC link inductor that is suitable for use with the proposed grid-connected inverter. Once the peak to peak ripple is determined based on (3.6), the core material size, gap value and number of windings can be obtained. Then power loss calculations and some of the constraints can be taken into account. For the sake of simplicity the design calculations are optimised and some of the constraint issues are ignored as they are not scope of this thesis. However these optimised calculations were used for the inductor which is constructed for the 160 W prototype inverter and it worked reasonably well. A summary of the calculated inductor properties, at rated power, is shown in Table A.1.

Two inductors were designed and built for the 160 W CSI inverter, one with a stored energy of approximately 1 J (1.15 J, 112 mH) and one with a stored energy of approximately 2 J (1.96 J, 192 mH). The inductors were both constrained to have copper losses which were of the order of 5 W. Their characteristics are listed in Table A.1. Both the 192 mH inductor (see Fig. A.2) and the 112 mH inductor are designed for the rated PV array current (I_0) that corresponds to peak power (P_0). The calculated peak to peak current ripple ($\Delta I/I_0$) is around 13% for the large inductor.

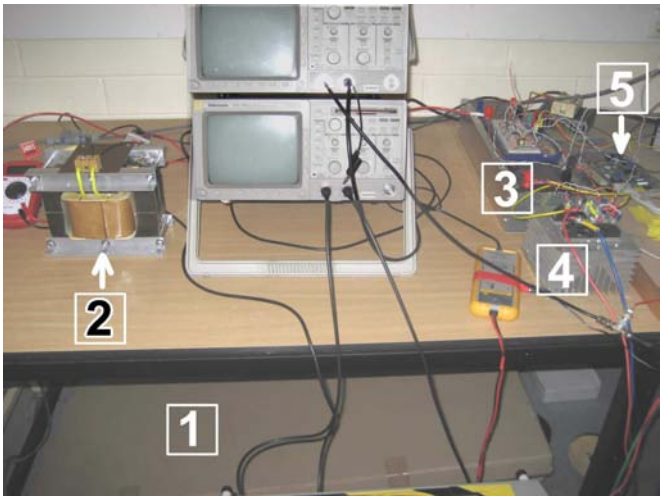


FIGURE A.2: *Grid-connected CSI test arrangement showing light covered PV modules (1), the 192 mH inductor (2), current wave-shaper (3), thyristor based inverter (4) and microcontroller (5).*

TABLE A.1: *Parameters of the two inductors for the proposed CSI.*

Parameter	Inductor 1	Inductor 2
Rated maximum input power (P_0)	160 W	160 W
Input current for P_0 (I_0)	4.5 A	4.5 A
Input voltage (V_0)	35 V	35 V
Inductance (L)	112 mH	192 mH
Stored energy	1.15 J	1.96 J
Diameter of the copper wire	2.4 mm	2.4 mm
Number of turns (N)	249	200
Resistance at 40°C(R_{CU})	0.25 ohm	0.324 ohm
Power losses in the inductor (P_{CU})	5.0 W	6.7 W
Current ripple (peak-to-peak)	21.3 %	12.8 %
Peak flux density (B)	1.5 T	1 T
Copper winding packing factor	0.46	0.37
Volume	0.00052 m^3	0.0021 m^3
Mass	5.5 kg	15.5 kg

A.2 Experimental Results

Fig. A.3 shows the measured inductance versus AC rms current. Two measurement methods were used, firstly instantaneous flux-linkage λ based on integrating $v(t)$ - $i(t)$R, and secondly using AC reactance. Both methods gave similar results.

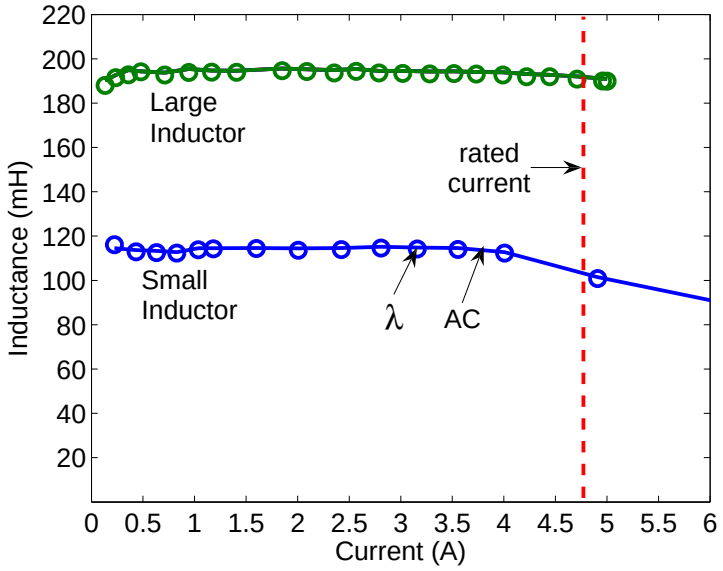
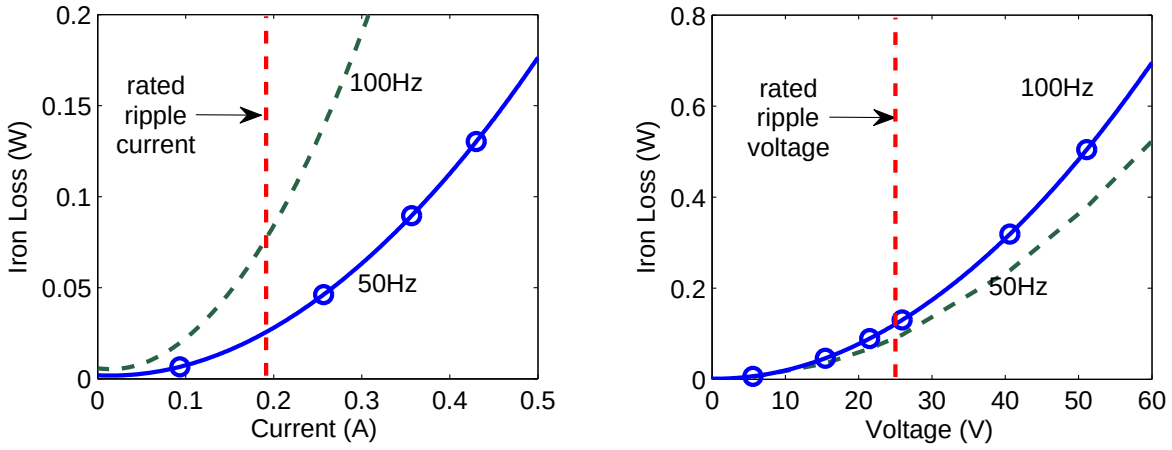


FIGURE A.3: *Measured inductance of the two different DC link inductors.*

Up to this point the inductor losses are assumed to be resistive (copper losses), however the inductor core also has iron losses which include hysteresis and eddy-current losses. Iron losses also increase the effective resistance of the coil even at low frequencies. At high frequencies the skin effect leads to big reductions in the effective cross-sectional area of the wire and the resistance of a coil is often many times greater than its DC value.

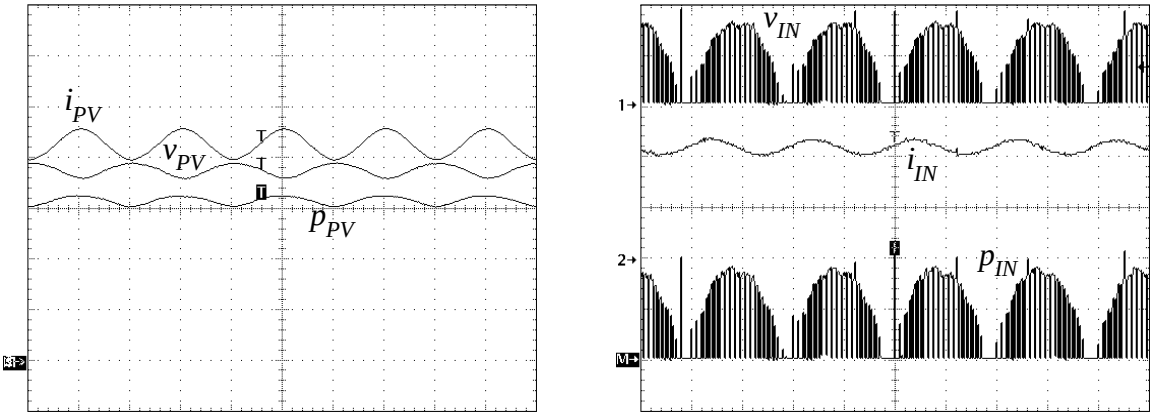
Fig. A.4 shows the measured larger (192 mH) inductor iron losses at 50 Hz, as a function of both current and voltage. Presuming that half of the iron loss is hysteresis and the other half is eddy-current, the losses with the 100 Hz fluctuation was consistently estimated at about 0.08 W from both the rated inductor current and voltage ripple (see Table A.2) at MPP.

The indicated power variations in Fig. 3.5 (see Chapter 3) can also be seen in Fig. A.5. The figure shows the measured PV cell voltage, current and power waveforms. Fig. A.5(b) shows the measured waveshaper input voltage, current and power waveforms.



(a) (b)

FIGURE A.4: *Iron loss vs.* (a) *coil current and* (b) *voltage for the 192 mH inductor. Measured 50 Hz test points (circles) and estimated 100 Hz loss (dashed line)* .



(a) (b)

FIGURE A.5: *The measured PV array output current, voltage and power waveforms (the vertical scales are 1 A, 10 V and 50 W, and horizontal scale is 5 ms per division)* (a), *the measured WS input voltage, current and power waveforms (the vertical scales are 50 V, 2 A and 200 W, and horizontal scale is 5 ms per division respectively)* (b).

Table A.2 provides the simulation and test results for the 160 W (using the first prototype with two series BP380U PV modules in this case before second prototype was constructed) current-source GCI describing the PV array ripple and the inductor losses. The measured PV array current ripple (13.4%) shows a good correspondence with the simulated results (13.0%) however the measured voltage ripple was much less than the calculated value. This is likely to be due to bandwidth issues associated with the constant-current power supply used for the dark I-V arrangement. This power supply has output capacitance which reduces its output impedance at 100 Hz. When the constant-current power supply was connected directly to the PV array, the measured voltage ripple was

TABLE A.2: *160 W inductor measured results.*

	192 mH Inductor	
	Calculated	Tests
Maximum Power Point		
V_{PV}	38.3 V	36.97 V
I_{PV}	4.33 A	4.39 A
P_{PV}	166.6 W	162.9 W
PV array ripple analysis		
v_{PV} (p-p)	12.7 %	7.6 %
i_{PV} (p-p)	13.0 %	13.4 %
p_{PV} (p-p)	2.65 %	6.10 %
p_{LOSS} (ripple)	1.33 %	3.10 %
Total PV power reduction	2.22 W	5.00 W
Inductor losses		
DC copper loss	6.07 W	5.86 W
100 Hz copper + iron loss	0.09 W	0.15 W
PWM loss	-	0.10 W
Total inductor loss	6.16 W	6.11 W
PV array power reduction and inductor losses	8.38 W	11.11 W

only about 30% of the simulated value. A 12 Ω resistor was then inserted between the power supply and the PV array in order to increase its high-frequency output impedance which increased the measured PV array voltage ripple to 60% of the simulated value. This confirmed the output impedance issue. Unfortunately it was not possible to use higher value series resistances due to output voltage constraints of the power supply. This effect also caused the PV array output power reduction to have significant error as it was assumed that the power reduction was equal to half the peak to peak ripple in the instantaneous PV array power.

The inductor loss breakdown was done by using power analyzer (Voltech-PM3000A). The 100 Hz copper and iron losses have been acquired by using the power analyzer's harmonic analysis of the voltage and current waveforms. The PWM losses were determined as the difference between the total measured losses and the sum of the measured DC and 100 Hz losses.

A.3 Conclusion

The analysis and design of the DC link inductor for a single-phase photovoltaic grid-connected inverter was examined. The key results are as follows :

- there is a trade-off between the inductor size and the PV average power reduction;
- a 100 mH and a 200 mH DC link inductor was designed and built for a 160 W inverter;
- the inductor losses are largely resistive due to the large DC current component;
- there was a good correspondence between both the measured and calculated PV array output current ripple and the inductor losses.

APPENDIX B

DESIGN SCHEMATICS AND CONTROLLER CODE

B.1 Design Schematics

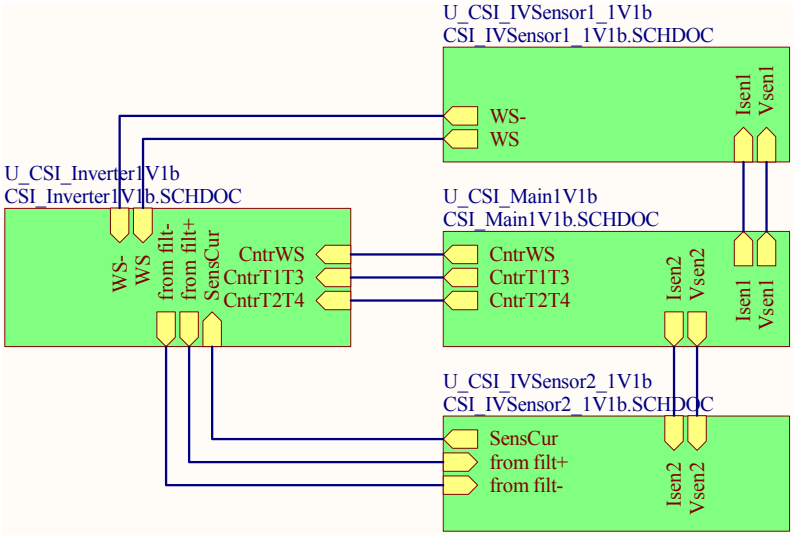


FIGURE B.1: *Master file of the PCB design which shows the circuit connections.*

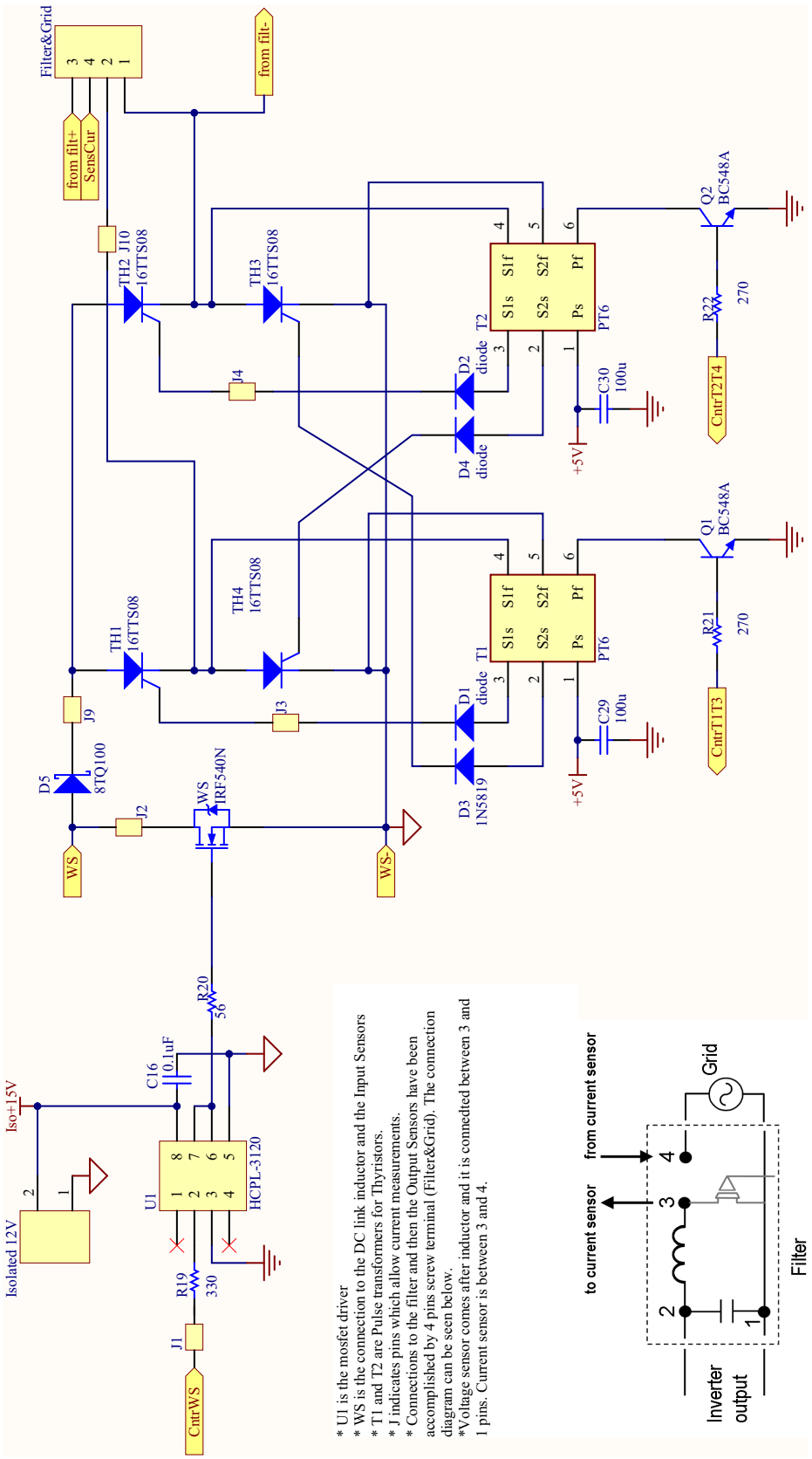


FIGURE B.2: *The CSI circuit schematic showing the WS, unfolding circuit and pulse transformers. In addition the output filter connections and sensor positions are illustrated.*

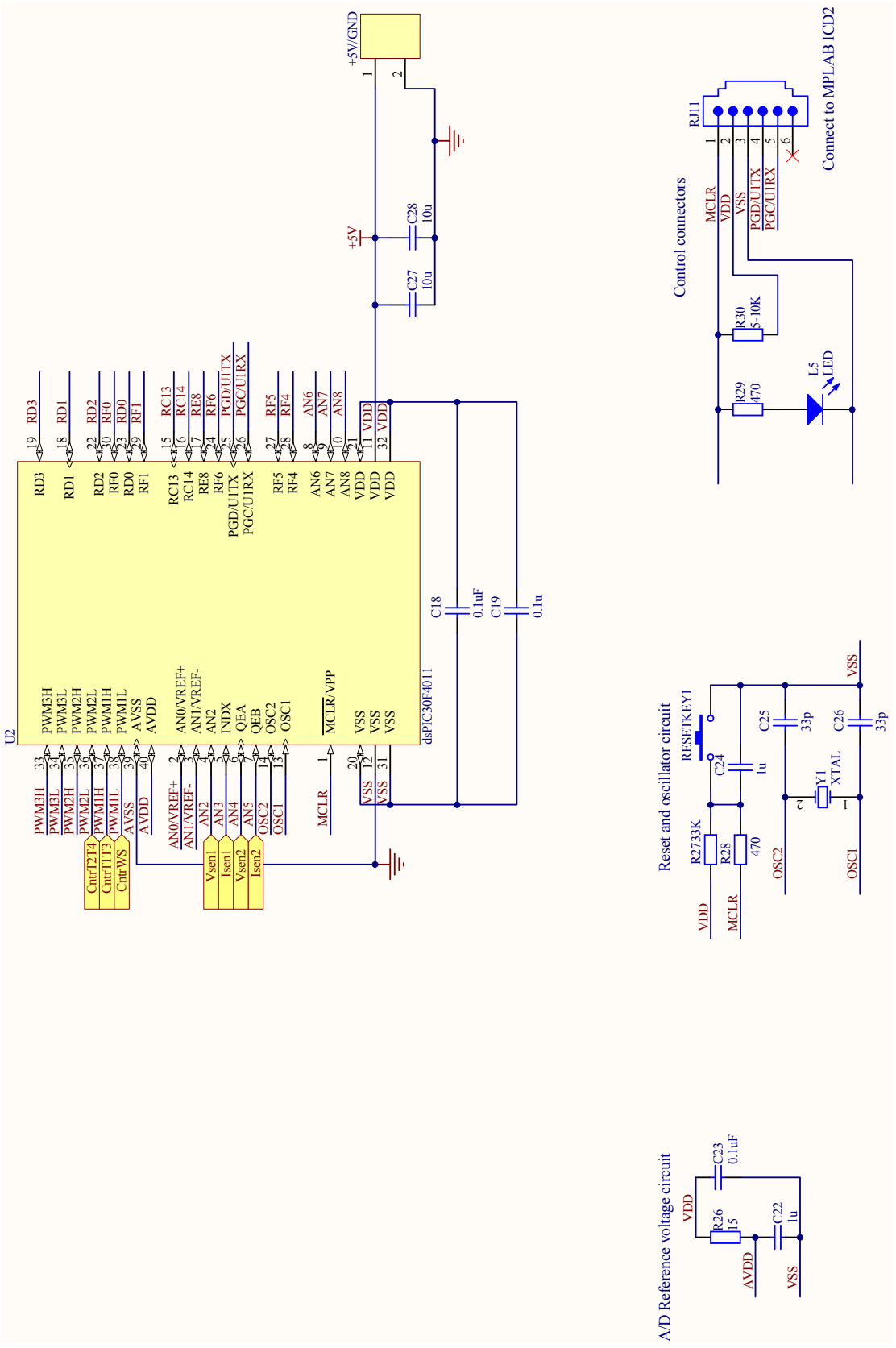


FIGURE B.3: *Microcontroller and its connections including external debugger/programmer, reset and oscillator circuits.*

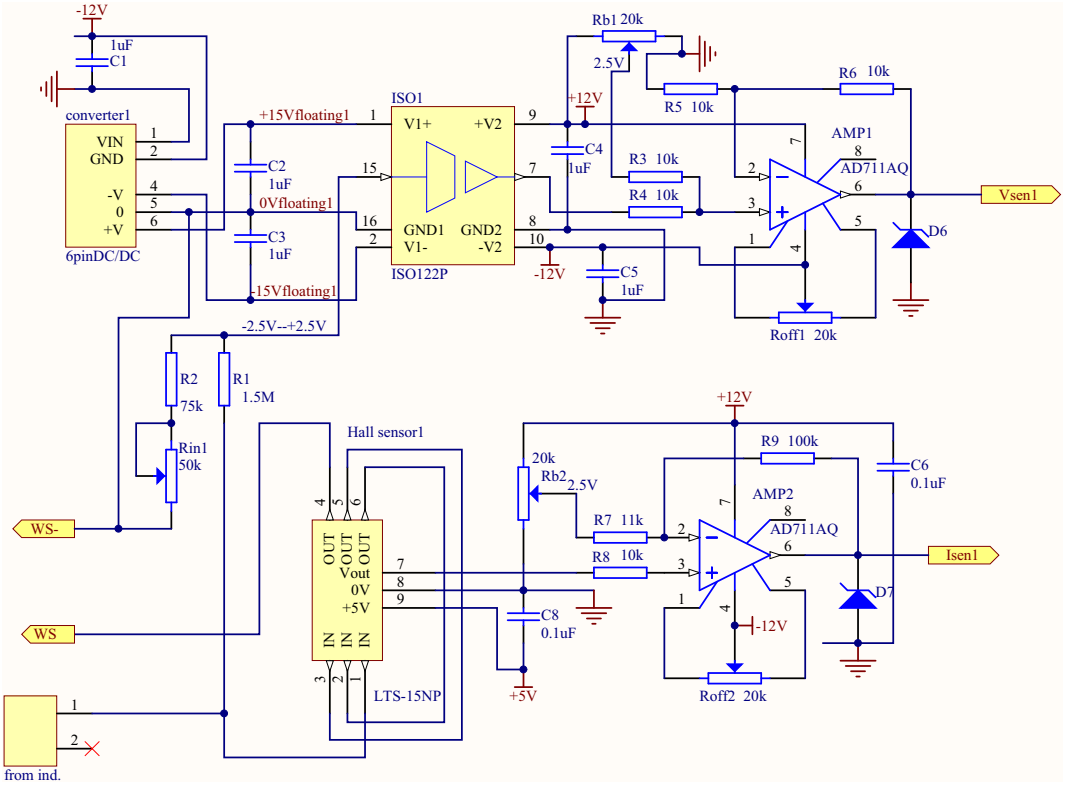


FIGURE B.4: *The input current and voltage sensors after the DC link inductor. The current sensor was used for the feedforward control.*

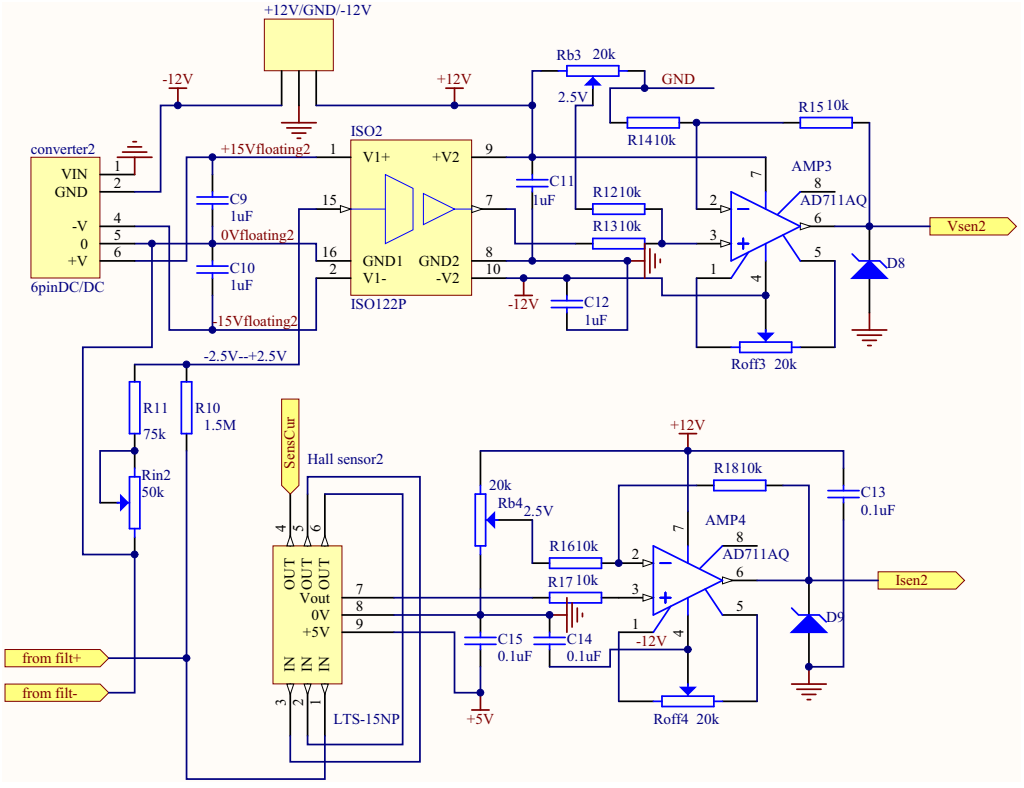


FIGURE B.5: *The output current and voltage sensors after the low-pass filter. These two sensors were not used. They have been included for future control implementations.*

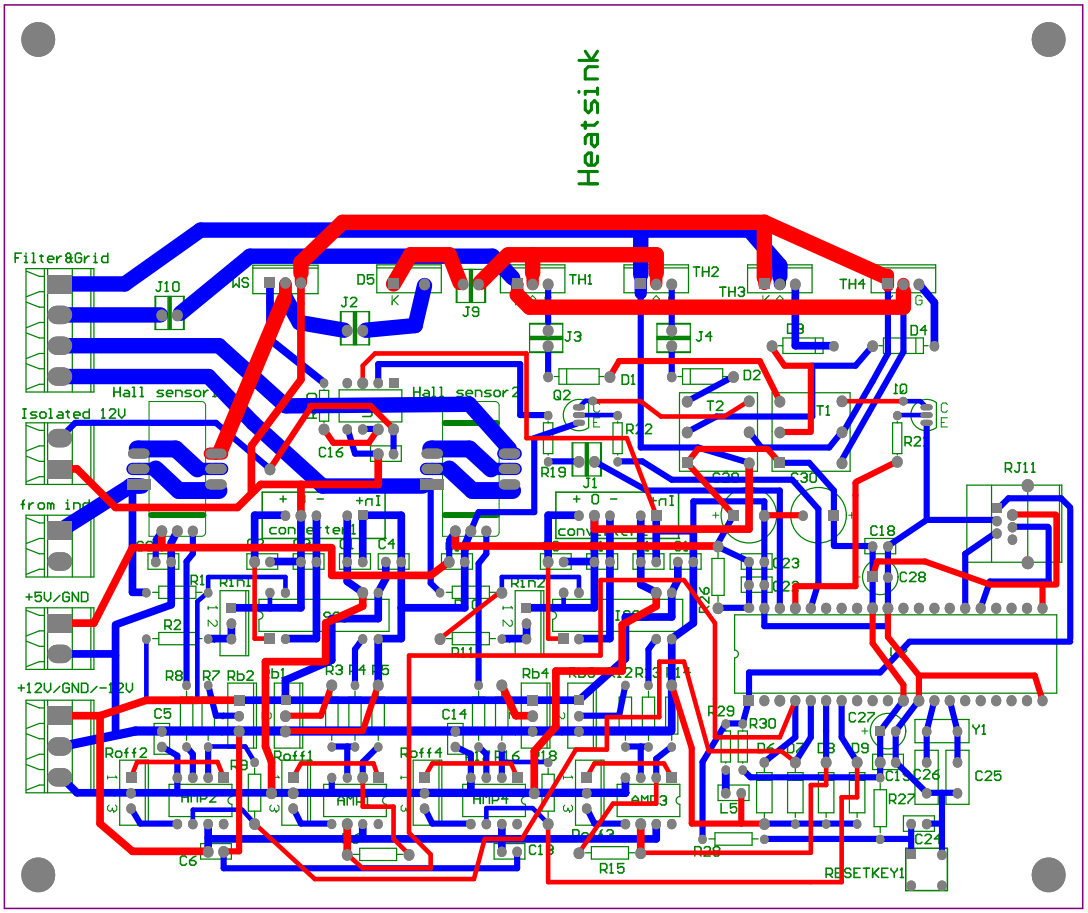


FIGURE B.6: *PCB layout of the proposed inverter.*

B.2 Microcontroller Code

The listed C code was used by the microcontroller to utilise feedforward control algorithm.

```
#include <p30f4011.h>

/* OSCILLATOR CONFIGURATION */
_FOSC(CSW_FSCM_OFF & XT);
_FWDT( WDT_OFF);
//invert polarity of PWM signals
_FBORPOR(PBOR_OFF & MCLR_DIS & PWMxH_ACT_LO & PWMxL_ACT_LO);

#define PLL_Mult 1                          //PLL multiply
#define Crystal 16000000                    //Crystal frequency
#define FCY (Crystal/4)*PLL_Mult            //4 MIPS for 16 MHz PLLx1
#define FPWM 4000                           //4 kHz
#define THYR_ON 20000                       //20 kHz to get 50us
#define phase 0                             //phase of ZCD synchronization

//PORTE Register bits
#define RE0    0x0001
#define RE1    0x0002
```

```
#define RE2    0x0004
#define RE3    0x0008
#define RE4    0x0010
#define RE5    0x0020
#define RE8    0x0100

//PORTF Register bits
#define RF0    0x0001
#define RF1    0x0002
#define RF2    0x0004
#define RF3    0x0008
#define RF4    0x0010
#define RF5    0x0020
#define RF6    0x0040

//Macro NEXT_DUTY_CYCLE moves scaled sinetable[pindex] to PDC1
#define NEXT_DUTY_CYCLE {\
asm ("PUSH.D  W0"); \
asm ("RLNC    _pindex,WREG");    \
asm ("MOV   #_sinetable,W1"); \
asm ("MOV    [W0+W1],W1");    \
asm ("INC    _pindex");       \
asm ("MOV    _ModulationIndex,W0"); \
asm ("MUL.UU  W0,W1,W0"); \
asm ("MOV   W1,PDC1");   \
asm ("POP.D   W0" );\
}

/*
asm ("PUSH.D  W0");                                 //save W0,W1
asm ("RLNC    _pindex,WREG");                       //pindex*2->W0
asm ("MOV   #_sinetable,W1");                       //address of sintable ->W1
asm ("MOV    [W0+W1],W1");                          //sinetable[pindex]->W1
asm ("INC    _pindex");                             //pindex++
asm ("MOV    _ModulationIndex,W0");                 //ModulationIndex ->W1
asm ("MUL.UU  W0,W1,W0");                           //sintetable[pindex]*ModulationIndex->W0,W1
asm ("MOV   W1,PDC1");                              //high word of multiplication ->PDC1
asm ("POP.D   W0" );                                //restore W1,W0
*/

unsigned int pindex;                                //used only inside interrupts
unsigned int ZDC_delay;                             //delay in us from ZCD pulse to synchronization
unsigned int NextThyr;
unsigned int LastPORTE;
unsigned int NeedCalculation=0;
//unsigned long Temp;                               //use in ISR only

/* HALF SINUSOID LOOKUP TABLE */
unsigned int const sinetable100[80]={0,161,321,479,633,784,929,1069,
    1201,1326,1442,1549,1646,1732,1807,1870,1921,1960,1985,1998
    ,1998,1985,1960,1921,1870,1807,1732,1646,1549,1442,1326,1201,1069,
    929,784,633,479,321,161,0, /*begin copy of the first part*/
    0,161,321,479,633,784,929,1069,
    1201,1326,1442,1549,1646,1732,1807,1870,1921,1960,1985,1998
    ,1998,1985,1960,1921,1870,1807,1732,1646,1549,1442,1326,1201,1069,
    929,784,633,479,321,161,0};
unsigned int sinetable[80];                         //sinetable in RAM
unsigned int ModulationIndex;

unsigned int Vsen1=0;
unsigned int Isen1=0;
unsigned int Vsen2=0;
unsigned int Isen2=0;

unsigned long PDClong=0;
unsigned long MpyResult=0;
unsigned int Idesired=800;                          //desired value (Vo(opamp)/Vref(AVdd))*1024
//unsigned int Isensed=111;                         //example only to test multiplication and division
```

```
void CopySineTable();
void InitADC();


/* MAIN ROUTINE */
int main(void)
{
    InitADC();
  CopySineTable();                          //sinetable for 100 percent from Flash to RAM
  // set duty cycle
  ModulationIndex=0xffff;                   //gives about 100 percent modulation index
  ...
  //ModulationIndex=0x28F;                  //gives 1 percent modulation index

  PTCONbits.PTEN=0;                         //resetting PTCON
  PTCON=0x0000;
    PTPER=(FCY/FPWM)-1;                     //sinusoidal PWM signal period
  SEVTCMP=0x0000;
  PWMCON1bits.PEN1L=1;
  PWMCON1bits.PEN3H=1;
  PWMCON1bits.PMOD1=1;
  // use PWM channel 3:PWM3H
  PWMCON2=0x0000;
  DTCON1=0x0000;                            //no dead time is controlled
  FLTACON=0x0000;                           //no fault input used
  LATEbits.LATE0=1;
  TRISEbits.TRISE0=0;
  TRISEbits.TRISE3=0;
  TRISEbits.TRISE2=0;
  TRISEbits.TRISE4=0;
  TRISEbits.TRISE5=0;
  PDC1=0x0000;                              //clear PDC1 values
  PDC3=2000-150;                            //rising edge shortly before end of PWM cycle
  IFS2bits.PWMIF=0;                         //clear pending interrupts
  IEC2bits.PWMIE=1;                         //setting interrupt for PWM signals
  IFS1=0x0000;                              //clearing external interrupt flag
  INTCON2bits.INT1EP=1;                     //falling edge of INT1
  NextThyr=RE2;                             //start with this thyristor pair
  PTCONbits.PTEN=1;                         //set PTCON

  //timer1 responsible for resetting thyristor signals after some time
  T1CON=0;                                  //init timer1: prescaler 1:1 internal clock
  TMR1=0;
  PR1=(FCY/THYR_ON)-1;                      //50 us period
  IFS0bits.T1IF=0;                          //clear interrupt flag
  IEC0bits.T1IE=1;                          //enable timer interrupt
  //do not start timer!!! timer is started in INT2 interrupt

  //timer3 responsible for delaying ZDC pulse by 10 ms+-some us
  ZDC_delay=19850;                          //initialize delay variable delay=us
  T3CONbits.TON=0;
  T3CON=0b00010000;                         //prescaler 1:8; one tick = 2 us at 4 MHz fcy
  TMR3=0;
  PR3=(ZDC_delay/2)-1;                      //set delay in us
  IFS0bits.T3IF=0;                          //clear interrupt flag
  IEC0bits.T3IE=1;                          //enable timer3 interrupt
  //do not start timer!!! timer is started in INT1 interrupt

  IEC1bits.INT1IE=1;                        //enabling interrupts for ZCD

#if __DEBUG
  //use timer2 to get interrupt every cycle 20 ms = 50 Hz
  //grid can be 49 Hz...51 Hz
  T2CON=0;
  TMR2=0;
  T2CON=0b00100000;                         //prescaler 1:64
  PR2=(FCY/64)/50-1;                        //50 Hz
  //PR2=(FCY/64)/49-1;                      //49 Hz
  IFS0bits.T2IF=0;                          //clear interrupt flag
```

```
  IEC0bits.T2IE=1;                                  //enable interrupt
  T2CONbits.TON=1;                                  //start timer

  LATFbits.LATF0=0;
  TRISFbits.TRISF0=0;
  LATFbits.LATF1=0;
  TRISFbits.TRISF1=0;
#endif

  while (1)
  {
    if (NeedCalculation!=0)
    {
      NeedCalculation=0;

    MpyResult=(unsigned long)PDC1*(unsigned long)Idesired;
    if (Isen1==0)
    {
        PDC1=2000;
    }
    else
    {
      PDClong=MpyResult/Isen1;                      //32bits/16bits->32bits result
      if (PDClong>2000)
      {
         PDClong=2000;
      }
      PDC1=(unsigned int)PDClong;
    }
    ADCON1bits.SAMP=0;                              //start A to D conversion
  };
  };
}                                                   //main loop end

void _ISR _PWMInterrupt(void)
{
  // PWM interrupt is also falling edge of PWM1L
  // fire tyristors here
  LATE=NextThyr;
  T1CONbits.TON=1;                                  //start timer1; 50 us

  if (pindex == 40)
  {
      NextThyr=RE3;
  }
  if (pindex==80)
  {
    NextThyr=RE2;
    pindex = 0;                                     //reset after 80 values
  }
  NEXT_DUTY_CYCLE;
  NeedCalculation=1;
  IFS2bits.PWMIF=0;    //clear pending interrupts
}


void _ISRFAST _T3Interrupt (void)
{
    T3CONbits.TON=0;                                //disable timer
    TMR3=0;                                         //reset timer-register
    LATF^=RF1;                                      //testing interrupt

    //start synchronization here
    PTCONbits.PTEN=0;                               //resetting PTCON
    pindex=phase;                                   //phase = 0,1,2...
    //PDC1=sinetable[pindex++];                     //load initial duty cycle
    NEXT_DUTY_CYCLE
    PTMR=0x0000;                                    //clear PWM timer
    IFS2bits.PWMIF=0;                               //clear pending interrupts
```

```
    PTCONbits.PTEN=1;                           //set PTCON
    //PDC1=sinetable[pindex++];                 //next index from the sine table
    NEXT_DUTY_CYCLE
    NextThyr=RE2;                               //start with this thyristor pair
    IFS0bits.T3IF=0;                            //clear interrupt flag
}

void CopySineTable()
{
  int i;
  for (i=0; i<80; i++)
  {
    sinetable[i]=sinetable100[i];
  }
}

void InitADC()
{
    //reference voltage selection: use AVDD and AVSS
    ADCON2bits.VCFG=0b000;

    //negative inputs to channels CH1,CH2,CH3=-Vref-
    ADCHSbits.CH123NA=0b00;
    //negative input to CH0 is Vref-
    ADCHSbits.CH0NA=0b0;

    //positive inputs to CH1,Ch2,CH3 are AN3,AN4,AN5
    ADCHSbits.CH123SA=0b1;
    //positive input to CH0 is AN2
    ADCHSbits.CH0SA=2;

    //simultaneous sampling
    ADCON1bits.SIMSAM=1;
    //auto-sampling after conversion complete
    ADCON1bits.ASAM=1;
    //Output format unsigned integer
    ADCON1bits.FORM=0b00;
    //trigger source = software by clearing SAMP bit
    ADCON1bits.SSRC=0b000;

    ADCON1bits.DONE=0;

    //conversion clock selection:
    //16MHz->fcyc=4MHz->Tcyc=250ns
    //minimum required Tcyc=167ns,so TAD=Tcyc should work
    //TAD=1*fcyc->ADCS<5:0>=000001
    ADCON3bits.ADCS=0b000001;
    ADCON3bits.ADRC=0;                          //use system clock and not RC clock

    //convert channel 0,1,2,3
    ADCON2bits.CHPS=0b10;
    //interrupt every sample/conversion cycle
    ADCON2bits.SMPI=0;

    //interrupt settings
    IFS0bits.ADIF=0;                            //clear interrupt flag
    IEC0bits.ADIE=1;                            //enable interrupt

    //enable ADC
    ADCON1bits.ADON=1;
}
```

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