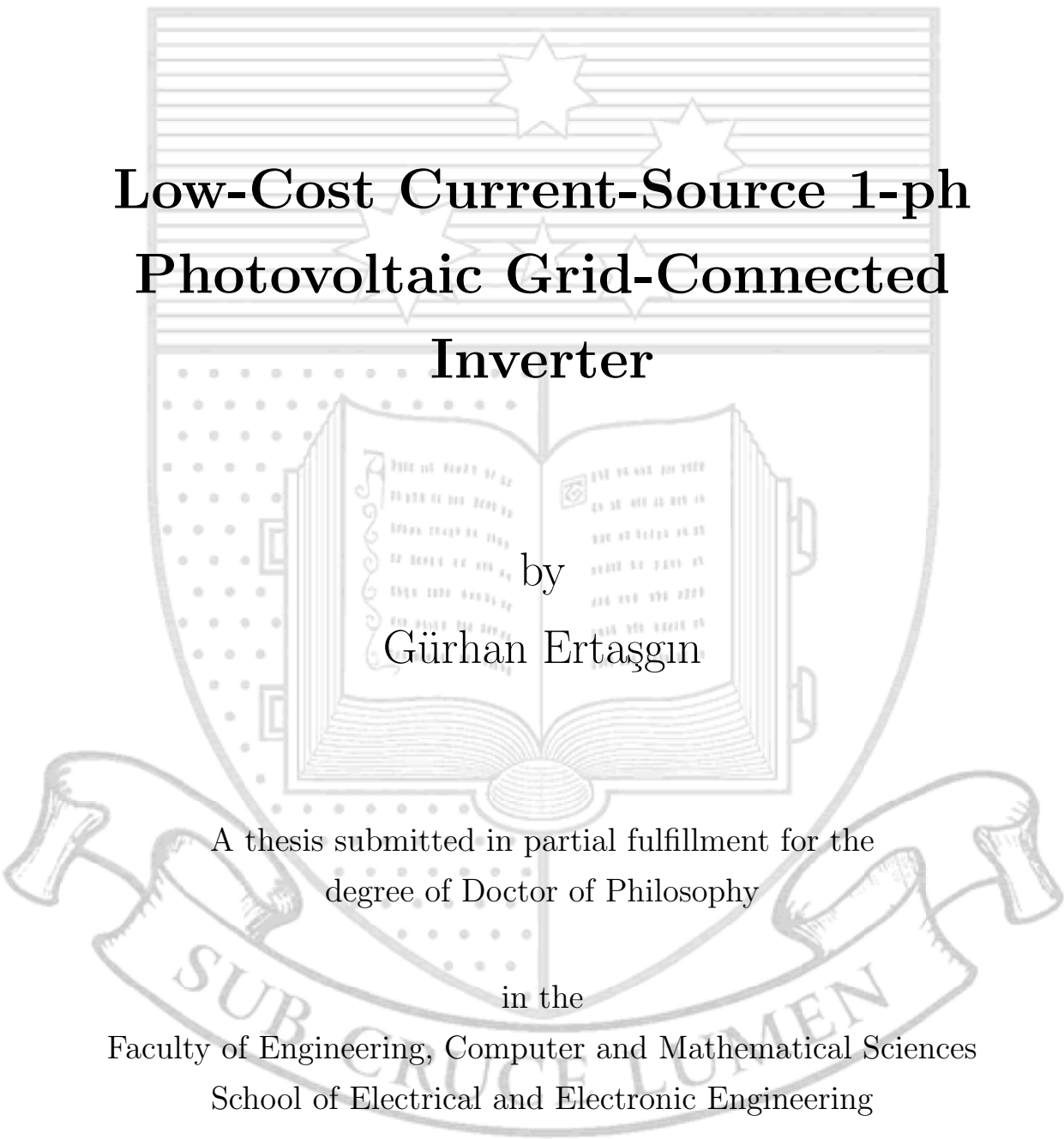


THE UNIVERSITY OF ADELAIDE



**Low-Cost Current-Source 1-ph  
Photovoltaic Grid-Connected  
Inverter**

by  
Gürhan Ertasgin

A thesis submitted in partial fulfillment for the  
degree of Doctor of Philosophy

in the

Faculty of Engineering, Computer and Mathematical Sciences  
School of Electrical and Electronic Engineering

August 2010

---

---

# CHAPTER 5

---

## LOW-PASS FILTER DESIGN

This chapter addresses one of the critical sections of the current-source inverter, the output filter. Firstly, the background of low-pass output line filters for VSIs and CSIs are provided. Important factors such as filter resonance and damping are explained. Then four different damped CL filter circuits are discussed and the performance of the filter with the proposed CSI inverter is analysed. The filter normalisations for the design process are also provided. The output current THD for the simplified CSI model given in the previous chapter is compared with a model which includes PWM switching and the output filter. Finally the selection of the filter parameters are examined.

### 5.1 Low-Pass Filter Design

The output low-pass filter reduces the high frequency harmonic content of the line current caused by the PWM switching. Generally the line filter consists of only a filter inductor (L filter) for VSIs but other configurations of inductors and capacitors such as CL filters for CSIs and LC and LCL filters for VSIs can be used (see Fig. 5.1).

Although the L filters are very common for VSIs, they attenuate high frequencies at only 20 dB/decade. Therefore their use is restricted to high-frequency low-power converter applications. The LCL filter addresses these problems. The higher harmonic attenuation of this type of filter permits the use of a lower switching frequency to meet the harmonic limits, increasing efficiency and lowering overall costs [38]. A capacitive-inductive (CL) filter, by contrast, is used with current source inverters (CSI), and attenuates high frequencies at 40 dB/decade [22].

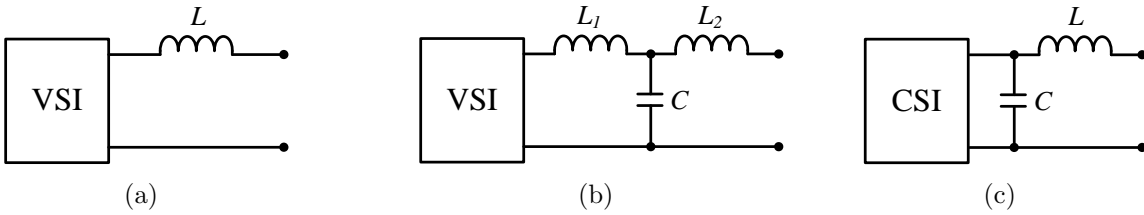


FIGURE 5.1: *Common grid-connected inverter low-pass filter types. The L (a) and LCL (b) filters are employed to couple VSIs, while the CL (c) filter couples a CSI to the grid.*

### 5.1.1 Design Criteria

It is well known that a GCI is required to provide high quality (low THD) power to the grid, whilst meeting the necessary power factor. The low-pass filter determines the harmonic attenuation and also affects the inverter power factor. However the importance of the low-pass filter design is often overlooked. Such filter has copper and iron losses and hence reduces the overall inverter efficiency. The low-pass filter is designed such that the inverter is able to meet the following grid requirements [9] while exhibiting a low damping resistance power loss (relative to rated power) :

- a power factor between 0.8 lead and 0.95 lag, from 20% to rated output power and
- attenuate the high-frequency harmonics such that the output current contains less than 5% THD.

### 5.1.2 Filter Resonance and Damping

For this application, a second-order CL type low-pass filter is required as it allows the coupling of the current source inverter to the voltage source grid, according to the impedance mismatch criteria [39]. An example of this type of filter is shown in Fig. 5.2 where  $R_D$  is the damping resistor.

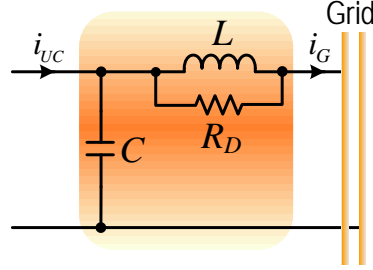


FIGURE 5.2: Parallel-damped CL type low-pass filter.  $R_D$  represents the damping resistor. The capacitor ESR and the inductor copper resistance are neglected.

The filter cutoff frequency  $f_c$  is commonly referred to as the resonant frequency,  $f_R$ , as the filter has an infinite gain at that frequency if there is no damping resistance. In order to avoid any large amplification at the resonant frequency, the output filter must be properly damped. There is some natural damping due to series losses in the inductor and the capacitor. However, it is frequently the case that additional damping is necessary. The resonant frequency can be given by

$$f_R = \frac{1}{2\pi\sqrt{LC}} \quad (5.1)$$

The inverse of damping is quality factor  $Q$  which is related to the gain of the filter at the resonant frequency. Note that the filter gain represents the ratio of output to input current, i.e.  $I_G / I_{UC}$  in Fig. 5.2. The expression for  $Q$  is dependent on the filter topology and the type of damping used. An analysis of various practical filter topologies and damping techniques is continued in Section 5.1.4. The  $Q$  of the filter in Fig. 5.2 may be expressed as

$$Q = \sqrt{\left(\frac{R_D}{Z_0}\right)^2 + 1} \quad (5.2)$$

where,  $Z_0 = \sqrt{L/C}$  is the characteristic impedance of the filter. If the  $Q$  of the filter is too high an increase in THD can occur at the resonant frequency of the filter. If it is

too low it will produce a large filter loss. The recommended values of  $Q$  for grid filters varies for 2-4 [39]. Therefore a value of  $Q$  of 4 is chosen initially for the filter analysis in Section 5.2.

The CL filter is able to substantially attenuate the high-frequency PWM harmonics if the resonant frequency is selected to be small compared to the PWM switching frequency,  $f_{sw}$  (say an order of magnitude lower). If the resonant frequency is low, the low-pass filter requires large filter inductance, which results in higher loss. On the contrary, if the switching frequency is too high, switching losses are increased. In this application a value of  $f_{sw}$  of 4 kHz was chosen. This value corresponds to that used experimentally in Chapter 6. As a result the  $f_c$  is chosen to be 500 Hz to have a reasonable ratio  $f_c/f_{sw} = 0.125$ . The trade-off between quality factor and the ratio of  $f_c/f_{sw}$  is shown in Fig. 5.3.

### 5.1.3 Filter Normalisations

As it is well known, the use of normalisation generalises the analysis. Thus the filter cut-off (or resonant) frequency and filter components are normalised in this study. The normalised cut-off frequency,  $\omega_{cn}$  is expressed in relation to the base frequency,  $\omega_B$ , which is given below in (5.3).

$$\left. \omega_{cn} \equiv \frac{\omega}{\omega_B} \right\} \quad \text{where} \quad \omega_B = 2\pi f_1 \quad (5.3)$$

where  $f_1$  represents the grid (inverter fundamental) frequency. Considering a single-phase inverter designed to deliver rated power,  $P_B$  into a grid of rated voltage  $V_B$ , the resulting base impedance,  $Z_B$  can be given by (5.4), and is later used to normalise the filter components. Note that the base impedance is defined as the ratio of the base voltage,  $V_B$  and the base current  $I_B$ .

$$Z_B \equiv \frac{V_B}{I_B} = \frac{V_B^2}{P_B} \quad (5.4)$$

The normalised filter capacitance,  $C_n$  is given in (5.5), where  $C_B$  is the base capacitance. Similarly, the normalised filter inductance,  $L_n$  is expressed relative to the base

inductance,  $L_B$  [22].

$$\left. \begin{aligned} C_n &= \frac{1}{\omega_{cn}^2 L_n} = \frac{C}{C_B} \\ L_n &= \frac{1}{\omega_{cn}^2 C_n} = \frac{L}{L_B} \end{aligned} \right\} \text{ where } \begin{aligned} C_B &= \frac{1}{\omega_B Z_B} \\ L_B &= \frac{Z_B}{\omega_B} \end{aligned} \quad (5.5)$$

As stated earlier, the power factor requirements are 0.8 leading to 0.95 lagging for all outputs from 20% to 100% of rated output power. The maximum value of  $C_n$  can be determined based on the 0.8 leading requirement at 20% of output power, to be 0.124 pu [22]. Thus a  $C_n$  value of 0.1 pu is used initially for the filter in Fig. 5.2 so as to analyse with the proposed CSI in Section 5.2.

#### 5.1.4 Filter Configurations

Table 5.1 shows four different CL filter configurations which differ in the location of the damping resistor. The table also provides the transfer functions  $H(s)$ , quality factor  $Q$  and the high-frequency attenuation or roll-off rate for each filter configuration (FC).

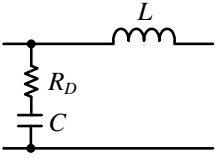
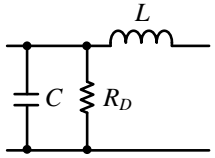
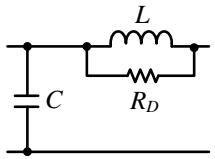
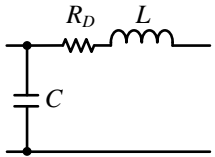
The first FC uses a resistor in series with the capacitor of the CL filter. This causes the filter to have a first-order high frequency roll-off. The high frequency impedance of the filter is also increased. The damping resistor in this arrangement mainly sees the high-frequency current components and has a moderate power dissipation ( $P_d$ ).

A resistor in parallel with the capacitor in FC 2 acts essentially as a resistive load which damps the filter. As it can be seen in the circuit this resistor has the full fundamental output voltage across it and hence the high power dissipation will make it impractical.

The FC 3 in Table 5.1 has a resistor in parallel with the filter inductor which gives it a first-order high frequency roll-off. The power dissipation in  $R_D$  would be expected to be much smaller compared to the other types as the fundamental voltage drop across the inductor is small.

The FC 4 however has a resistor in series with the filter inductor. This configuration has two problems : a resistive output impedance at low frequencies and high losses. At low frequencies, the impedance of the filter is equal to the damping resistor [39]. The series

TABLE 5.1: Resistive ( $R_D$ ) damping of second-order CL filter configurations [22, 39].

FC	Circuit	Transfer Function $H(s)$	Quality Factor Q	Roll-off rate beyond $f_R$
1		$\frac{sCR_D + 1}{s^2CL + sCR_D + 1}$	$\sqrt{\left(\frac{Z_0}{R_D}\right)^2 + 1}$	-20 dB/decade
2		$\frac{R_D}{s^2CLR_D + sL + R_D}$	$\frac{R_D}{Z_0}$	-40 dB/decade
3		$\frac{sL + R_D}{s^2CLR_D + sL + R_D}$	$\sqrt{\left(\frac{R_D}{Z_0}\right)^2 + 1}$	-20 dB/decade
4		$\frac{1}{s^2CL + sCR_D + 1}$	$\frac{Z_0}{R_D}$	-40 dB/decade

resistor in FC 4 sees the full grid current and thus has high losses, but has a second-order roll-off at high frequencies which is a positive feature.

The performance of the four CL filter configurations were carefully analysed by Whaley [22] under the conditions of a switching frequency of 4 kHz and a filter capacitance of 0.12 pu (to meet the power-factor standards). The quality factor as a function of normalised cut-off frequency for each filter configuration (FC) is also given in Fig. 5.3.

As given previously the normalised cut-off frequency in the figure is the ratio of the cut-off frequency to the switching frequency. In each graph the solid lines represent contours of THD and power loss, which is equal to 5%. As highlighted, the solid lines separate the design space into four regions which correspond to areas where : (A) the THD is less than 5%, (B) the THD and damping resistance power loss are both less than 5% (this is labelled as the design space), (C) the power loss is less than 5%, and (D) both the THD and power loss are greater than 5%. The 5% threshold for power loss was chosen arbitrarily as an upper limit, clearly a lower value would be desirable.

NOTE:  
These images are included on page  
67 of the print copy of the thesis held  
in the University of Adelaide Library.

FIGURE 5.3: *Power loss and THD contours of 5%, for filter configurations (a) 1, (b) 2, (c) 3 and (d) 4, for a switching frequency of 4 kHz [22].*

The design region (B) in the figures allows the filter inductance to be easily selected based on the desired cut-off frequency and the filter configuration. Similarly, the damping resistor can also be determined knowing the quality factor. Note that the inverter performance can be improved, i.e. the output current THD and damping resistor power loss can be reduced by increasing the filter quality factor.

Fig. 5.3 shows that FC 1 and 3 are the only configurations that meet recommendation of a  $Q$  between 2 and 4 [39]. In addition, FC 3 is able to meet this over a wider range of cutoff frequencies, and at lower values of  $Q$  than FC 1. In contrast, both FC 2 and 4 can not meet the suggested  $Q$  range; the minimum  $Q$  which allows FC 4 to lie within the design region, is 6.5, whilst that of FC 2 is about 20 (for a  $f_c$  of 0.1 pu). Based on these results, FC 3 was chosen as a low-pass filter in this research.



## 5.2 Analysis of Low-Pass Filter with Proposed CSI

Previously, it was assumed that the filter is supplied with a unipolar PWM current that is created using an ideal constant current source. However, the proposed GCI uses a PV array and DC link inductor. Therefore, the effects of this non-ideal current source are examined here using the filter configuration 3 (see Table 5.1).

A baseline filter design is determined as follows. The normalised capacitance  $C_n$  is selected as 0.1 pu to meet the leading power factor requirements. The cut-off frequency  $f_c$  is chosen as 500 Hz which is an order of magnitude above the fundamental frequency to prevent significant filter phase delay and roughly an order of magnitude below the switching frequency (4 kHz). Based on the recommendation regarding a quality factor of  $Q$  of 2-4, a value of 4 was selected. Note that the effects of changing the filter parameters will be discussed later in Section 5.3.

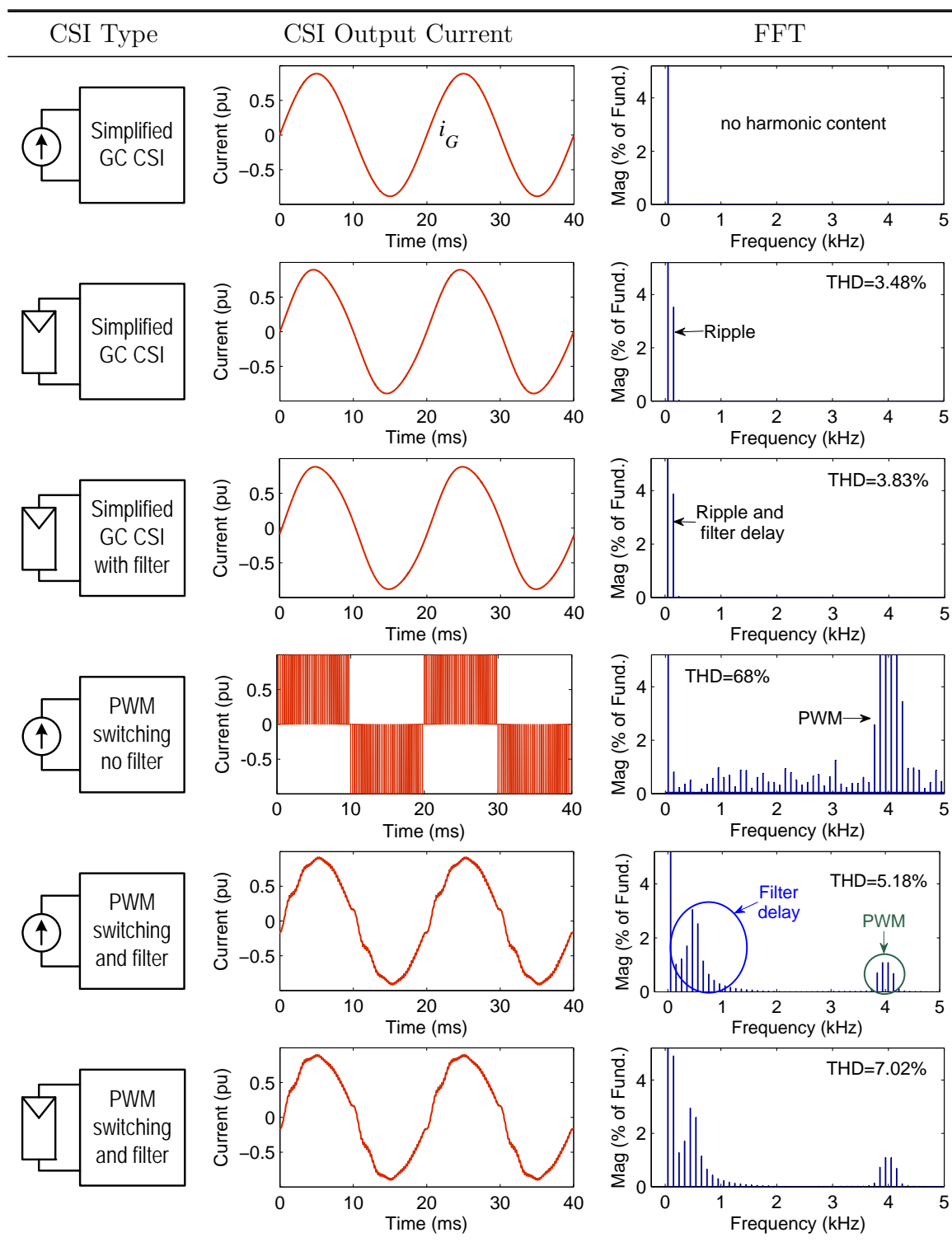
Table 5.2 is given to show the normalised output currents of the grid-connected CSI and their FFT spectrums for different circuit configurations. Firstly, the ideal case of a GC CSI based on the simplified model with no PWM switching (see Chapter 4) was examined using a constant current-source. The CSI output current has no harmonics and therefore there is no need for the CL low-pass filter for this CSI configuration.

The second CSI type is also based on the simplified model, but using a 4-diode model for the PV array. The difference with the first type is the output current harmonic content which is caused by the power fluctuations at twice the grid frequency resulting in PV output current ripple. The low frequency harmonics in this type of CSI, such as the 3<sup>rd</sup> harmonic can be effectively removed by incorporating a feedforward controller.

The third CSI type is identical with the second one except it includes the CL low-pass filter. There is little effect in terms of THD due to phase delay. Therefore the THD increases due to a slight increment in the 3<sup>rd</sup> harmonic.

The fourth CSI type uses a PWM switching model of the inverter (rather than the simplified model used in the previous types) with an ideal current source input. The output current thus contains strong frequency component associated with PWM harmonic sidebands and the THD is very large.

TABLE 5.2: The normalised output currents of the CSI and their FFT spectrums for simplified and including the WS and the CL low pass filter. Obtained results are under nominal conditions at the maximum power point.



The fifth CSI type is based on the fourth case but includes the low-pass filter. As expected this reduces the PWM switching components down to relatively small levels. However it was found that the output current has significant components around the resonant frequency of the low-pass output filter, which is due to the phase delay of the filter. In combination with the PWM harmonics this results in a THD slightly greater than the 5% requirement.

The sixth and final CSI type employs a 4-diode model instead of the constant current-source. As expected this results in a larger 3<sup>rd</sup> harmonic output current component which increases the THD to about 7%.

The next section investigates the use of phase advance technique to reduce the output current THD to acceptable levels.

### 5.2.1 Phase Advance

The previous section showed that the phase delay produced by the low-pass grid filter means that the unfolding circuit output voltage  $V_{UC}$  has a phase advance compared to the grid voltage  $V_G$ . This phase delay combined with the PWM switching causes commutation problems at the zero crossings as seen in Fig. 5.4(a) in the unfolding circuit output current  $i_{UC}$ . Hence these glitches excite the resonant frequency of the low-pass filter and produce a range of harmonics in the inverter output current  $i_G$  (see Table 5.2, type 5). To overcome this problem, phase advance of the waveshaper and unfolding circuit control signals with respect to the grid voltage needs to be introduced. From the equivalent circuit in Fig. 5.4(b), the phasor diagram can be drawn, taking into account that assuming the grid current is required to in phase with respect to the grid-voltage phasor.

The calculation of the phase angle can be done based on the phasor diagram. Then the rated CSI output current  $I_G$  can be calculated with rated output power  $P_{OUT}$  and the peak grid voltage  $V_{PK}$  as

$$I_G = \frac{P_{OUT}}{V_{PK}} \sqrt{2} \quad (5.6)$$

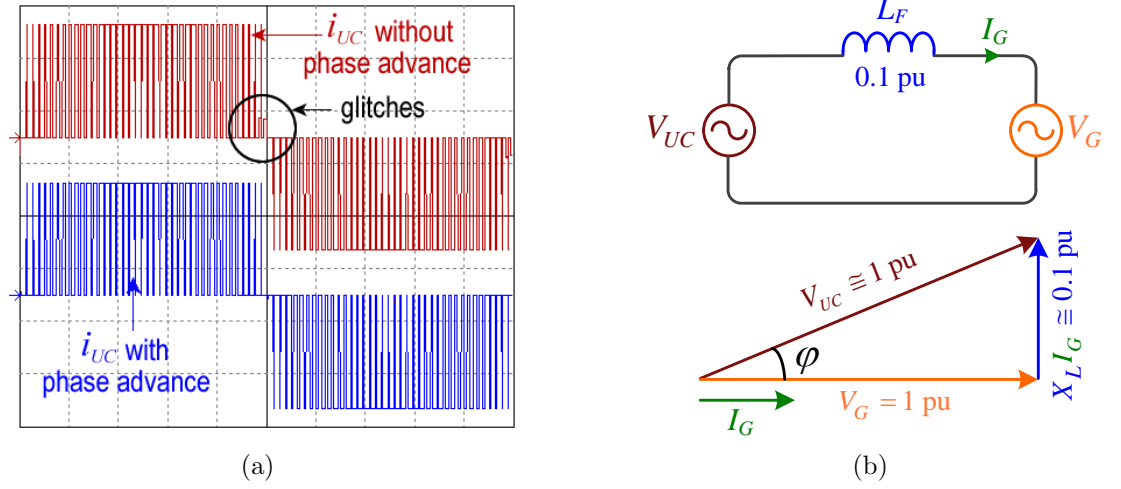


FIGURE 5.4: (a) The unfolding circuit output current without and with phase advance showing the glitch in circle (scales are 2 A/div and 2 ms/div) and (b) phasor diagram at the AC side of the circuit.

The applied voltage to the inductor  $V_{L,F}$  can be found by

$$V_{L,F} = I_G L_F \omega \quad (5.7)$$

where  $L_F$  is the inductance and  $\omega$  is the angular frequency. From the diagram in Fig. 5.4(b) the hypotenuse is the output voltage  $V_{UC}$ , which can be given by

$$V_{UC} = \sqrt{V_{L,F}^2 + V_{PK}^2} \quad (5.8)$$

Thus the phase angle  $\varphi$  can be found with the well-known trigonometric term using the vector diagram in Fig. 5.4(b).

$$\varphi = \cos^{-1} \frac{V_{PK}}{V_{UC}} \quad (5.9)$$

As seen in (5.8) and (5.9) the calculated phase advance is directly proportional to the filter inductance. The phase advance can be added to the reference signal of the control circuit to compensate the phase difference between  $V_{UC}$  before the filter and  $V_G$  after the filter. However  $\alpha$  is slightly different compare to analytical phase advance  $\varphi$ . In other words,  $\alpha$  is used in the control signal (as simulation) to create analytically calculated  $\varphi$  between  $V_{UC}$  and  $V_G$ . Fig. 5.5(a) shows  $\varphi$  and  $\alpha$  in degrees for different power outputs under 0.5 and 1 kW/m<sup>2</sup> irradiances. The difference between  $\varphi$  and  $\alpha$  can be seen in this figure clearly.

Fig. 5.5(b) shows the output current THD as a function of phase advance angle,  $\alpha$  for under 0.5 and 1 kW/m<sup>2</sup> irradiances. At rated irradiance, the output THD reduces substantially due to higher current hence DC link energy storage capacity (see Chapter 3). Both PSIM and PLECS simulation tools give identical results that the output current THD is below the grid THD requirement at around  $\alpha = 7^\circ$  for the rated output power.

Fig. 5.5(c) shows the THD curve for different output powers using constant  $\alpha$ , which is determined for the rated output power only. In this case  $\alpha$  is not changed for irradiances from 1 to 0.1 kW/m<sup>2</sup>. As seen from the curve the output current THD is below the grid

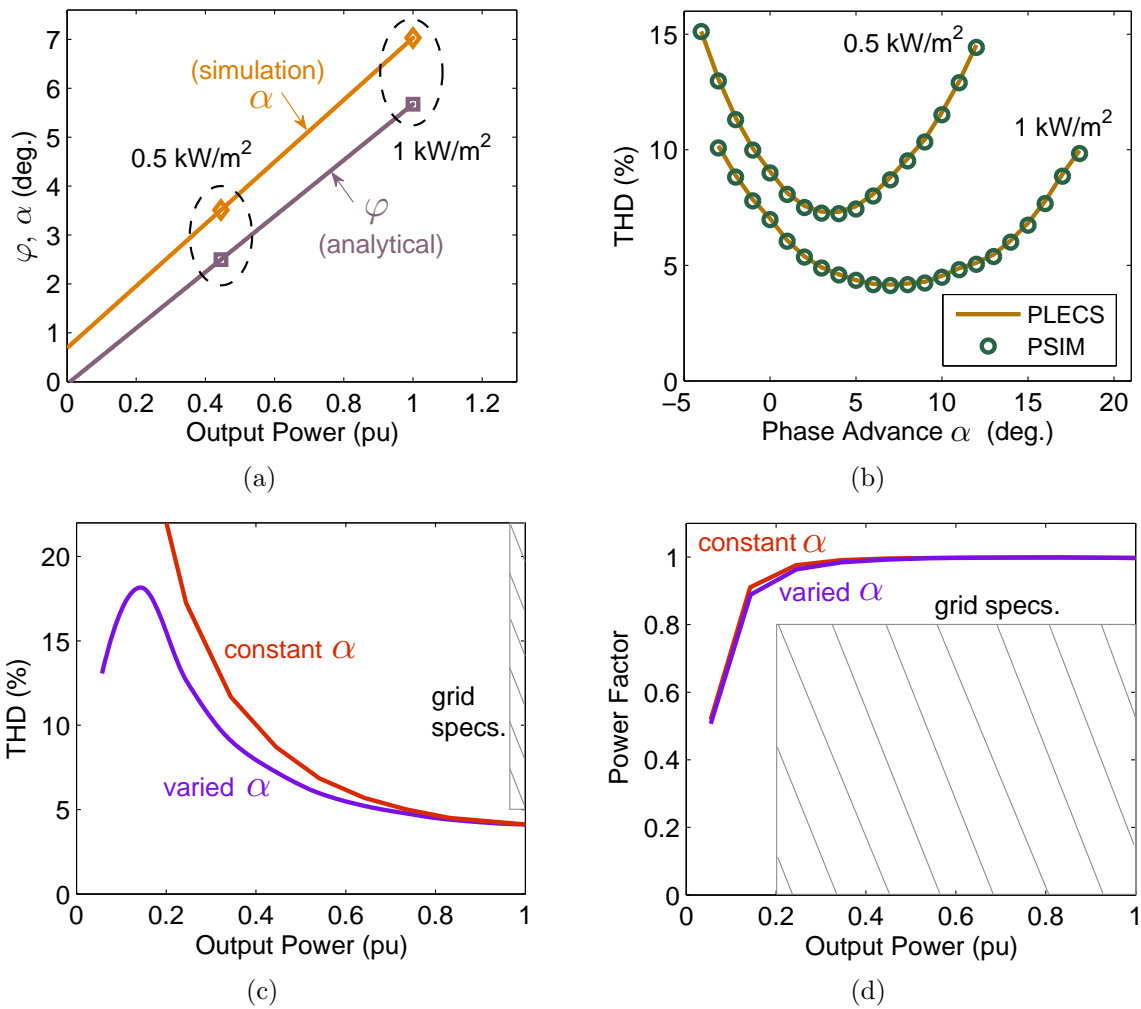


FIGURE 5.5: (a) Analytical phase advance  $\varphi$  and its corresponding phase difference  $\alpha$  in the reference signal as a function of output power, (b)  $\varphi$  and  $\alpha$  versus THD as a function of output power obtained by varying the irradiance, (c) THD and (d) power factor for fixed  $\alpha$  at the rated output power and variable  $\alpha$  for each irradiance at the MPP.

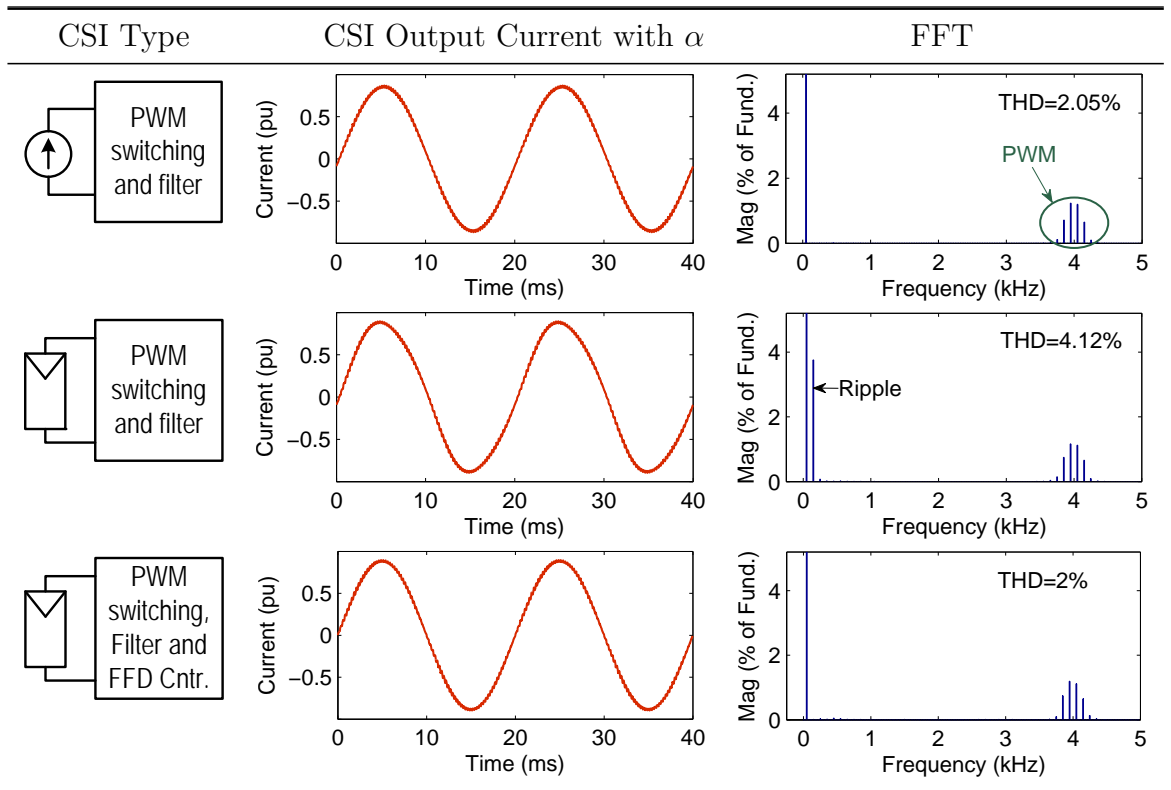
THD requirement at the rated output power. After  $0.7 \text{ kW/m}^2$  irradiance value the THD increases sharply due to less PV array output current as expected (see Fig. 4.10(a)).

The other THD curve for several irradiances is generated adjusting  $\alpha$ . The adjusted  $\alpha$  gives the optimum THD value due to analytical  $\varphi$  at that power level (see Fig. 5.5(b)). There is an insignificant difference between two THD curves in Fig. 5.5(c) especially after  $0.7 \text{ kW/m}^2$  irradiance. As a result determining  $\alpha$  for only rated output power does not affect the THD in terms of Australian Standards.

Similarly power factors for constant and variable  $\alpha$  values do not illustrate considerable difference in Fig. 5.5(d). Hence both PF curves meet the Australian Standards.

Table 5.3 illustrates CSI output current waveforms and their FFT spectrums. The first CSI type is identical with the fifth type in Table 5.2 except  $\alpha$  adjustment. Therefore in this case there are no glitches at the zero crossings which result in significant THD components around the resonant frequency of the low-pass output filter.

TABLE 5.3: The normalised output currents of the CSI and their FFT spectrums. The CCS and 4-diode model are used as the CSI input and the reference signal with phase advance  $\sin(\omega t + \alpha)$ . Obtained results are under nominal conditions at the MPP.



The second CSI type corresponds to final case in Table 5.2. Again in this case  $\alpha$  is included in the reference signal of the control circuit. As it can be seen, the THD is slightly higher than the first case due to 100 Hz fluctuations. However the output current THD is still below the grid THD requirements and much lesser than the final CSI type in Table Table 5.2.

The third and final CSI type is same as the second type. This type differs as feedforward controlled CSI. The FFD control eliminates the 100 Hz ripple effect. Therefore the output current waveform is exactly same as the first type in Table 5.3. The THD value is 2% due to PWM switching similar to first case. If the PWM switching is ignored as in Chapter 4, there should not be any THD content (see Fig. 4.10(c)).

## 5.3 Design Trade-Offs

The previous analysis has been done based on a baseline low pass filter design with  $C_n = 1$  pu,  $f_c = 500$  Hz,  $Q = 4$ . It was shown that with phase advance control this filter could meet the Australian Standards. In this section the effect of varying these parameters on the output current THD, power factor and the damping resistor power loss is investigated.

### 5.3.1 Effect of $C_n$ Variation

Fig. 5.6(a) shows the CSI output current THD versus output power for several  $C_n$  values as a function of irradiance. Although the THD values at the rated power are similar, the 0.05 pu  $C_n$  case has the lowest THD. The grid THD requirements are met for  $C_n$  values of 0.05 to 0.15 pu at the rated output power. For medium to low irradiances the THD is inversely proportional to the  $C_n$  especially for smaller  $C_n$  values.

For small  $C_n$  values the value of  $L_n$  is also increased to maintain constant cut-off frequency which result in higher  $Z_0$ .  $P_d$  is directly proportional to  $Z_0$  hence higher  $Z_0$  will increase  $P_d$  significantly as seen in Fig. 5.6(c).

On the contrary, increasing  $C_n$  such as  $C_n > 0.12$  pu may not keep the power factor over 0.8 at 20% of the rated power as seen in Fig. 5.6(b). The PF curve for using 0.15 pu  $C_n$  is very close to PF of 0.8 at 20% of the rated output power.

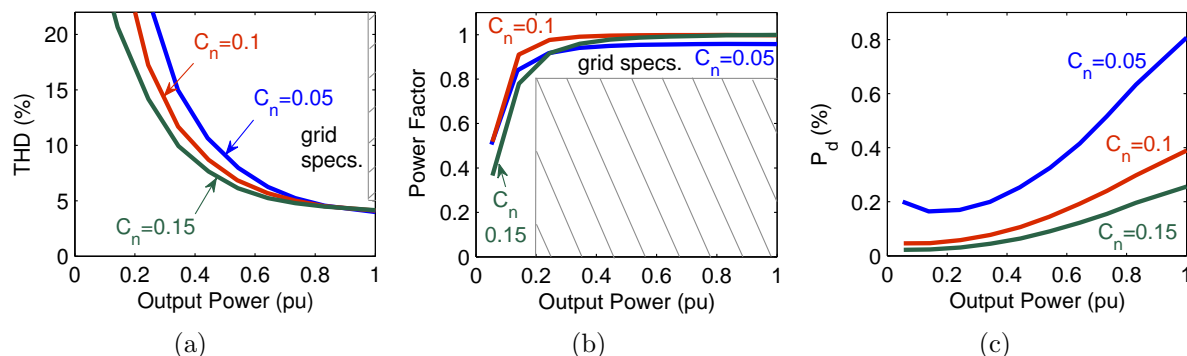


FIGURE 5.6: The CSI output power versus (a) output current THD, (b) power factor and (c) damping resistance power loss ( $P_d$ ) by changing normalised capacitance for various irradiances.  $Q = 4$  and  $f_c = 500$  Hz.

### 5.3.2 Effect of $f_c$ Variation

Fig. 5.7(a) shows the output current THD for varying irradiances with  $f_c$  equal to 5, 10 and 20 times the fundamental. As it is illustrated, a 250 Hz  $f_c$  results in a larger  $L_n$ , hence the  $Z_0$  is increased similar to the 0.05 pu  $C_n$  case in Fig. 5.6(a). Fig. 5.7(a) implies that the low-pass filter becomes less effective as  $f_c$  approaches the switching frequency  $f_{sw}$ , as higher magnitude high-frequency components can pass through the filter, which ultimately increases the output current THD at the rated output power. However the harmonic content is less for higher  $f_c$  values due to the lower phase delay of the filter. The phase delay is inversely proportional to the filter cut-off frequency.

Fig. 5.7(b) suggests that using the small values of  $f_c$  may not meet the grid requirements due to high phase delay despite the added phase advance  $\varphi$ .

The  $P_d$  for the 250 Hz  $f_c$  value is relatively high at about 3% compared to the higher cut-off frequencies in Fig. 5.7(c). This is due to the higher  $Z_0$  which is similar to the  $C_n = 0.05$  pu case in Fig. 5.6(c) although in this case the  $P_d$  is doubled.



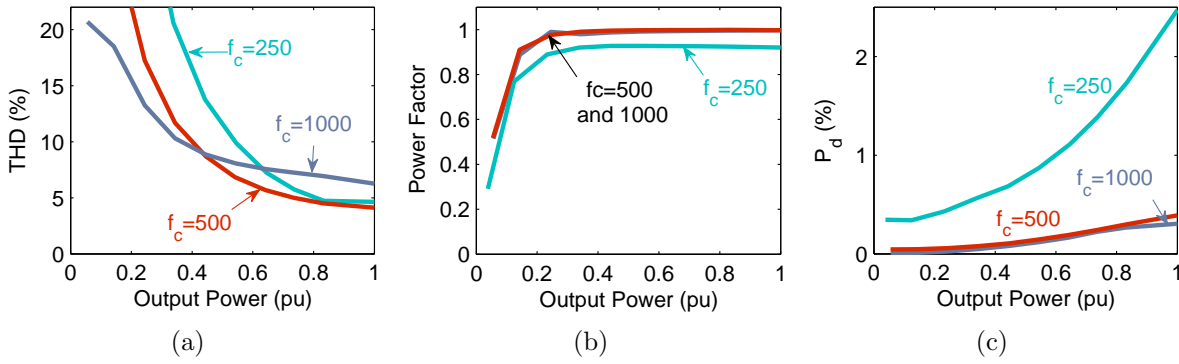


FIGURE 5.7: The CSI output power versus (a) output current THD, (b) PF and (c)  $P_d$  by changing cut-off frequency as a function of irradiance.  $Q = 4$  and  $C_n = 0.1$  pu.

### 5.3.3 Effect of $Q$ Variation

The variation of the  $Q$  of the designed filter can be seen in Fig. 5.8 as a function of irradiance. THD curves in Fig. 5.8(a) are very similar for  $Q$  values of 4 and 8. The least THD value is obtained at the  $Q$  of 8 although the amplification at the  $f_c$  is higher compared to  $Q = 2$  and 4 as it has better attenuation for higher frequencies. The  $Q$  of 2 case is just above the grid THD requirements.

The PF factor is identical for all different  $Q$  values as  $Q$  variations do not affect  $C_n$  and  $L_n$  values. The  $P_d$  is the least for the  $Q$  value of 8 in Fig. 5.8(c). There is a trade-off between THD and  $P_d$  values. The reason that  $P_d$  is lower with the higher damping resistance is the reduced current flow through into  $R_D$  due to the fixed  $L_n$  value. As a result value of  $Q$  is directly proportional to  $R_D$ .

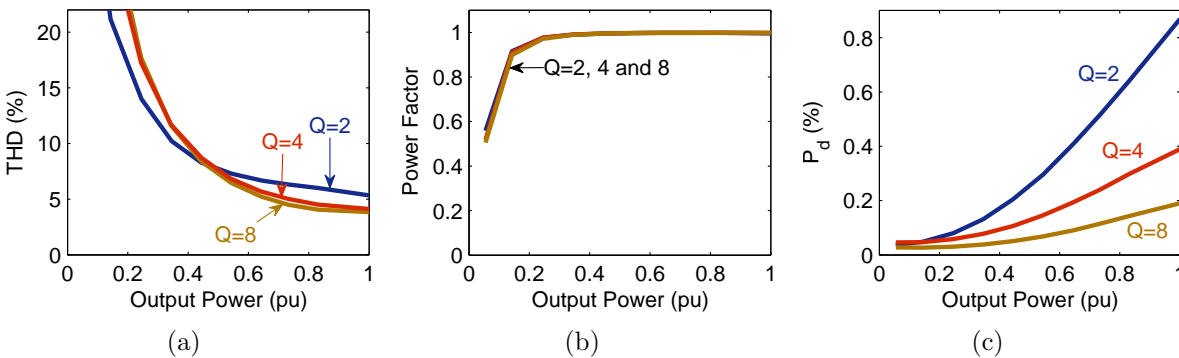


FIGURE 5.8: The CSI output power versus (a) output current THD, (b) PF and (c)  $P_d$  by changing quality factor for various irradiances.  $C_n = 0.1$  pu and  $f_c = 500$  Hz.

### 5.3.4 Summary of Effects of Variations

Fig. 5.9 summarises the damping resistor loss as a function of THD for the  $C_n$ ,  $f_c$  and  $Q$  variations at the rated output power ( $P_0$ ). The maximum THD is seen for the  $f_c = 1$  kHz case. On the contrary the maximum power loss is seen for the  $f_c = 250$  Hz case. The  $Q = 8$  case is the best filter configuration in terms of the lowest THD and  $P_d$ . The baseline filter appears to be relatively optimum as well while offering a lower  $Q$ . The  $C_n = 0.15$  pu case and baseline filter have similar performance at the rated output power.

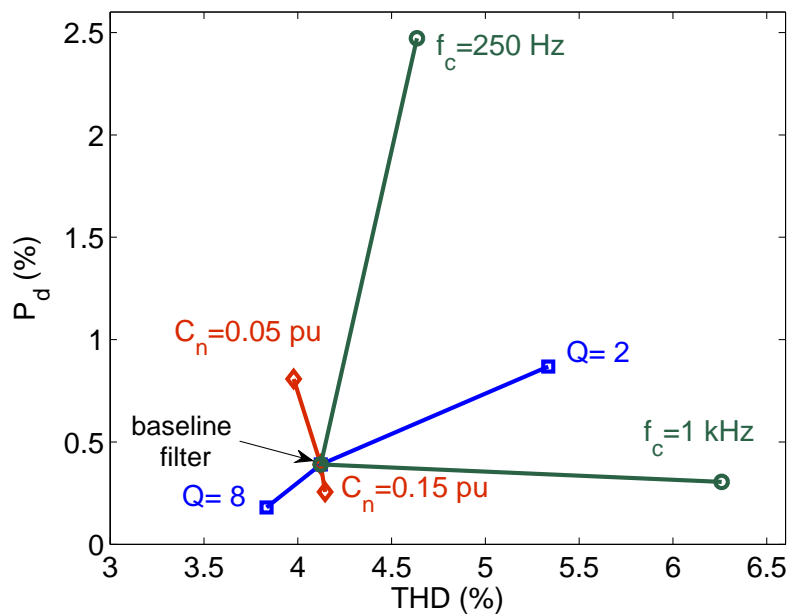


FIGURE 5.9: Damping resistance power loss for several THD values in respect to  $C_n$ ,  $f_c$  and  $Q$  changes for only rated output power.

## 5.4 Summary

The required low-pass output filter to remove high-frequency PWM harmonics for a current-source grid-connected inverter is addressed. The CL type filter is analysed, and it is shown that damping is required to limit the effect of resonance. Four damping resistor locations, and their respective power loss vs. harmonic attenuation (output current THD) trade-offs are discussed. The configuration with the damping resistor connected in parallel to the filter inductor offers the least power loss, whilst sufficiently attenuating the high-frequency PWM harmonics.

Baseline values for the three filter parameters ( $C_n = 0.1$  pu,  $f_c = 500$  Hz,  $Q = 4$ ) were selected. The non-linear PV array input current effect to the CSI output current using the baseline filter is investigated. The analysis shows that the low-pass filter introduces a phase delay which can cause undesirable harmonic content. Therefore adding phase advance to the control signals is investigated to compensate. For this delay it is shown that with phase advance the baseline filter can meet the grid THD and PF requirements. A limited optimisation of the filter parameters was performed. The analysis suggests that a low  $f_c$  ( $\leq 250$  Hz) may not meet the grid requirements for THD and PF. A low  $Q$  ( $< 2$ ) may not meet the grid THD requirements. In addition to these, a high  $C_n$  ( $> 0.15$  pu) could not meet the grid PF requirements. Hence the designed baseline low-pass filter meets the grid THD and PF requirements and its power losses are close to the optimum value.

---

---

## CHAPTER 6

---

# 160 W INVERTER SIMULATION AND TEST RESULTS

This chapter investigates the design and performance of a 160 W single-phase current-source grid-connected inverter topology that is based on a PV array and DC link inductor acting as a constant-current source. The inverter is implemented using a single boost switch, a H-bridge inverter and a CL output filter. As it was shown in the previous chapter, the inverter output current is easily controlled using the boost switch and simple open-loop control. The inverter input is simulated using the dark I-V configuration of two series PV modules. The comprehensive test results are obtained to verify the computer simulation results. Furthermore, the proposed inverter's ability to deliver a sinusoidal current to the grid whilst meeting the appropriate standards, i.e. total harmonic distortion and power factor requirements are also examined for various modulation index values and irradiances. Finally the feedforward compensation control tests are shown for validation.

## 6.1 Proposed Inverter Implementation

### 6.1.1 Inverter Simulation

The proposed inverter system was simulated using PSIM. The simulation model is shown in Fig. 6.1, which includes equivalent circuit parameters, the inverter and the 4-diode model that represents the PV modules. The semiconductor devices are also accurately modelled as well that is to say the thyristor and reverse blocking diode voltage drops are taken into account and the on resistance of the MOSFET is included. Since the test setup included an auto transformer, the inductance and resistance of the autotransformer are also considered in the simulation model before the voltage source (grid).

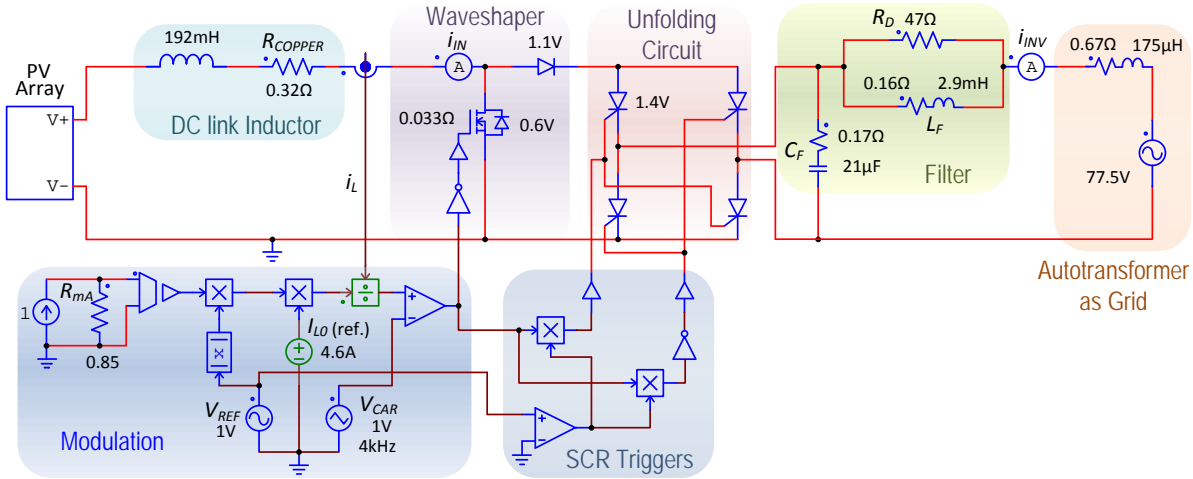


FIGURE 6.1: Inverter circuit simulation using PSIM, showing PV array (4-diode model), DC link inductor, waveshaper, unfolding circuit, output filter, grid model, modulation index controller and PWM signal generator.

### 6.1.2 Inverter Control

The PV inverters are required to extract maximum power from the PV arrays using maximum power point tracking (MPPT). The output power of the inverter can be controlled using open-loop or closed-loop control.

#### Maximum Power Point Tracking

Since the PV module current-voltage characteristics vary according to operating conditions, so too will the voltage corresponding to the maximum power point tracking

(MPPT). Hence to maximise the output power the inverter must be able to vary the PV array output voltage while maintaining a fixed AC output voltage, that is achieved by varying the modulation index. The proposed MPPT algorithm is based on maximising the inverter output current using the perturb-and-observe method [16], that is shown in Fig. 6.2.

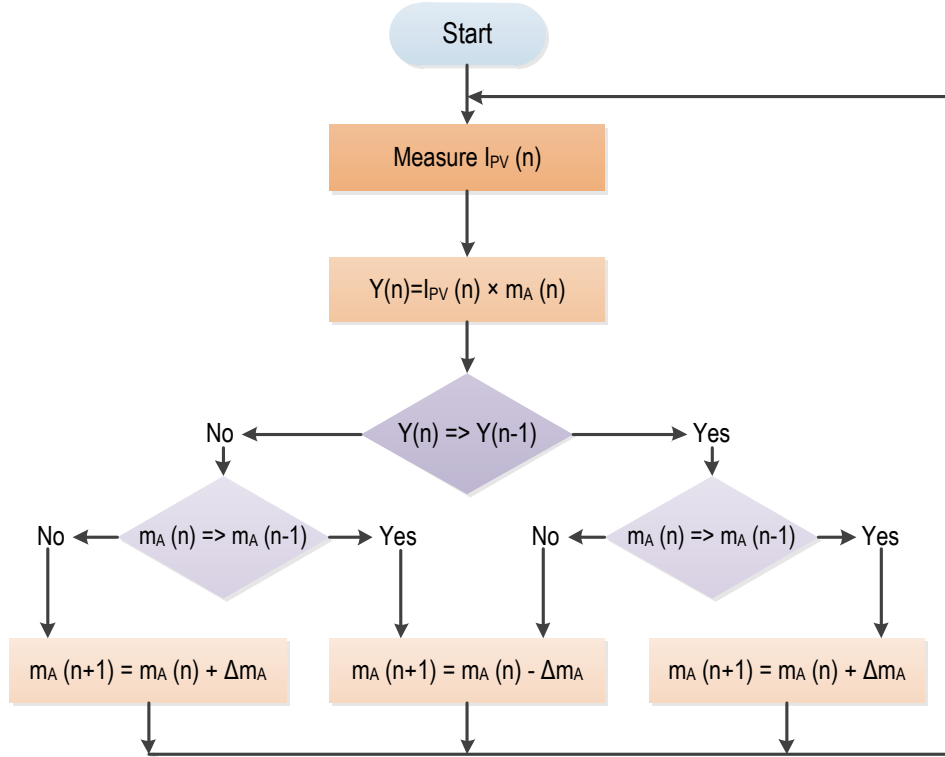


FIGURE 6.2: MPPT algorithm flow diagram using perturb-and-observe method.

In this application, the grid current is not measured directly but estimated as the product of modulation index and measured PV array output current as shown in (6.1).

$$I_{UC} = \frac{m_A I_L}{\sqrt{2}} \quad (6.1)$$

where  $I_{UC}$  is the fundamental component of the unfolding circuit (H-bridge) output (grid) current and  $I_L$  is the DC link inductor current.

### Open-Loop Control

The open-loop control approach requires perfect knowledge of the system i.e. one knows exactly what inputs are required to get the desired output, and it assumes there are no disturbances to the system.

Before testing the feedforward compensation control, an open-loop control algorithm was utilised for the two different prototypes (see Fig. 6.5).

In the implemented open-loop control algorithm, the microcontroller uses the zero-crossings of the grid voltage to generate the PWM signal and SCR trigger pulses. The PWM switching frequency is set to 4 kHz, as this is a reasonable trade-off between the inverter switching losses and output current waveform quality, both of which are proportional to switching frequency. The PWM signal is based on a duty-cycle look-up table with an index counter which is reset at negative grid voltage zero-crossings, which produces an unfolding circuit output current which is in-phase with the grid voltage.

The look-up-table stores 40 integer values which represent half cycle of a sinusoidal waveform based on a 16 MHz crystal oscillator frequency. The value corresponds to a modulation index  $m_A$  of unity. The inverter output current magnitude and hence power can be controlled by varying the modulation index, which effectively increases/reduces the waveshaper PWM duty cycle. This adjusted duty-cycle  $d$  is expressed by (6.2), where  $i_{OUT}$  represents the WS output or the unfolding circuit input current.

$$i_{OUT} = i_L [(1 - d) m_A] \quad (6.2)$$

The microcontroller is programmed using the C language, and makes use of both software and hardware interrupts (see Appendix B). A simplified overview of the microcontroller hardware and its behavioural flow diagram are shown in Fig. 6.3.

Fig. 6.4(a) shows the WS PWM pulses and one of the SCR pair's drive pulses. Fig. 6.4(b) shows both SCR pair pulses that unfold the WS current. These SCR pulses are the compliment of the PWM pulses. They commutate naturally due to the nature of the waveshaper output current i.e. the current sufficiently falls below the SCR holding current to turn them off. A positive output current is obtained when  $T_1$  and  $T_3$  conduct and a negative output current when the  $T_2 - T_4$  pair conducts (see Fig. 6.1).

Grid synchronisation is achieved using a simple mains voltage zero-crossing detector based on a comparator which generates a signal which is used to interrupt the microcontroller. The microcontroller uses this information to reset the SCR and WS look-up table duty-cycle, and hence outputting the current whose fundamental is synchronised to the grid.

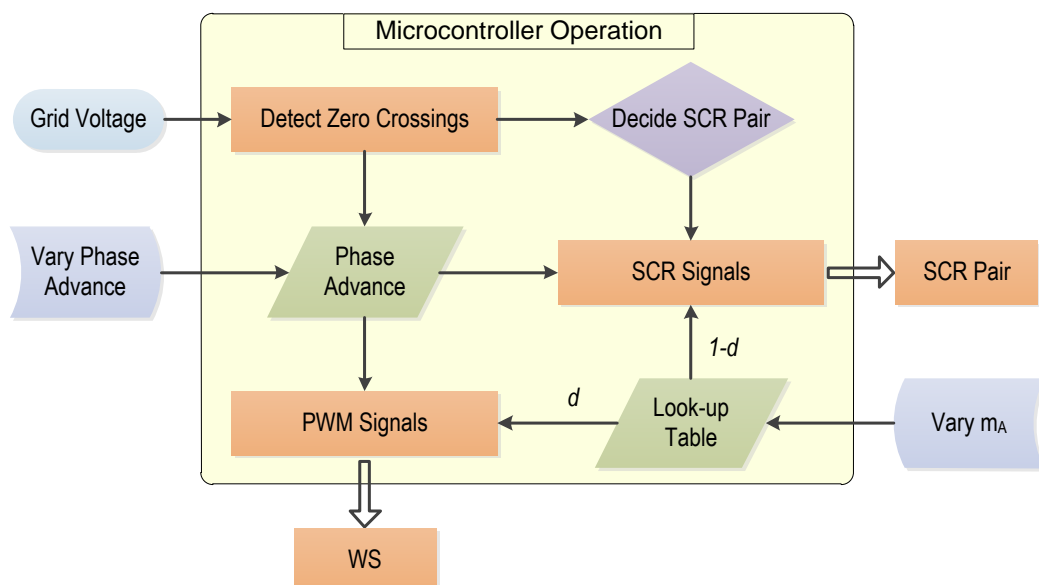


FIGURE 6.3: Simplified behavioural flow diagram of the microcontroller operation.

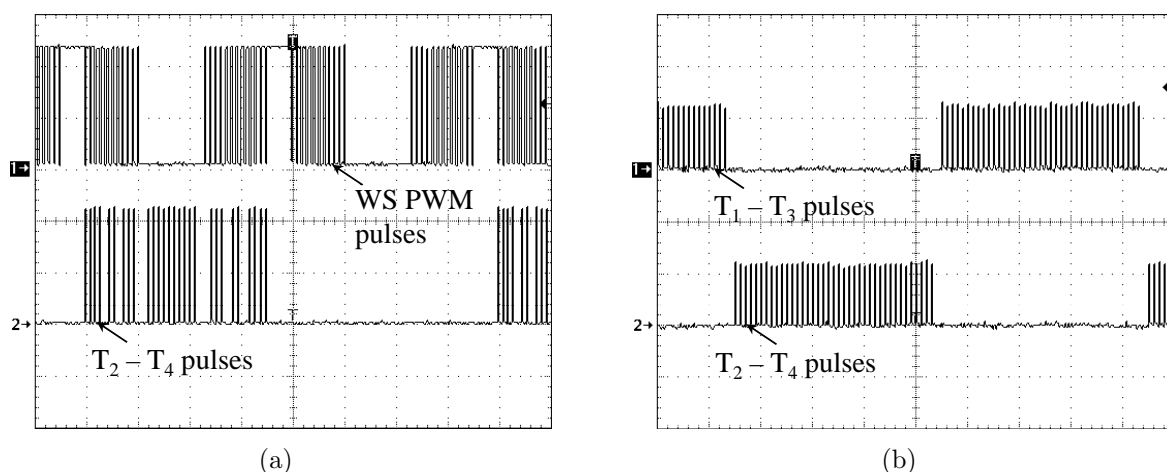


FIGURE 6.4: Measured (a) sinusoidal PWM signals from controller (top) SCR gating pulses (bottom), (b) microcontroller output for SCR pair's drive pulses.

## 6.2 Experimental System

As mentioned earlier, two CSI prototypes were used for the testing of the proposed grid-connected CSI concept. The first CSI prototype accommodated the converter topology that was used in a small-scale grid-connected wind generator application [22]. Since the first prototype did not consider optimised semiconductor devices and DC link inductor, the second CSI prototype was constructed using components which have less power loss than the first prototype. The proof of concept demonstration will be provided with



the first prototype and rest of the chapter will contain analysis related to the second (optimised) prototype (see Fig. 6.5).

### 6.2.1 First CSI Prototype

The first CSI prototype was rated at 80 W. A photo of it is shown in Fig. 6.5(a) and its semiconductor parameters are given in Table 6.1. This prototype is constructed using: adjustable power supply, single PV module (BP380), DC link energy storage inductor, waveshaper (consists of a MOSFET and a fast recovery diode), module thyristors, capacitor bank (100-600 $\mu$ F), resistor bank (0.1-300 $\Omega$ ), autotransformer, isolation transformer, microcontroller (Mitsubishi MSA0654A), mosfet driver (HCPL-3120), pulse transformers (PT6) and zero-crossing detection circuit (using LM 311N).

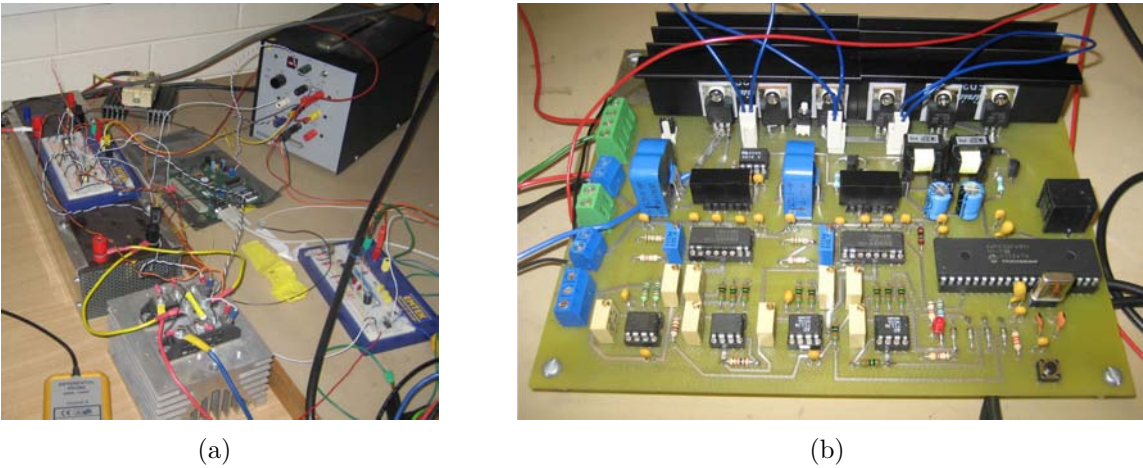


FIGURE 6.5: Photo of the CSI prototypes (a) first setup and (b) second (optimised) setup.

TABLE 6.1: First inverter prototype semiconductor properties.

Property	MOSFET	Diode	SCR
Manufacturer	IR	IR	SEMIKRON
Part Number	IRFP150N	70HFLR	SKKT 42
Rating	100 V, 42 A	1000 V, 70 A	1200 V, 40 A
Voltage Drop	-	1.85 V	1.95 V
On Resistance	0.036 $\Omega$	-	-
Latching Current	-	-	0.6 A
Holding Current	-	-	0.25 A

The detailed component specifications of the prototype grid-connected PV CSIs are given in Table 6.2.

TABLE 6.2: Parameters of the two CSI prototypes.

Parameter	Prototype 1	Prototype 2
Rated maximum input power ( $P_0$ )	82 W	164 W
Input current for $P_0$ ( $I_0$ )	4.5 A	4.5 A
Input voltage ( $V_{CELL}$ )	17.5 V	35 V
DC Link Inductance ( $L_{DC}$ )	82 mH	192 mH
DC Link Inductance Energy Storage ( $E$ )	$\approx 10$ mJ/W	$\approx 12$ mJ/W
DC Link Inductor Resistance ( $R_{LDC}$ )	1.3 $\Omega$	0.33 $\Omega$
Filter Inductance ( $L_F$ )	0.2 - 0.3 mH	2.9 mH
Filter Capacitance ( $C_F$ )	100-600 $\mu$ F	21 $\mu$ F
Filter Inductor Resistance ( $R_L$ )	0.3 $\Omega$	0.16 $\Omega$
Filter Damping Resistance ( $R_D$ )	0.3-0.5 $\Omega$	44.5 $\Omega$
SMR Switch Resistance	0.036 $\Omega$	0.033 $\Omega$
SCR Voltage Drop	1.95 V	1.3 V
Diode Voltage Drop	1.85 V	0.7 V
PWM Switching Frequency	4 kHz	4 kHz

### 6.2.2 Verification of the First CSI Prototype

Considering the low-voltage DC output from a single PV module, the CSI was grid-connected using a 10 A autotransformer, whose secondary voltage was varied between 5 and 20  $V_{RMS}$ . In addition, an isolation transformer was connected between the mains and the autotransformer for safety, as shown in Fig. 6.6. The figure shows the CSI test arrangement in the laboratory, which includes a resistive load,  $R_L$  and two switches,  $S_1$  and  $S_2$ , which are used to make the transition from resistive loading to grid connection. This procedure will be explained further in grid-connected testing.

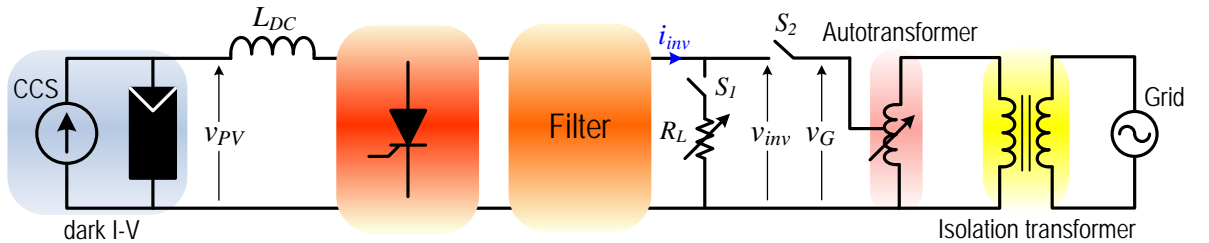


FIGURE 6.6: Grid-connected CSI test arrangement, showing an isolation and auto-transformer.

### Resistive Loading

The grid connection was performed in three stages. The inverter was initially operated into a resistive load as the first stage. Fig 6.6 shows the block diagram of the test arrangement. Note that in this stage the resistive load switch  $S_1$  is on and the grid switch  $S_2$  is off.

The simulation and test results (see Fig. 6.7) of the CSI illustrate its key principles : The power source acts as a current source, and the waveshaper acts as a PWM current chopper which produces a waveform whose fundamental component is a full-wave rectified sinewave. The unfolding circuit changes the polarity of the output current.

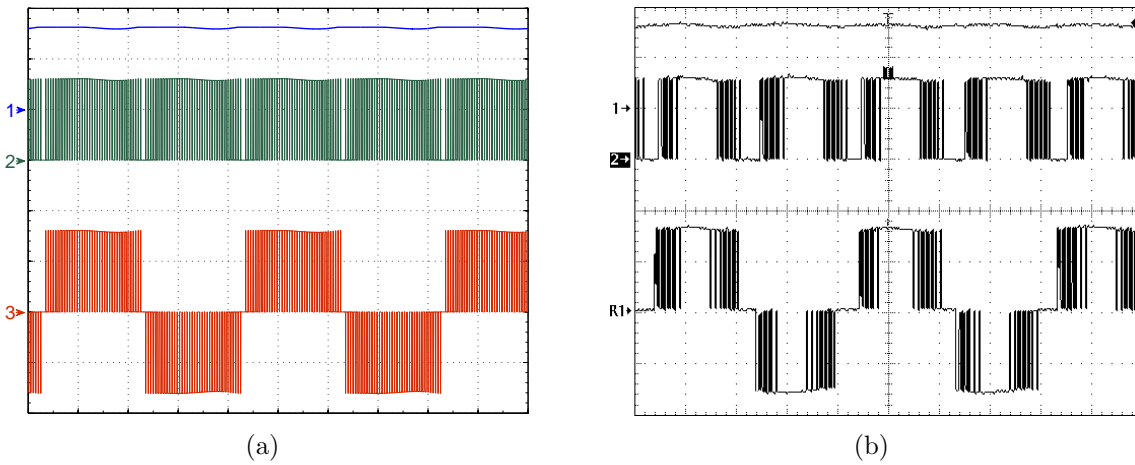


FIGURE 6.7: (a) *Simulated* and (b) *measured resistive load current waveforms for unity  $m_A$ ; from top to bottom : PV array output, WS output and UC output. The vertical and horizontal scales are 3 A and 5 ms per division respectively.*

### Grid-Connected Testing

Once it has been demonstrated that the resistive load and grid voltages are synchronised, switch  $S_1$  is closed and the grid (autotransformer output) is connected in parallel with the resistive load (intermediate grid-connection stage). In this second stage, ideally the grid should provide zero current and the output power of the inverter should still be absorbed by the load resistance. Then the third stage involved removing the load resistor and hence feeding the inverter output power into the grid (see Fig. 6.6).

The simulated and experimentally measured inverter output current for the resistive load, the resistive load with grid-connection, and the pure grid-connection can be seen in Fig. 6.8 for an autotransformer output voltage of 16  $V_{RMS}$  at nominal  $m_A$ . This corresponds to 0.92 modulation index. The ratio between the nominal PV array voltage and

the peak grid voltage  $v_{PV}/V_{PK}$  is 0.87 based on the analysis given earlier in Section 4.3.2. This ratio is higher than the idealised value of 0.425 under optimal GC CSI operation due to the resistive loss in the DC link inductor and voltage drops in the diode and SCRs. The other drawback to having a nominal  $m_A$  of 0.92 is that there is more limited range to increase  $m_A$  to allow MPP tracking under low temperatures (see Fig. 4.5(b)).

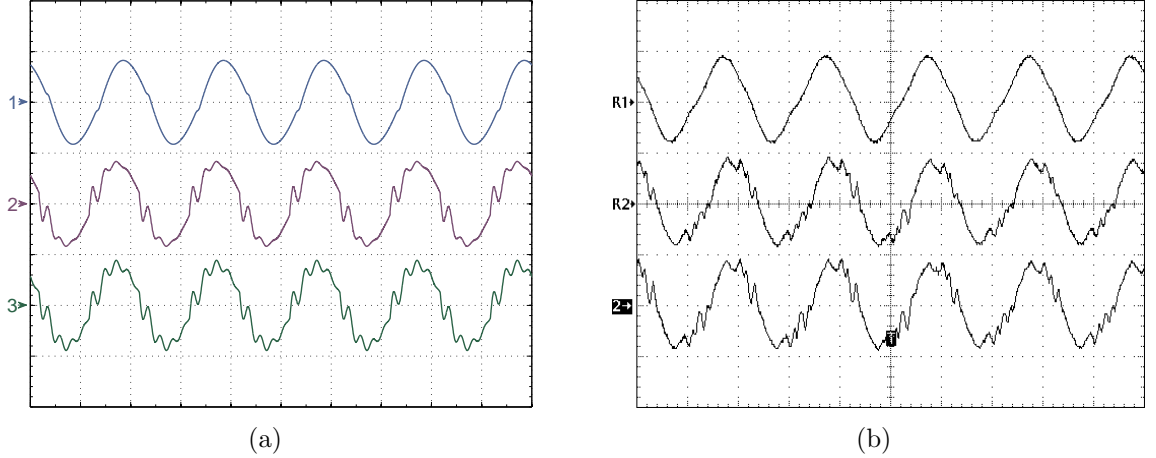


FIGURE 6.8: Comparison of the inverter output current waveforms for resistive load (top), resistive load parallel to the grid (middle), and grid-connected load (bottom) for nominal  $m_A$  (a) simulation and (b) test results. The vertical and horizontal scales are 5 A and 10 ms per division, respectively.

Fig. 6.8 shows the distortion of the output current waveforms especially during the second and the third (pure grid-connected) cases. The  $Q$  of the low-pass output filter is around 2 which corresponds to a high THD and loss ( $P_d$ ) at the rated output power (see Fig. 5.8). Due to large capacitance in the low-pass filter there is a significant phase delay and this is not fully compensated in the microcontroller. This causes undesirable harmonic content in the CSI output current. Furthermore, the energy storage capacity of the DC link inductor is only 10 mJ/W which may not be sufficient to reduce the 100 Hz fluctuation effect on THD as seen in Fig. 4.10(a).

### 6.2.3 Second CSI Prototype

The power input for the second prototype is 160 W which is supplied by two series connected BP 380U solar modules. Fig. 6.5(b) showed the second CSI prototype, which featured a more careful selection of the power electronics devices constructed on a PCB. In

addition, a DC link inductor was designed and constructed to reduce copper losses. The detailed inductor design and its analysis is provided in Appendix A. A low-pass output filter was designed based on the analysis in Chapter 5. A more powerful microcontroller (dsPIC30F4011) was chosen. Detailed circuit schematics are found in Appendix B.

The parameters of the CSI were shown previously in Table 6.2 as well as in Fig. 6.1. Table 6.3 provides the switching ratings of the second prototype.

TABLE 6.3: *Optimised inverter prototype semiconductor properties.*

Property	MOSFET	Diode	SCR
Manufacturer	IR	IR	IR
Part Number	IRF540N	8TQ100PBF	16TTS08
Rating	100 V, 33 A	100 V, 8 A	800 V, 16 A
Voltage Drop	-	1.1 V	1.35 V
On Resistance	0.04 $\Omega$	-	-
Latching Current	-	-	0.2 A(max)
Holding Current	-	-	0.1 A

## 6.2.4 Verification of the Second CSI Prototype

In this prototype, an isolated autotransformer is used to connect to the grid (see Fig. 6.6). The grid voltage via the autotransformer was set to 54 V<sub>RMS</sub>. The autotransformer was modeled by an equivalent series inductor of 174  $\mu$ H and series resistance of 0.67  $\Omega$  (see Fig. 6.1) based on measurements.

### Resistive Loading

As in the first prototype, the CSI was initially connected to a resistive load using the switch  $S_1$  (see Fig. 6.6). The simulated and measured inverter output current and voltage waveforms for a 21  $\Omega$  resistive load are shown in Fig. 6.9. There is no phase advance  $\alpha$  in the reference signal of the simulation. However a phase advance value of 2.7° in the microcontroller was required for the test results in Fig. 6.9(b). These show excellent agreement with the simulations.

As shown in the figure, the output current of the inverter is nearly sinusoidal. This is due to filter damping produced by the resistive load (as in FC 2 shown in Table 5.1).

The resistor has the full fundamental output voltage across it, and there is no phase delay between the CSI voltage and current waveforms.

The resistive output current of the first prototype in Fig. 6.8 seems slightly distorted compare with the second prototype due to the non-optimised low-pass output filter which has a large normalised output capacitor value of 0.33 pu.

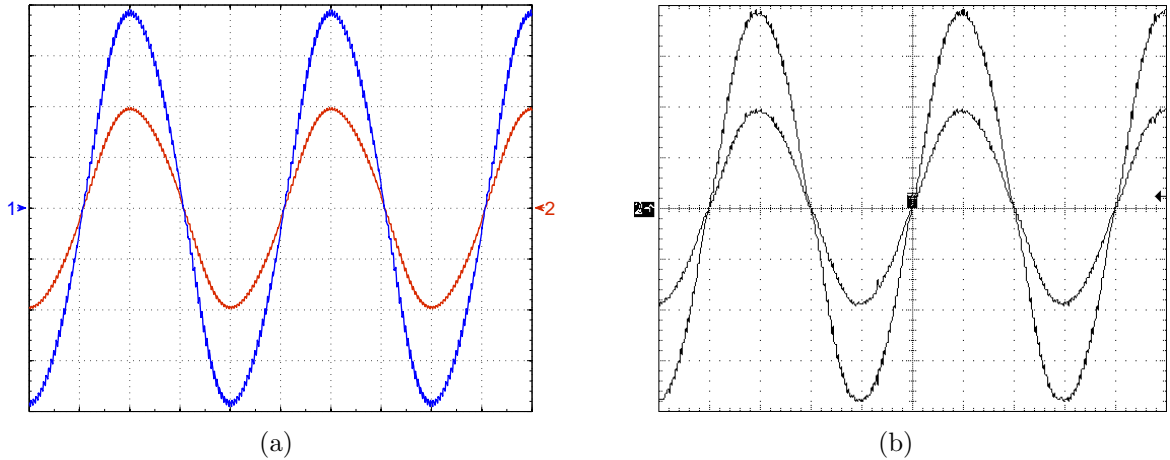


FIGURE 6.9: (a) *Simulated and (b) measured CSI output voltage and current for resistive load case at nominal  $m_A$ . The vertical scales are 20 V and 2 A and horizontal scale is 5 ms per division.*

### Grid-Connected Testing

Fig. 6.10(a) shows the simulated PV array output current and the grid-connected inverter output current at the nominal modulation index. The CSI output voltage is set to 54 V<sub>RMS</sub> to be the same as the autotransformer voltage for synchronisation. The control circuit phase advance  $\alpha$  was set to 13° in the simulation model to have a good agreement with the test results in Fig. 6.10(b). There is a substantial difference between the phase advance values used in the simulation model and the prototype (2.7°). This needs to be improved by fine tuning the control algorithm as the CSI prototype requires the correct phase advance value for proper unfolding operation with the existing algorithm.

Compared to the first prototype, the output current THD is improved from 21% to 8.1% using the optimised low-pass filter with open-loop control. However the 8.1% THD value still exceeds the grid requirement of 5%. This could be due to the approximations in the look-up table. Therefore a harmonic elimination method can be used to reduce THD in the look-up table [40]. Alternatively, it may be due to issues with the phase advance used.

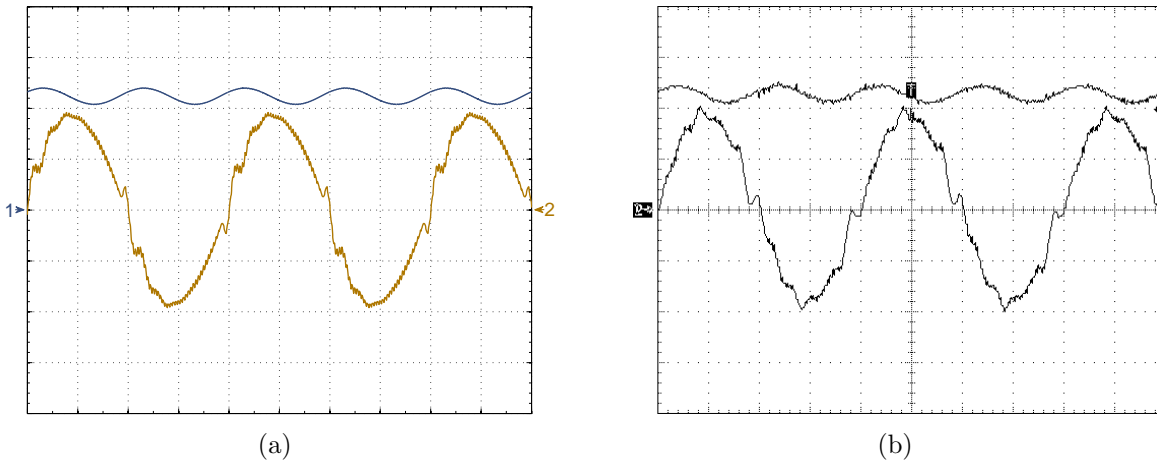


FIGURE 6.10: (a) *Simulated* and (b) *measured* CSI input and output currents for grid-connected case at nominal  $m_A$ . The vertical and horizontal scales are 2 A and 5 ms per division, respectively.

## 6.3 Performance Analysis of the Second Prototype

The grid-connected inverter was tested to examine its performance in the following areas :

- use of modulation index control to maximise the output power for a given irradiance condition
- ability to meet the grid THD requirement of 5% at rated output power,
- ability to meet the grid power-factor requirements of 0.8 leading to 0.95 lagging from 20% to 100% of rated output power, and
- efficiency over the output power range.

During the tests, the dark I-V current source was set to the level to simulate standard irradiance conditions.

### 6.3.1 Modulation Index and Irradiance Adjustments

Simulation and test results are shown in Fig. 6.11(a) where the output power is varied using the modulation index.  $P_0$  corresponds to the MPP where the  $m_A$  is 0.85 and the power is maximum. As mentioned in Chapter 4, the  $m_A$  of 85% is the optimum

value for the CSI and this is shown in Fig. 6.11(a). The nominal  $m_A$  is chosen based on the trade-off between the ability for tracking the MPP under cold conditions versus the inverter efficiency as analysed in Chapter 4. This figure shows that the output power is directly proportional to  $m_A$  as indicated in Fig. 4.7(c) as well as in Tables 4.4 and 4.5. The measured results show a good agreement with the simulations.

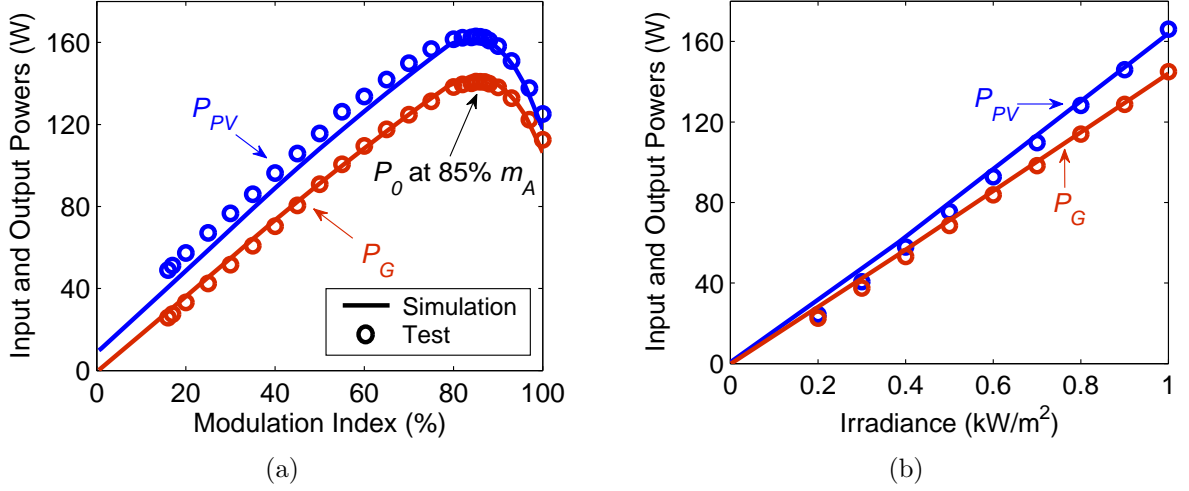


FIGURE 6.11: Simulated and measured CSI input ( $P_{PV}$ ) and output ( $P_G$ ) powers for various (a) modulation index and (b) irradiance values (operating at MPP).

The input and output power versus irradiance curves are shown in Fig. 6.11(b). As mentioned in Section 4.3.5 the irradiance reduction results in an average power reduction as the PV array output current is directly proportional to irradiance. Whereas the PV array output voltage is proportional to the modulation index while the current stays relatively constant due to the PV array I-V characteristics. Conduction losses are the major loss mechanism in the inverter and hence its losses increase with the PV array current. Due to the relatively constant current in the constant irradiation case in Fig. 6.11(a), the difference between the PV array output and the CSI output power remains almost constant.

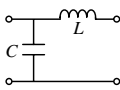
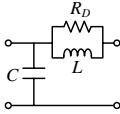
However in the changing irradiance case in Fig. 6.11(b), the power loss reduces proportional to the PV array output current which results in higher efficiency at low output power levels.



### 6.3.2 Total Harmonic Distortion

The output filter types, their parameters and the CSI output current THD results for the three different loading cases are shown in Table 6.4. The first prototype (80 W) results are compared with the second prototype (160 W). The CL filter arrangement for the first prototype has a series damping resistance (similar to FC 4 in Chapter 5) due to the autotransformer (see Table 6.2). As this low-pass filter is not optimised, the THD values are significantly high as mentioned in Section 6.2.2. Even though the optimised low-pass filter reduced the THD in the CSI output current it is still higher (8.1%) than the limit set by the Australian Standards [9]. Further study will be needed to reduce the THD to the acceptable level.

TABLE 6.4: *Inverter output filter types and parameters showing quality factor, resonance frequency and normalised capacitance. The loading arrangements for three different cases and THD values are also provided.*

Setup	Filter	$Q$	$f_R$	$C_n$	Arrangement	THD
Prototype 1		2	649 Hz	0.33 pu	Resistive Load	9.27 %
					Resistive + Grid	16.0 %
					Grid	21.2 %
Prototype 2		4	646 Hz	0.12 pu	Resistive Load	4.3 %
					Resistive + Grid	7.7 %
					Grid	8.1 %

The simulation and test results of the CSI output current THD by changing both the  $m_A$  and  $G$  values are shown in Fig. 6.12. Though there is a good correspondence in the THD at rated output conditions, there is a substantial error in the simulated results under light loads. This could be due to the switching losses in the power electronics devices and may be due to the modified phase advance angle to match with the rated output power test results. As indicated before, the phase angle value which is added to simulation model is larger than the value used in the microcontroller. Based on the analysis in Chapter 5, the phase advance angle is directly proportional to the output power. Therefore for the light loads, a smaller phase advance is required. In addition the large phase angle ( $13^\circ$ ) provides good correspondence with the rated output power but exhibits a significant THD compared with the test results for light loads.

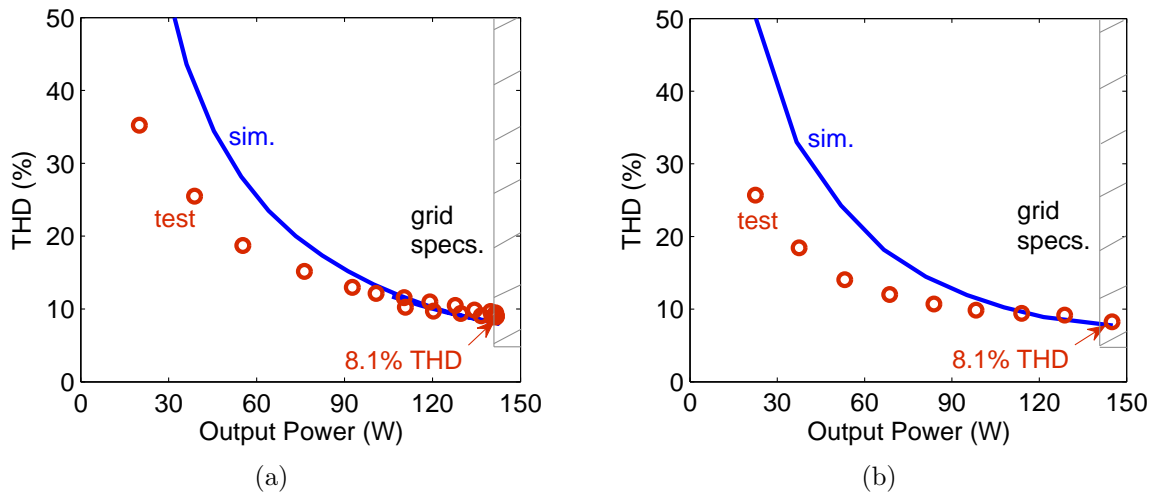


FIGURE 6.12: *Simulated and measured CSI THD as a function of output power for various (a) modulation index and (b) irradiance values (operating at MPP) .*

Likewise in the changing irradiance case, the test results show a good agreement with the simulations for the rated output power. In the test results the output current THD for the  $G$  variations is lower than constant irradiance case in Fig. 6.12(b).

### 6.3.3 Power Factor

Fig. 6.13(a) shows the simulated and measured results for the grid power factor as a function of modulation index. Note that during these studies the current was always leading, and the power factor is defined from the grid's point of view with regards to a passive load. The figure shows that the grid power factor requirement of at least 0.8 leading over the output power range of 20% to 100% of rated output has been met.

Fig. 6.13(b) illustrates power factor curves for the varying irradiance condition and similar to the modulation index variations, the grid specification of the power factor is achieved. Due to operating at the MPP for each irradiance case, the PF for the light loads is slightly better for the varying irradiance case in Fig. 6.13(b).

Observing the results from the analysis in Section 5.3, it can be concluded that it is not difficult to meet the grid PF requirements for different filter parameters. The simulation and test results in Fig. 6.13 also verify this conclusion.

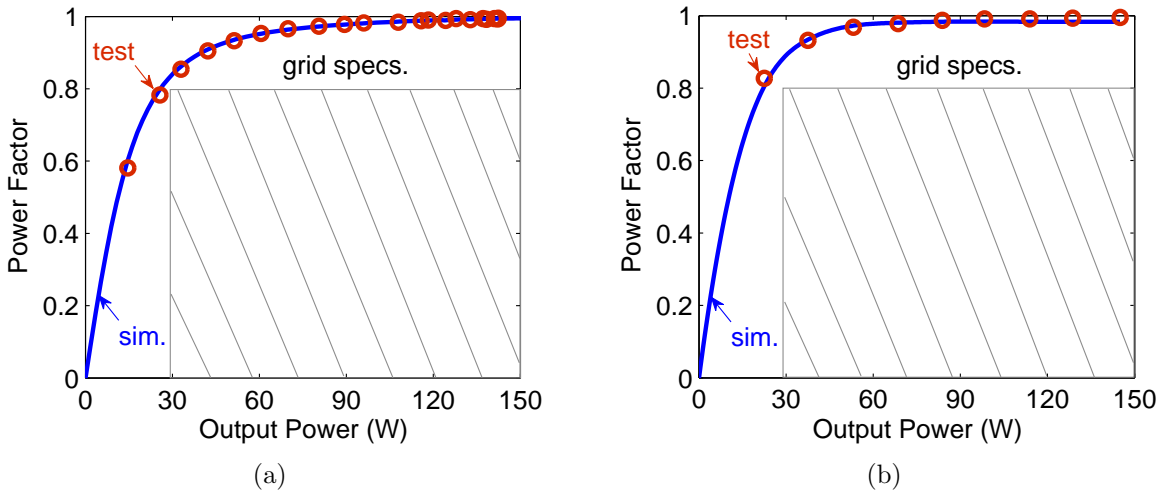


FIGURE 6.13: Simulated and measured CSI power factor as a function of output power for various (a) modulation index and (b) irradiance values (operating at MPP).

### 6.3.4 Efficiency

The inverter efficiency can be measured using the input power  $P_{PV}$  and the output power  $P_G$ . The efficiency measurement was performed using a power analyser (Voltech-PM3000A). Though there is a good correspondence in the efficiency at rated output conditions, there is a substantial error in the simulated results under light loads for the initial test results (see Fig. 6.14(a)). The error may be due to wirings between the inverter and the external measuring devices, such as the power analyser. Although the cables used are capable of carrying the maximum current (4.8 A) they have significant copper losses. In another measurement the thickness of the cables was increased, which resulted in higher efficiency and simulation results show a good agreement with the measured results.

Fig. 6.14(b) illustrates the efficiency as a function of output power at the MPP for each irradiance value. The resultant efficiency curve is different than that obtained by changing  $m_A$  with constant irradiance as the PV array output current is proportional to irradiance. This results in lower resistive losses, and hence higher efficiency.

The CSI power loss breakdown as a function of output power for the varying modulation index case is shown in Fig. 6.14(c). It shows the power loss of the various stages of the grid-connected CSI including the DC link inductor copper and iron losses, the WS MOSFET and diode, the UC and the low-pass filter. As it can be seen in the figure,

the UC voltage drops and the DC link inductor copper losses are a large fraction of the total loss for the nominal conditions. As the  $m_A$  is reduced, the average PV output current increases slightly and hence the DC link inductor copper loss increases. The WS MOSFET conduction loss is proportional to the square of the rms MOSFET current. In addition the duty cycle of the MOSFET is inversely proportional to  $m_A$ . As a result, the MOSFET losses increase more rapidly compared to the DC link inductor losses when  $m_A$  is decreased. The diode, UC and low-pass filter power losses are all proportional to the WS output current.

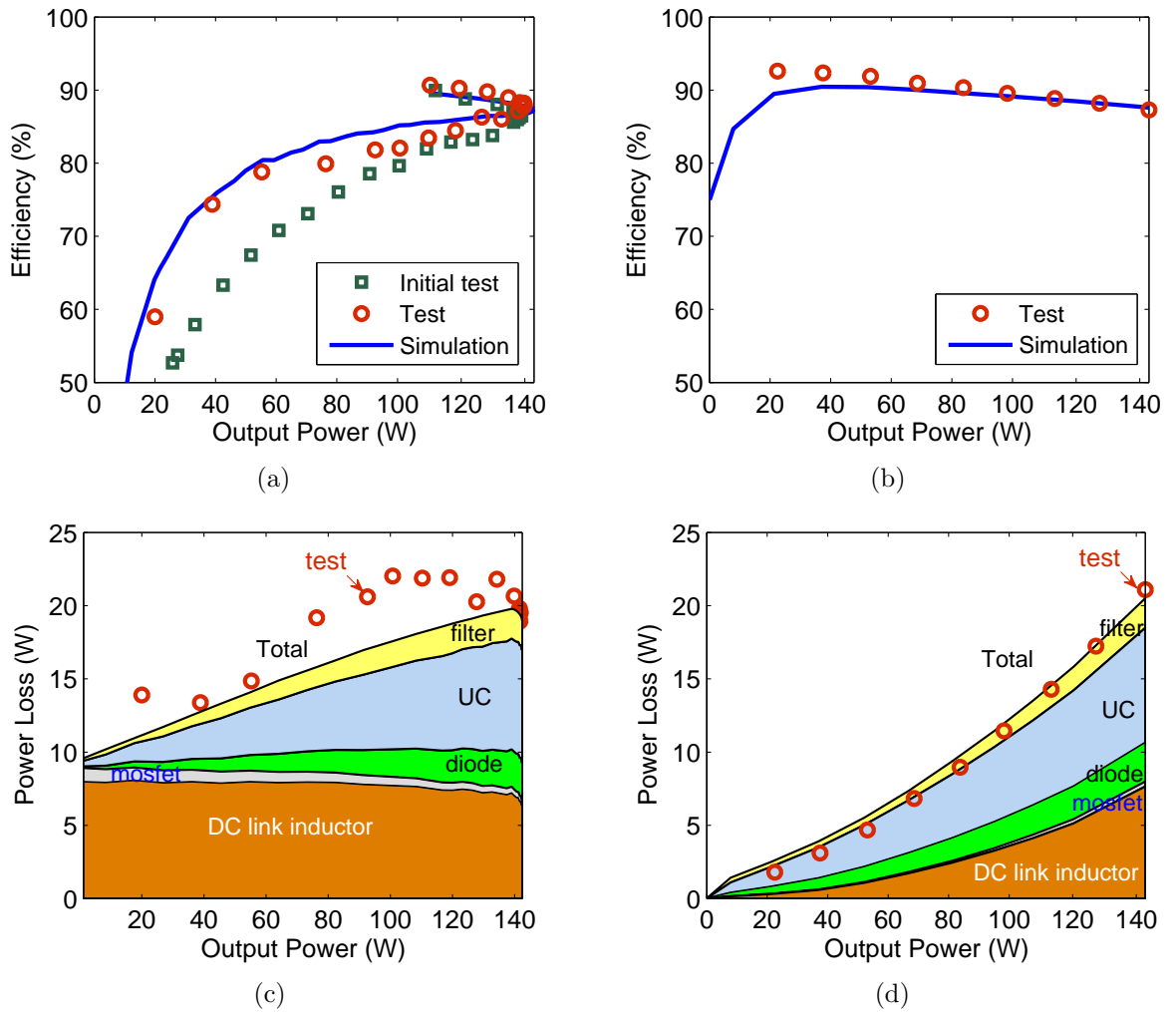


FIGURE 6.14: Simulated and measured CSI efficiency as a function of output power for various (a) modulation index (b) irradiance values. CSI loss breakdown as a function of output power for various (c)  $m_A$  and (d)  $G$  values. Note that the PV array 100 Hz ripple power reduction is not included.

The loss breakdown for the varying irradiance case is shown in Fig. 6.14(d). In contrast with constant irradiance case, the DC link inductor and MOSFET losses are proportional

to the square of the output power. This is the reason the overall efficiency of the CSI increases when the irradiance reduces. The other components have about the same losses as the constant irradiance case in Fig. 6.14(c). The rest results show a good match with the calculated values.

Fig. 6.15 shows the calculated rated power loss breakdown of the CSI at the MPP (input power 164 W and total loss 19 W). The unfolding circuit (UC) has the largest fraction of the losses due to the SCR's voltage drops. The DC link inductor losses (copper and iron) are slightly less than UC losses. The PV array 100 Hz output power reduction is relatively high. Although, this can be reduced by using a higher energy storage value than 12 mJ/W, it will increase the DC link inductor losses. Therefore, further optimisation study will be needed to address this. For this application the 12 mJ/W is determined as a reasonable starting point.

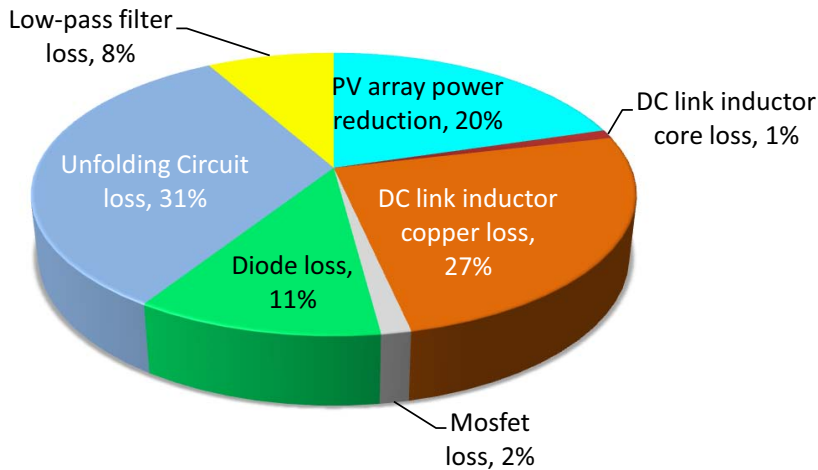


FIGURE 6.15: Calculated rated loss breakdown of the 160 W prototype.

As can be seen from the efficiency curve in Fig. 6.14, the measured efficiency at the maximum power point ( $m_A = 85\%$ ) shows a good correspondence with the calculated results. The measured peak efficiency is around 90.4% for unity  $m_A$ . The slightly low efficiency (88% at nominal  $m_A$ ) of the CSI is partly due to the low output voltage of the prototype. Increasing the AC output voltage will correspondingly reduce the effect of the voltage drops of the components, however, this will increase the switching losses. The analysis of a higher power CSI will be given in Chapter 7.

## 6.4 Feedforward Implementation and Results

There are two alternatives for improved control of the AC output current waveform : feedback and feedforward control. Conventional voltage-source current controlled inverters employ the feedback control by measuring the output current.

The feedforward control principle is to sense the perturbation and then control the system to compensate for its effect. Adding feedforward to closed-loop systems gives faster response and better control of the operating trajectory. If the system model is exact then feedback control is not required. Another important difference is that feedback techniques need to measure the controlled variables. The controlled variables (output to the system) are chosen according to the control objectives [41] and hence feedback control requires more sensors compared to the feedforward approach. As a result, the feedforward approach can be less expensive and faster solution.

### 6.4.1 Feedforward Compensation Control

Initially it was assumed that the inverter is fed by an ideal constant current source. However the PV current has 100 Hz ripples which result in power reduction and harmonic content in the inverter AC output current. To reduce the THD, the DC link inductor must have a large energy storage capacity (see Fig. 4.10(a)). However oversizing the inductor would make it heavy. The feedforward control approach can be a solution to reduce the inverter output current THD for this application (see Table 5.3). However the feedforward control will not change the PV array 100 Hz fluctuation power reduction.

Feedforward current control was first discussed in a single-phase AC/DC for converter input power factor correction [36]. The basic idea is to generate a “nominal duty ratio pattern” to reduce the task of the feedback controller to eliminate some low-order harmonics. The feedforward approach is introduced into the proposed converter by including the sensed PV array output current  $i_L(t)$  and the desired WS output current  $I_{L0}$  amplitude to the open-loop control in (6.2). The relationship between the input and output current of the WS is seen in (6.3) for feedforward control. Due to the PV array characteristic, the actual PV array current  $i_L(t)$  is not equal to the nominal PV array output current  $I_{L0}$ . The algorithm to compensate the variations in  $i_L(t)$  by selecting the

duty-cycle  $d(t)$  is shown in (6.3).

$$1 - d(t) = \frac{i_{IN}^*(t)}{i_L(t)} \quad \text{where} \quad i_{IN}^*(t) = I_{L0} m_A |\sin(\omega t)| \quad (6.3)$$

where  $i_{IN}^*(t)$  represents the desired output current. Fig. 6.1 showed the control circuit implementing the algorithm.

## 6.4.2 Proof of Feedforward Implementation

Fig. 1.13 shows the current source inverter with feedforward control. In order to test the feedforward implementation is working reasonably well, some of the operation characteristics have been examined below;

1. Input current variation effect,
2. FFT analysis of the output current.

### Input current variation effect

To observe this effect the unfolding circuit was disconnected. The sinusoidal PWM chopped WS output is connected to a RC low-pass filter to obtain a rectified sinusoidal output waveform. Fig. 6.16 shows current waveforms for the open-loop and feedforward cases. Fig. 6.16(a) gives the input and output current of the waveshaper with a modulation index of 40%. When the input current is halved the output current is immediately halved. However for the FFD case in Fig. 6.16(b), the output current is forced to remain the same as the desired ( $i_{IN}^*(t)$ ) value is not changed. The output current will be controlled to remain the same until the provided input current is smaller than the desired current value based on (6.3).

### FFT analysis of the output current

The measured grid-connected inverter current waveforms and their FFT spectrums at nominal  $m_A$  are provided in Table 6.5. Although they have high harmonic content there are slight differences between the current waveforms. Utilising FFD control reduces the THD by around 1%. The 3<sup>rd</sup> harmonic expected to be eliminated relative to analysis in Table 5.3. The 3<sup>rd</sup> harmonic has a slight reduction and the 9<sup>th</sup> harmonic has higher

reduction than the OL case while the others remain relatively similar. These results imply that the output current distortion is not due to the 100 Hz PV array output current ripple.

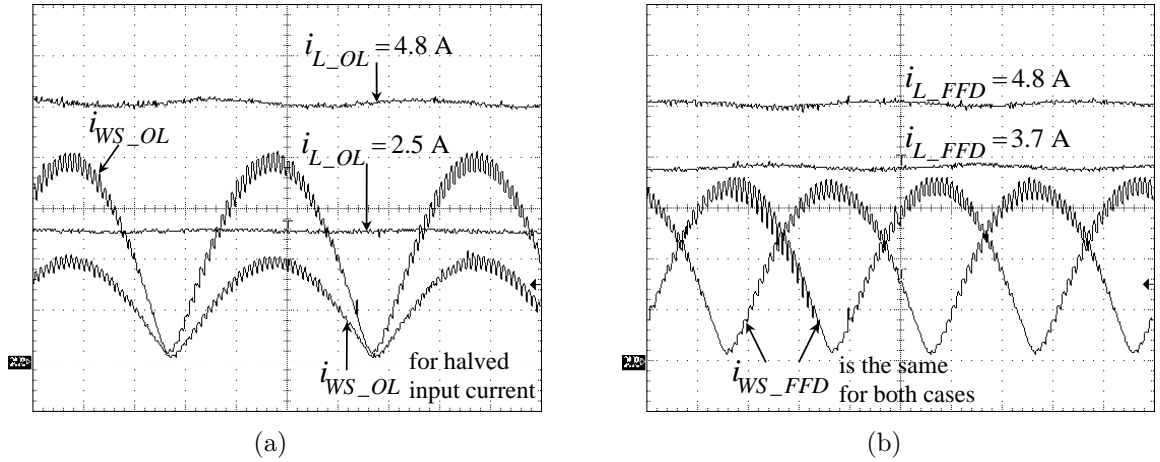


FIGURE 6.16: Measured WS input and output currents at 40%  $m_A$  (a) open-loop control and (b) feedforward control cases. The vertical and horizontal scales are 1 A and 2.5 ms per division respectively.

TABLE 6.5: Measured output currents of the CSI and their FFT spectrums for open-loop and feedforward control cases.

Control	CSI Output Current	FFT
Open-loop		
Feedforward		



## 6.5 Summary

This chapter examined the implementation of the 80 W and 160 W current-source grid-connected PV inverter prototypes. The first prototype is implemented as a proof of concept demonstration. Then the performance of the second prototype is examined more carefully. It was shown that the inverter could meet the grid power factor requirement over the required 20% to 100% of output power but that the inverter THD of 8.1% at rated output power did not meet the 5% requirement. This is due to unwanted delays in the system or the look-up table implementation [40].

The efficiency of the inverter was examined over a range of output powers for modulation index and irradiance variations. The calculated results showed a good correspondence with the measurements at rated output power. However, the measured efficiency at light load was lower than the predictions, likely caused by the unmodelled semiconductor switching and external cabling losses. Finally the feedforward compensation control is implemented and shown to improve the inverter output current waveform slightly. It is thus likely that the remaining output current distortion is due to the output filter phase delays causing issues with the unfolding current switching.

---

---

## CHAPTER 7

---

# DESIGN AND SIMULATION OF A HIGHER POWER GRID-CONNECTED INVERTER

This chapter employs the inverter analysis from previous chapters to design a higher power (1.2 kW) single-phase grid-connected current-source inverter that delivers high quality power to the grid. The aim of this chapter is to provide a systematic and detailed system design that also addresses practical issues with the inverter topology considered. The chapter begins with the selection of the solar array which is followed by the inductor sizing and the detailed inverter design. The inverter performance with open-loop and feedforward control is simulated and the THD and PF obtained. Finally, the efficiency of the inverter is analysed including a power loss breakdown comparing constant and variable irradiance cases.

## 7.1 Photovoltaic Array

### 7.1.1 Selection of Solar Array Voltage

In Chapter 4, it was shown that a design value of modulation index  $m_A$  of 0.85 gave a reasonable tradeoff between the inverter efficiency and the ability to track the MPP at low temperatures. For a 240 V (339 V<sub>peak</sub>) grid, equation (4.7) can be used to calculate the required nominal PV array voltage as 144 V. This estimate can be improved by including the voltage drops in the system as shown in Fig. 7.1. This figure shows the desirable voltage and current values along with estimates of the DC link inductor and switch resistances, and the voltage drops for the diode, SCRs, and the grid filter resistance. Considering these voltage drops in the voltage estimation the nominal PV array voltage is found as 152 V.

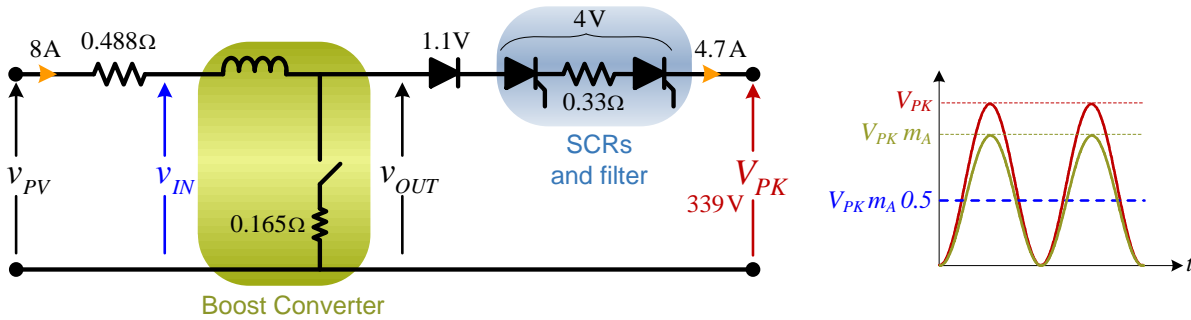


FIGURE 7.1: CSI circuit diagram showing voltage, current values and the voltage drops in the components of the system.

Note that Fig. 7.1 also illustrates the ideal voltage waveforms for peak grid voltage  $V_{PK}$ , output voltage scaled by the modulation index and the ideal required PV array input voltage.

### 7.1.2 PV Array Arrangement

As it is well known, PV cells are grouped into modules and the modules connected in arrays in a PV system. These arrays are connected in series and parallel to produce the desired output voltage and current. Therefore the PV array needs to be designed such that the inverter is able to deliver rated power to the grid at the chosen irradiance ( $G$ ) and temperature under nominal conditions.

As it was shown in the previous chapter, for the 160 W prototype inverter, two series 80 W PV modules (BP380U) were used. For higher power system six 200 W (BPSX3200) series-connected PV modules were chosen to achieve 1.2 kW power. Table 7.1 shows the properties of the proposed PV array. The nominal voltage at maximum output power of 147 V matches well with the desired value of 152 V. The slightly lower value of the voltage means that the nominal modulation index should be 0.82 rather than 0.85.

TABLE 7.1: Summary of the proposed 1.2 kW PV array properties based on six series-connected 200 W BP Solar (BPSX3200) modules.

Parameter	Value
Rated Maximum Power ( $P_0$ )	1.2 kW
Voltage at maximum power $P_0$ ( $V_0$ )	147 V
Current at maximum power $P_0$ ( $I_0$ )	8.16 A
Short Circuit Current ( $I_{SC}$ )	8.7 A
Open Circuit Voltage ( $V_{OC}$ )	184 V
Resistance for array ( $R_S$ )	0.13 $\Omega$

Fig. 7.2 shows PSIM simulation model for the proposed PV array which is based on the 4-diode PV model

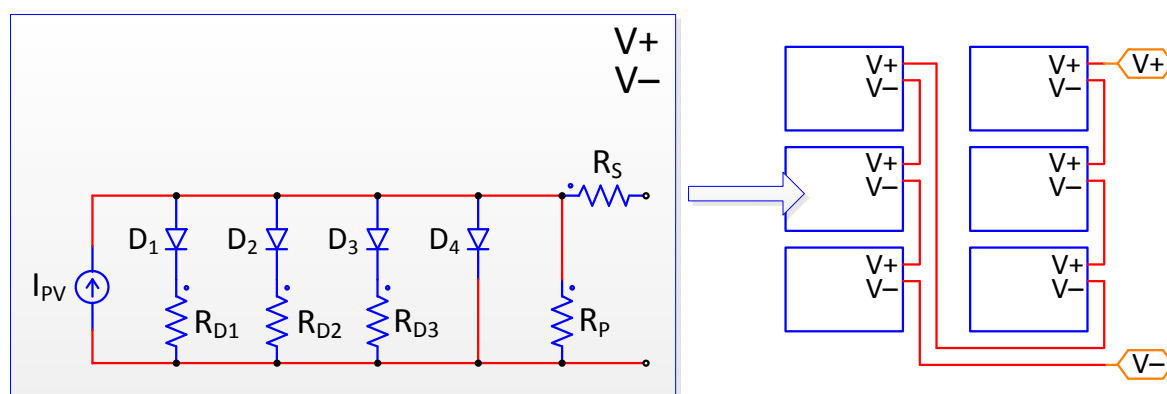


FIGURE 7.2: PV array simulation model which consists of six series 4-diode models to produce the required 1.2 kW input power.

Fig. 7.3 shows a comparison of the I-V curves of the PV array comparing the 4-diode model versus the non-linear PV model based on (2.1). As it can be seen in the figure there is a good correspondence among the I-V curves. As a result 4-diode model will be used in the simulation studies.

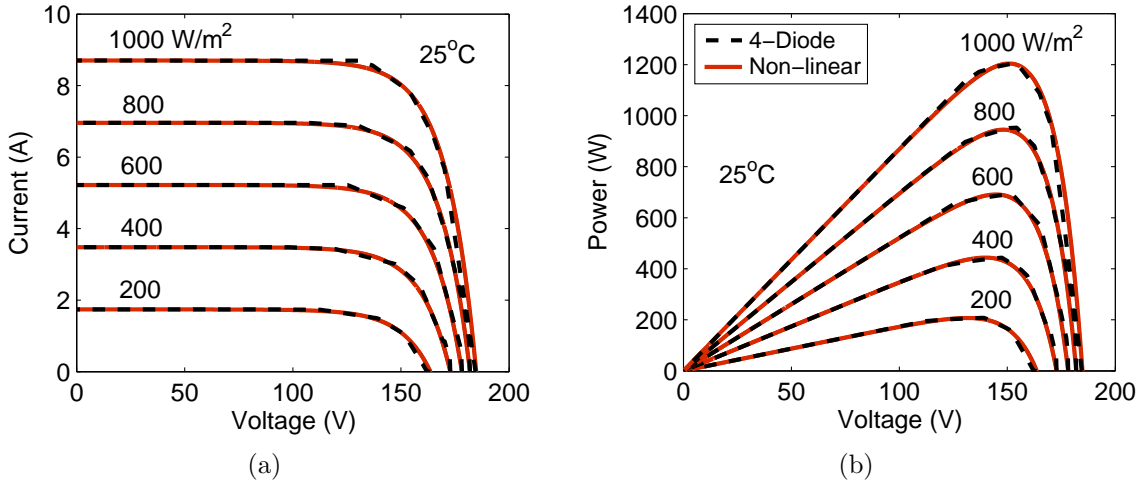


FIGURE 7.3: (a)  $I$ - $V$  and (b)  $P$ - $V$  curves of the 1.2 kW PV array under several irradiance values: 200, 400, 600, 800 and 1000  $W/m^2$  at 25°C for the non-linear model (solid lines) and 4-diode model (dashed lines).

## 7.2 DC Link Inductor

As it was discussed previously, single-phase CSIs require a DC link inductor which is an energy storage component and acts as a constant-current source. The DC link energy storage reduces the PV array output current ripple and hence the PV array output power reduction as mentioned in Chapter 3.

Fig. 7.4 shows the calculated output power reduction for the PV array as a function of the amount of energy storage based on the balanced ripple definition and the energy storage calculations in Chapter 3.

### 7.2.1 Required Energy Storage Assumption

An inductor was designed for the 1.2 kW inverter using the procedure described in Appendix A. The number of turns of the inductor was scaled appropriately to give the desired total inductance value and rated current. Its parameters are shown in Table 7.2. It has a stored energy of about 15 J. This corresponds to about 12 mJ/W which interestingly matches the minimum value found in Chapter 4. This achieves desirable values of output THD under open-loop control.

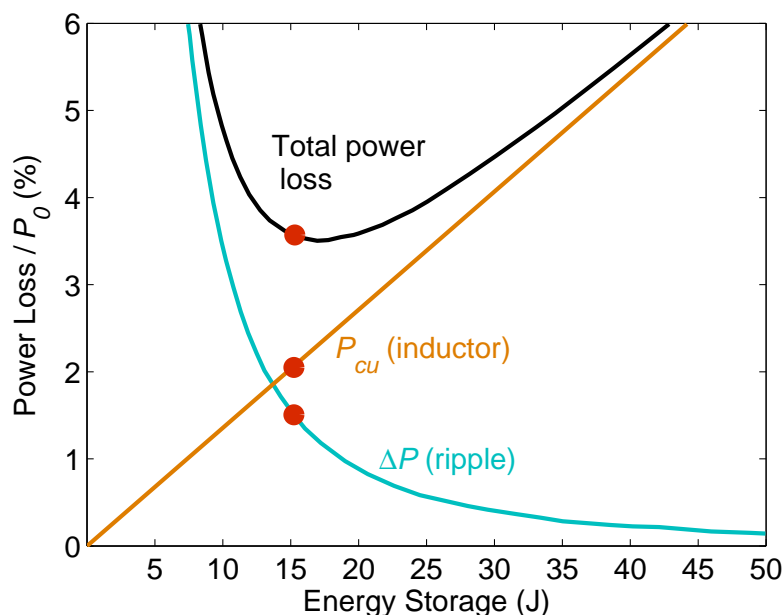


FIGURE 7.4: Inductor design trade-off graph, showing the ripple power loss, inductor power loss and total power loss versus energy storage.

TABLE 7.2: Parameters of the inductor for the 1.2 kW PV CSI.

Parameter	Values
Rated maximum input power ( $P_0$ )	1200 W
Input current for $P_0$ ( $I_0$ )	8 A
Input voltage ( $V_0$ )	148.5 V
Inductance ( $L$ )	455 mH
Stored energy	15.2 J
Diameter of the copper wire	2.4 mm
Number of turns ( $N$ )	144
Resistance at 40°C ( $R_{CU}$ )	0.488 $\Omega$
Power losses in the inductor ( $P_{CU}$ )	40 W
Current ripple (peak-to-peak)	12.6 %
Peak flux density ( $B$ )	1 T
Copper winding packing factor	0.35
Volume	0.023 m <sup>3</sup>

Fig. 7.4 also illustrates the trade-off for a 1.2 kW inverter with regards to its sizing, energy storage and losses. Note that lower copper losses could be obtained by increasing the size (and cost) of the inductor. Combining the PV array power reduction curve and the inductor copper loss curve gives a total power “loss” curve. This illustrates the trade-off between the two types of losses with the optimal power reduction of about 4%. Note for a VSI, the DC link energy storage losses would be much smaller resulting lower power reduction.

### 7.3 Switching Component Ratings

The components for the high power grid-connected inverter were selected to increase the overall inverter efficiency. Hence, components with low forward voltage drops and on resistance are selected to reduce conduction losses, and short on and off times are selected to reduce switching losses.

Fig. 7.5 summarises the component ratings and loss models for the 1.2 kW CSI design. As mentioned earlier, six PV modules are connected in series to provide 1.2 kW of input power to the CSI. The DC link inductor model includes a parallel resistor, which represents core losses, and its copper loss resistance. The waveshaper (WS) MOSFET, fast recovery diode and SCR device information ratings and loss models are also provided in the figure. The low-pass output filter is shown after the unfolding circuit. In the figure, the resistance of the filter inductor and damping resistor values are also presented. The grid is modelled a 240 V<sub>RMS</sub> voltage source.

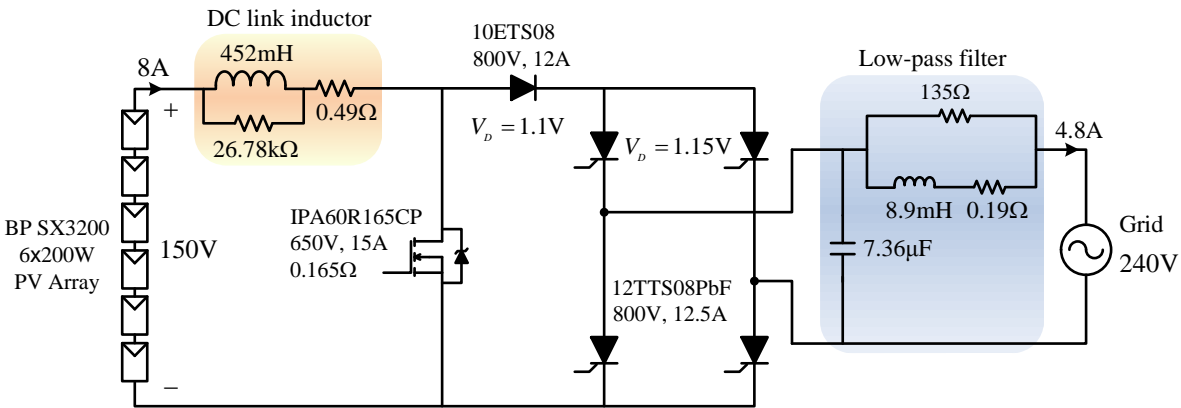


FIGURE 7.5: Proposed 1.2 kW inverter topology showing component ratings and loss models.

A high-voltage (650 V) MOSFET was chosen for the wave-shaper switch, though an IGBT would be a reasonable alternative.

Table 7.3 shows the summary of the components for the designed higher power 1.2 kW grid connected CSI. For the semiconductor components the table compares the calculated voltage and current values with the device maximum ratings. In the design study there is generally a safety margin of at least a factor of two.

TABLE 7.3: The designed higher power inverter component summary showing rated power and maximum ratings of the components.

Component	Calculated	Maximum Ratings
<b>1. Solar Array</b>	BP SX3200	
Rated Voltage	149 V	184 V
Rated Current	8 A	8.7 A
Rated Power	1188 W	1200 W
<b>2. DC Link Inductor</b>		
Rated Current	8 A	
Inductance	452 mH	-
Rated Energy Storage	14.5 mJ/W	
<b>3. Waveshaper Switch</b>	IPA60R165CP	
Peak Current	8.5 A	15 A
RMS Current	5.5 A	10.6 A
Peak Voltage	364 V	650 V
Switching Frequency	4 kHz	-
On Resistance	-	0.165 $\Omega$
<b>4. Diode</b>	10ETS08	
Peak Voltage	364 V	600 V
Peak Current	8.5 A	16 A
Average Current	4.2 A	10 A
<b>5. SCRs</b>	10TTS08PbF	
Peak Voltage	360 V	800 V
Average Current	4.21 A	6.5 A
<b>6. Output Filter</b>		
Rated Current	6.6 A	-
Cut-off Frequency	622 Hz	
<b>7. Grid Output</b>		
Rated Voltage	240 V	
Rated Current	6.6 A	-
Rated Power	1.1 kW	
Rated Frequency	50 Hz	

## 7.4 Low-Pass Filter Design

The low-pass line filter for the 1.2 kW inverter was designed using the procedure described in Chapter 5. A summary of the filter components is given in Table 7.4.

Filter configuration 3 was selected where the damping resistor is connected in parallel to the filter inductor. Though this configuration offers only a first-order attenuation rate



TABLE 7.4: Low-pass output filter component values and corresponding filter parameters for the proposed 1.2 kW grid-connected current-source inverter.

Component	Parameter
Inductance, $L$	8.9 mH
Capacitance, $C$	7.36 $\mu F$
Normalised capacitance, $C_n$	0.12 pu
Damping Resistance, $R_D$	135 $\Omega$
Quality Factor, $Q$	4
Resonant Frequency, $f_R$	622 Hz

beyond the resonant frequency, it can still meet the grid THD requirement and offers the lowest damping resistor power loss for low values of  $Q$ .

Although 4 kHz switching frequency, as the prototype unit was used, this could be increased to 10 or 15 kHz. The maximum value of normalised capacitance  $C_n$  of 0.12 pu was chosen that still met the leading power factor requirement of 0.95. A value of quality factor of 4 was chosen which is within the recommended range of 2 to 4. Finally a ratio of cut-off frequency to switching frequency of slightly over 0.15 was chosen using Fig. 5.3, which is a trade-off between the grid filter loss and the THD. This resulted in a cut-off frequency of around 620 Hz. Based on these selected values, the filter inductance, capacitance and resistance can be calculated, and are given in Table 7.4.

## 7.5 System Simulation

### 7.5.1 Simulation Procedure

It is desired to investigate the 1.2 kW inverter performance over a wide range of output powers by changing modulation index and irradiance. This was done by performing detailed simulation studies. The performance of the designed higher power CSI was analysed against Australian Standards [9] for THD and PF. The efficiency of the CSI is also another important performance indicator.

Two cases will be examined with simulations. These are

1. constant irradiance: the output power will be changed by adjusting the modulation index as seen in Fig. 4.7(a).
2. variable irradiance: for each irradiance level the CSI will operate at the MPP by altering the modulation index (see Fig. 4.7(b)).

In addition to these, for each case, open-loop (OL) and feedforward (FFD) operations of the CSI will be investigated.

### Simulation model

The 1.2 kW CSI design was also implemented in PSIM and the 4-diode model was used to model the PV array (see Fig. 7.6). The DC link inductor model includes both copper and iron loss (see Fig. 7.5). Both the PV array and DC link inductor are implemented in the simulation as subcircuits. Then the WS circuit, the UC, the low-pass filter and the grid as a voltage source (50 Hz 240 V<sub>RMS</sub>) are connected respectively as seen in Fig. 7.6.

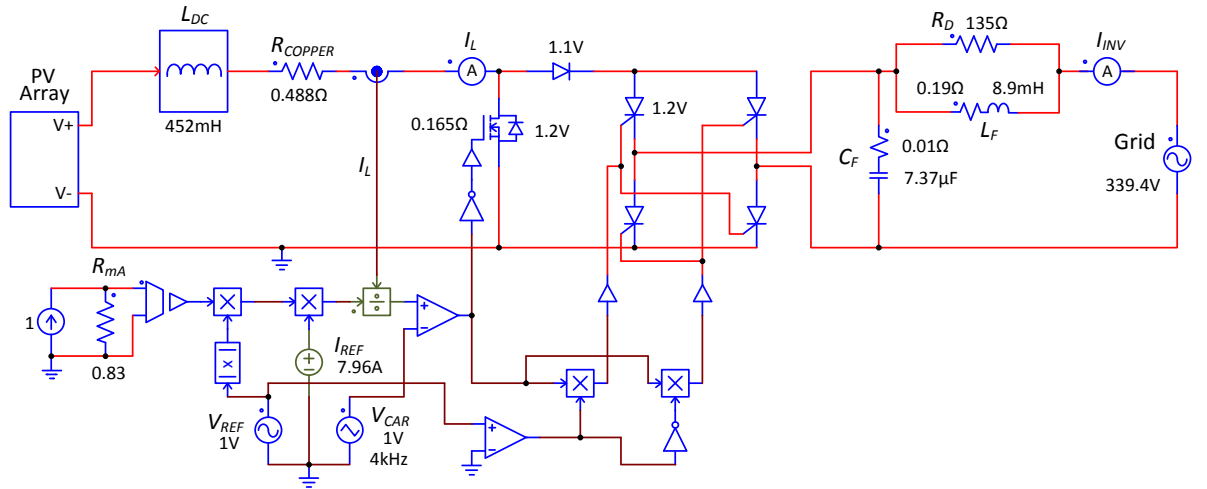


FIGURE 7.6: PSIM simulation model of the 1.2 kW CSI using FFD control.

Table 7.5 shows the simulation parameters of the inverter design. The total simulation time was selected as 3.3 seconds to allow the inductor current to reach steady-state. Only the last 0.45 of this period is recorded. As in the previous chapter, the time step was chosen to be relatively small for accurate simulation results.

As it was demonstrated earlier in the thesis, the advantage of the proposed grid-connected inverter design is that the SCRs in the circuit commute naturally due to the nature of

TABLE 7.5: Simulation model parameters of the designed higher power CSI.

Parameters	Values
PWM switching frequency	4 kHz
Total simulation time	3.3 s
Recorded simulation time	0.4 s
Time step	3 $\mu$ s

the waveshaper output current, i.e. the current sufficiently falls below the SCR holding current.

## 7.5.2 Voltage and Current Waveforms

### Constant Irradiance

The simulated voltage and current waveforms of the CSI are shown in Fig. 7.7. The CSI grid output voltage waveform and the current waveforms for four output power levels obtained by changing the modulation index are provided in Fig. 7.7(a). It was observed that the output current waveforms with OL control are similar to those with FFD control. The only difference is that the FFD compensated currents appear to be more sinusoidal. There is also a phase shift which is inversely related to the output current amplitude due to the capacitor in the low-pass filter circuit. The phase advance ( $\alpha$ ), as mentioned in Chapter 5, is not used in the simulations as it does not produce significant THD differences in the output current.

The amplitude of the 4 kHz PWM switching current ripple varies with the output current amplitude for the variable modulation index case. The highest and the lowest currents in Fig. 7.7(a) have lower ripple compared to intermediate value of current. The peak to peak ripple for the highest current is 0.29 A which corresponds to 4% (peak to peak ripple / current amplitude) PWM switching ripple. However for 0.8 kW and 0.5 kW, the percentage is 11 and 15% respectively. Even though the PWM ripple is smaller at the lowest power level of 0.2 kW, it has the ratio of 16% (0.25 A/1.53 A) which is slightly higher compared with middle power levels. This non-linear relationship between modulation index and PWM switching effect can be seen clearly in Fig. 7.8.

### Variable Irradiance

The current-source inverter voltage and current waveforms for the variable irradiance

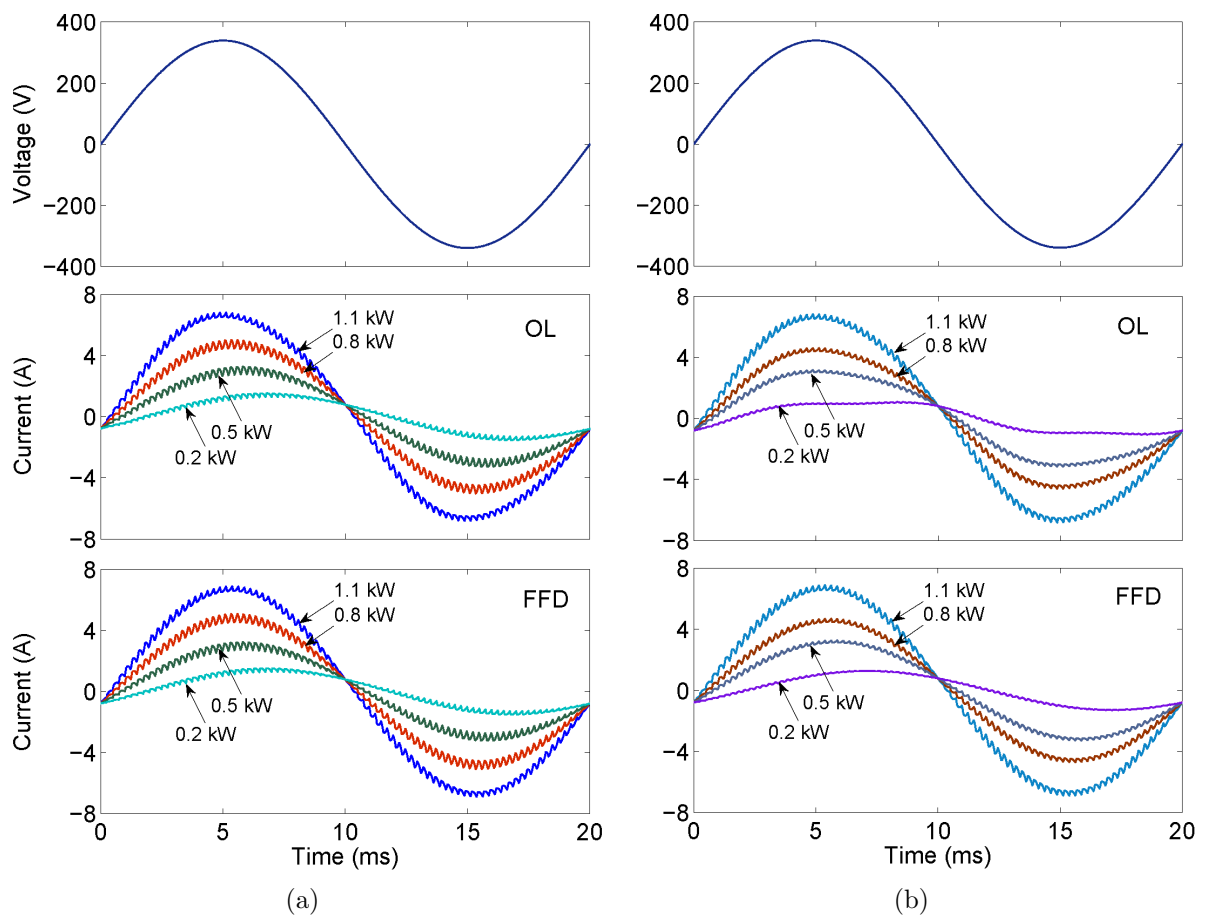


FIGURE 7.7: Simulated CSI output voltage and current waveforms for the two control approaches by varying (a) modulation index (b) irradiance.

case are shown in Fig. 7.7(b). In the OL mode, there is considerably more distortion at low output powers compared to the variable modulation index case.

Under variable irradiance operation, the modulation index is kept relatively constant and the PV array current varies. As was discussed in Chapter 4, inductor energy storage is proportional to square of the PV current and so the ratio of energy storage to output power drops at low values of output power causing the observed output current distortion. The FFD control compensates for the 100 Hz ripple effect on the current and so removes this distortion is shown in Fig. 7.7(b). This effect was seen earlier in Chapter 5 (Table 5.3).

It is interesting to note that the PWM current ripple magnitude is proportional to the fundamental current magnitude under variable irradiance operation. This is likely to be due to the nearly constant value of modulation index.

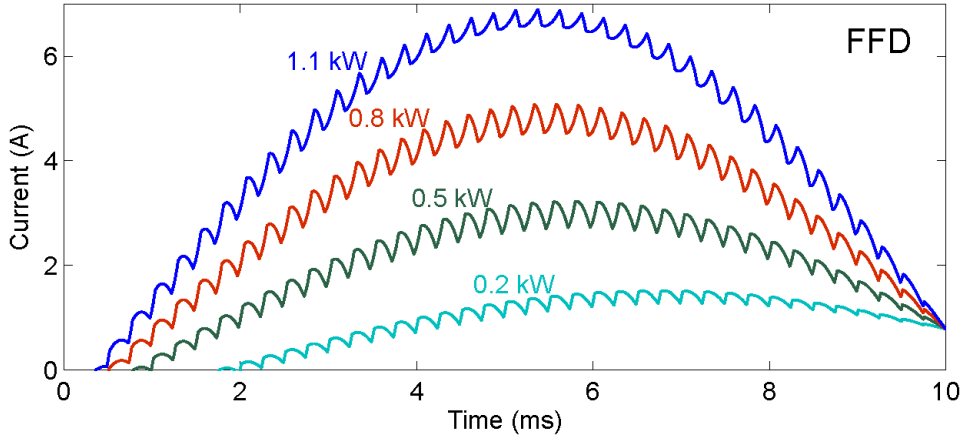


FIGURE 7.8: Simulated 4 kHz PWM switching effect on the several inverter output current waveforms as a function of  $m_A$  in FFD mode. This figure is the enlarged version of Fig. 7.7(a).

### 7.5.3 Total Harmonic Distortion

The CSI output current THD versus power curve is shown in Fig. 7.9(a) for changing modulation index with constant irradiance. Both the OL and FFD control methods present similar results except near the rated output power. It is near the rated output power that the 100 Hz PV input current ripple increases substantially. Under OL control, this produces significant 3<sup>rd</sup> harmonic distortion of the output current. Also under OL control, as the modulation index is increased beyond the maximum power point, the output power falls and the THD increases substantially. The FFD compensation control attenuates the 3<sup>rd</sup> order harmonic in the CSI output current significantly. The FFT spectrum comparison can be seen in Fig. 7.9(c). The THD at rated output is 4.28% for the OL control and 2.78% for the FFD control mode. There is thus a 1.5% improvement which is similar to what is shown previously in Table 5.3.

As expected from the previous section, there is a considerable difference between the OL and FFD control modes in relation to the THD for variable irradiance operation which is shown in Fig. 7.9(b). The values of THD for both control modes at rated output power is the same as for the variable modulation index case. For the OL case the THD increases considerably as the output power is reduced and reaches a peak of about 17% at 0.2 kW output power. For the FFD case, the THD drops with reducing output power.

Fig. 7.9(c) compares the FFT spectrum of the OL and FFD control modes showing the fundamental, 3<sup>rd</sup> and 5<sup>th</sup> harmonics at nominal  $m_A$  (83%) and nominal irradiance

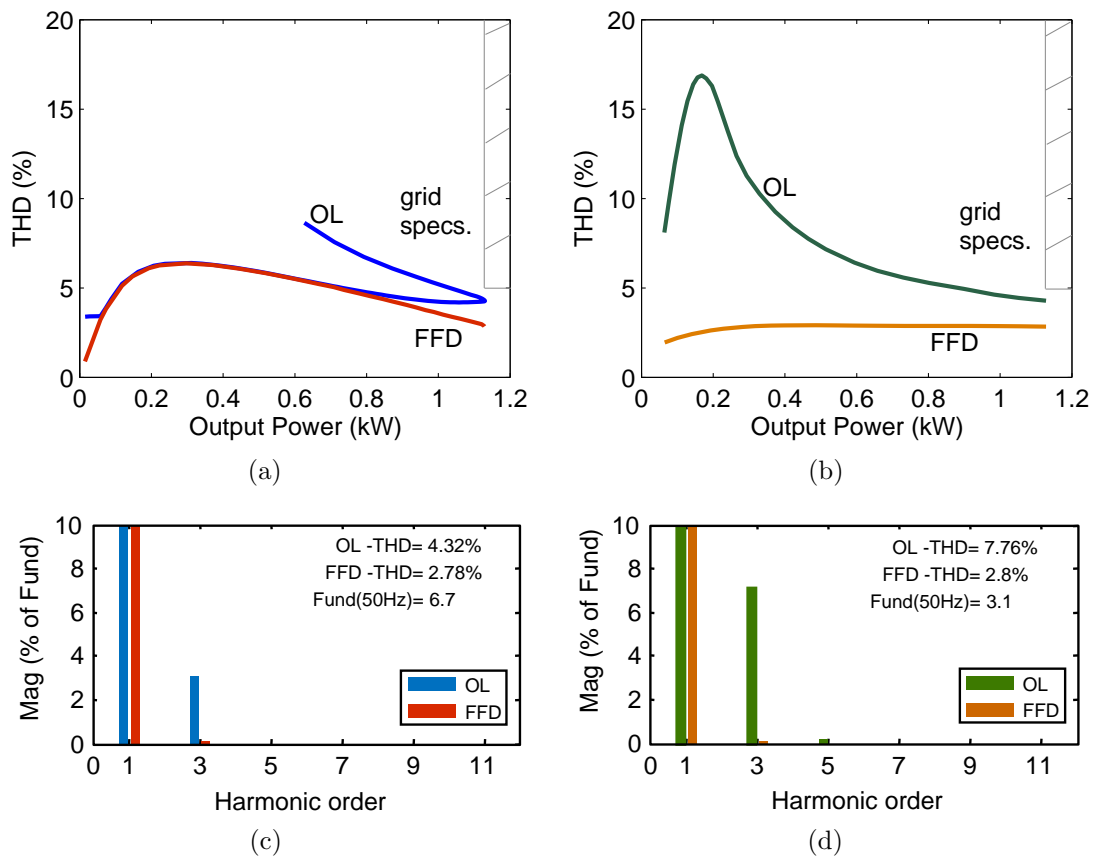


FIGURE 7.9: Simulated CSI total harmonic distortion as a function of output power for open-loop and feedforward control applications by varying (a) modulation index, (b) irradiance and the comparison the inverter output current FFT spectrums using the two control approaches with (c) 1 and (d)  $0.5 \text{ kW/m}^2$  irradiance values.

( $1 \text{ kW/m}^2$ ). As expected the 100 Hz fluctuation effect which corresponds to the 3<sup>rd</sup> harmonic reduces significantly in the FFD mode. Fig. 7.9(d) compares the OL and FFD modes for  $0.5 \text{ kW/m}^2$ . Due to lower energy storage capacity the CSI output current THD in the OL mode is relatively higher than FFD mode. The FFD control eliminates the 3<sup>rd</sup> harmonic regardless of the PV array output current ripple amplitude as seen in Fig. 7.9(b).

#### 7.5.4 Power Factor

Fig. 7.10 shows the power factor curves as a function of the CSI output power for the variable modulation index and variable irradiance cases using both OL and FFD control. Due to the capacitor in the grid low-pass filter, the power factor is zero at zero output power. The power factor rapidly increases with increasing output power and approaches

unity at rated output power. Both figures comply with the power factor requirements of the Australian Standards [9]. The power factor curves for the variable modulation index case are nearly identical however for variable irradiance case the power factor with OL control is slightly higher than that obtained using FFD control for low output powers in the range 0.2 to 0.4 kW. This is due to the larger PWM ripple amplitude at this power level (see Table 4.6).

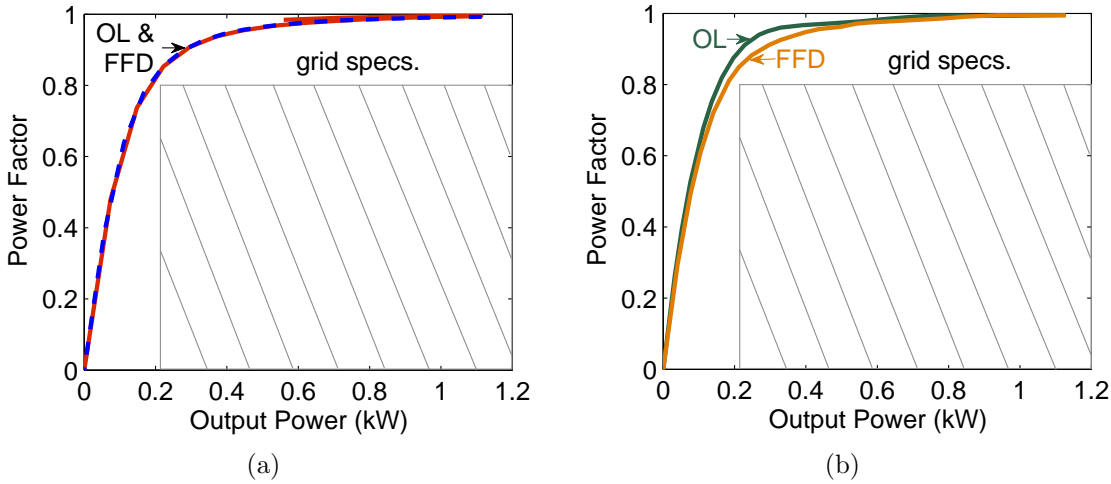


FIGURE 7.10: Simulated CSI power factor as a function of output power for (a) varying modulation and (b) varying irradiance cases.

### 7.5.5 Efficiency

The CSI efficiency, using OL and FFD control approaches with changing modulation index and irradiance cases are examined here. This efficiency includes the simulated power electronics, DC link inductor and grid output filter losses. A second efficiency value is discussed which also includes the PV array output power reduction due to the 100 Hz ripple, though this power reduction is not strictly a power loss.

The inverter efficiency is shown in Fig. 7.11(a), which shows the simulated efficiency as a function of inverter output power by changing modulation index with OL control. The efficiency is about 80% at 20% of rated output power and increases with increasing output power. The efficiency at rated output power is 95% which is 7% higher than that for the 160 W CSI prototype. The efficiency including the PV array power reduction is 94% at rated output power. The maximum efficiency is 97% at unity  $m_A$  however here

the CSI operates in the voltage-source region of the PV array and the output waveform is highly distorted. The FFD control version of the same curve is shown in Fig. 7.11(c). The efficiency obtained in this mode is similar to the OL mode.

The CSI efficiency for the variable irradiance case is given in Fig. 7.11(b) with OL control. At the rated output power the efficiency is the same as in the varying modulation index case. However with the variable irradiance case the efficiency increases slowly as the output power reduces. This is because the DC link inductor copper loss is a major loss component, and this loss is proportional to the square of the PV array current while the output power is proportional to the output current. Hence the losses decrease faster than the output power as the irradiance is decreased.

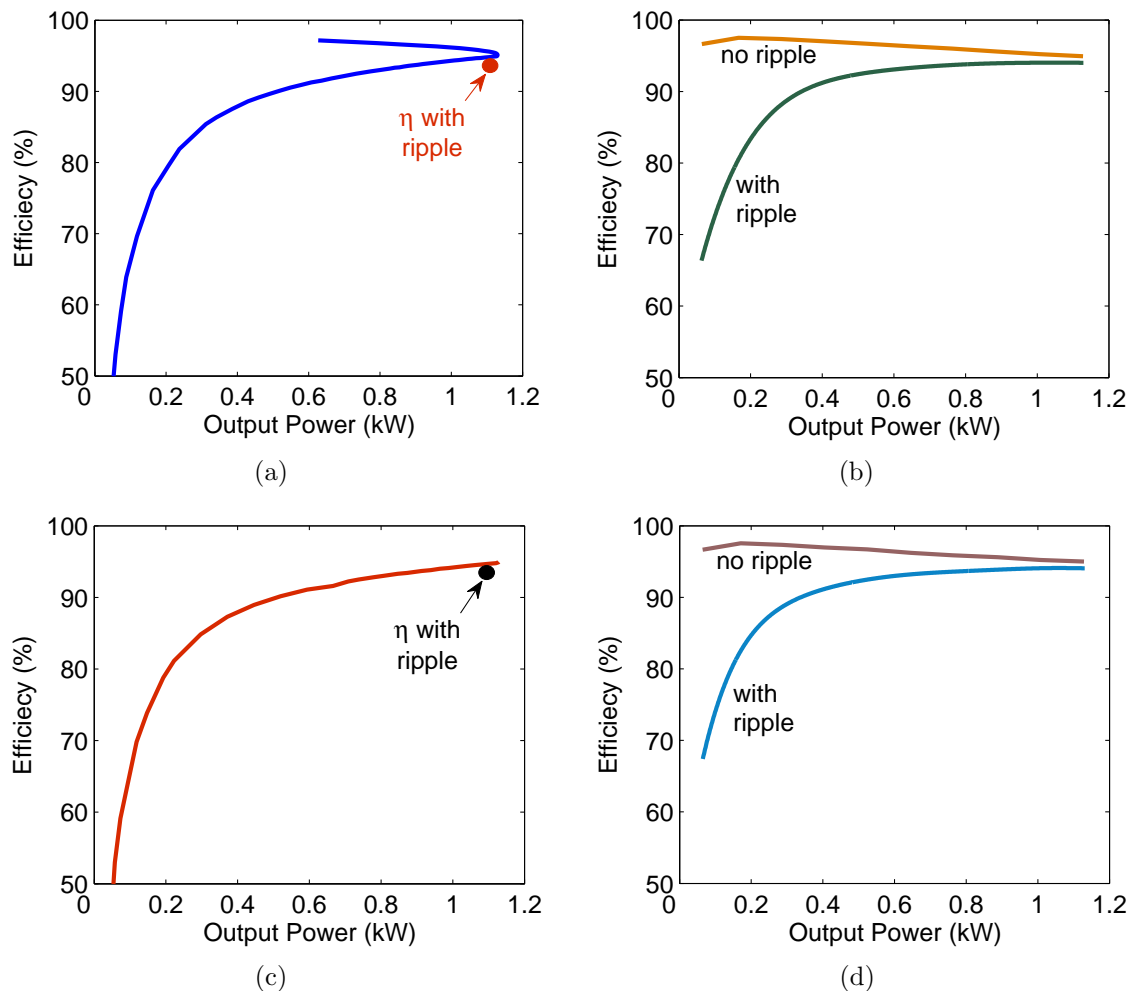


FIGURE 7.11: Simulated CSI efficiency as a function of output power using (a) OL control for variable modulation index, (b)  $G$  values and (c) FFD control for various  $m_A$  and d)  $G$  values. The efficiency with the 100 Hz PV array power reduction is indicated as a point for the constant irradiance case and curve for the changing irradiance case.



When the PV array ripple power reduction is included, the efficiency drops substantially at lower power levels. This is due to the increasing amplitude of the 100 Hz current ripple relative to the output current due to the reduced energy storage in the DC link inductor. The efficiency at 20% rated power is about 88% including this power reduction.

The FFD operation in Fig. 7.11(d) provides similar results to the OL operation of the CSI.

Table 7.6 gives the summary of the inverter power losses for each component including the required rated current and voltages.

TABLE 7.6: Simulated loss calculation summary at the rated output power.

Component	Parameter Value
<b>1. PV array</b>	
Ripple current	1.04 A (12.6%)
Ripple loss	15.4 W (1.3%)
<b>2. DC Link Inductor</b>	
RMS current	8.01 A
RMS voltage	23.7 V
Copper resistance	0.488 $\Omega$
Copper loss	31.6 W (2.5%)
Iron loss	2.34 W (0.19%)
<b>3. Waveshaper Switch</b>	
RMS current	5.52 A
MOSFET on resistance	0.165 $\Omega$
Conduction and switching losses	5.21 W (0.43%)
<b>4. Diode</b>	
Average current	4.21 A
Conduction loss	4.62 W (0.38%)
<b>5. SCRs</b>	
Average current	4.21 A
Conduction loss	10.9 W (0.9%)
<b>6. Output Filter</b>	
RMS current	4.72 A
Damping resistance	135 $\Omega$
Filter inductor resistance	0.19 $\Omega$
Filter loss	7.36 W (0.6%)
<b>Total Power Loss</b>	<b>76 W (6.3%)</b>

Fig. 7.12 illustrates the simulated inverter power loss breakdown as a function of output power. This shows the power loss of the various stages of the grid-connected inverter, including, the DC link inductor, MOSFET and diode (WS), the unfolding circuit (UC) and the output low-pass grid filter.

Fig. 7.12(a) illustrates the constant irradiance case with OL control. At zero output power the PV array current is at its maximum value and this current all flows through the MOSFET. Thus the DC link inductor and MOSFET power losses are at their maximum values. There is no output current and hence no loss in the diode, UC or grid filter. As the output power is increased, the PV array current decreases slightly causing the DC link inductor copper losses also to decrease slightly.

The MOSFET losses decrease more significantly as more of the input current is fed to the output. As the output current increases, the diode, UC and filter losses all increase proportionally. The power loss at rated output is about 61 W and is dominated by the DC link inductor losses.

Similar to Fig. 6.14(d) in Chapter 6 the power loss reduces rapidly with decreasing irradiance in the open loop case in in Fig. 7.12(b). This is because the PV array current reduces, hence reducing the copper loss in the DC link inductor and MOSFET. The unfolding circuit, diode and filter losses are roughly the same as in the variable modulation case shown in Fig. 7.12(a).

The loss breakdown for the constant irradiance case using the FFD control in Fig. 7.12(c) is very similar to Fig. 7.12(a). Likewise, the irradiance variation case for OL control in Fig. 7.12(b) and FFD control in Fig. 7.12(d) are also similar.

Fig. 7.12(e) is the same as Fig. 7.12(d) except it also shows the PV array 100 Hz ripple power reduction. The 100 Hz power reduction increases as the output power is reduced. The overall power loss at the rated output power is close to 70 W which represents a 6% power loss that corresponds to 94% overall efficiency.

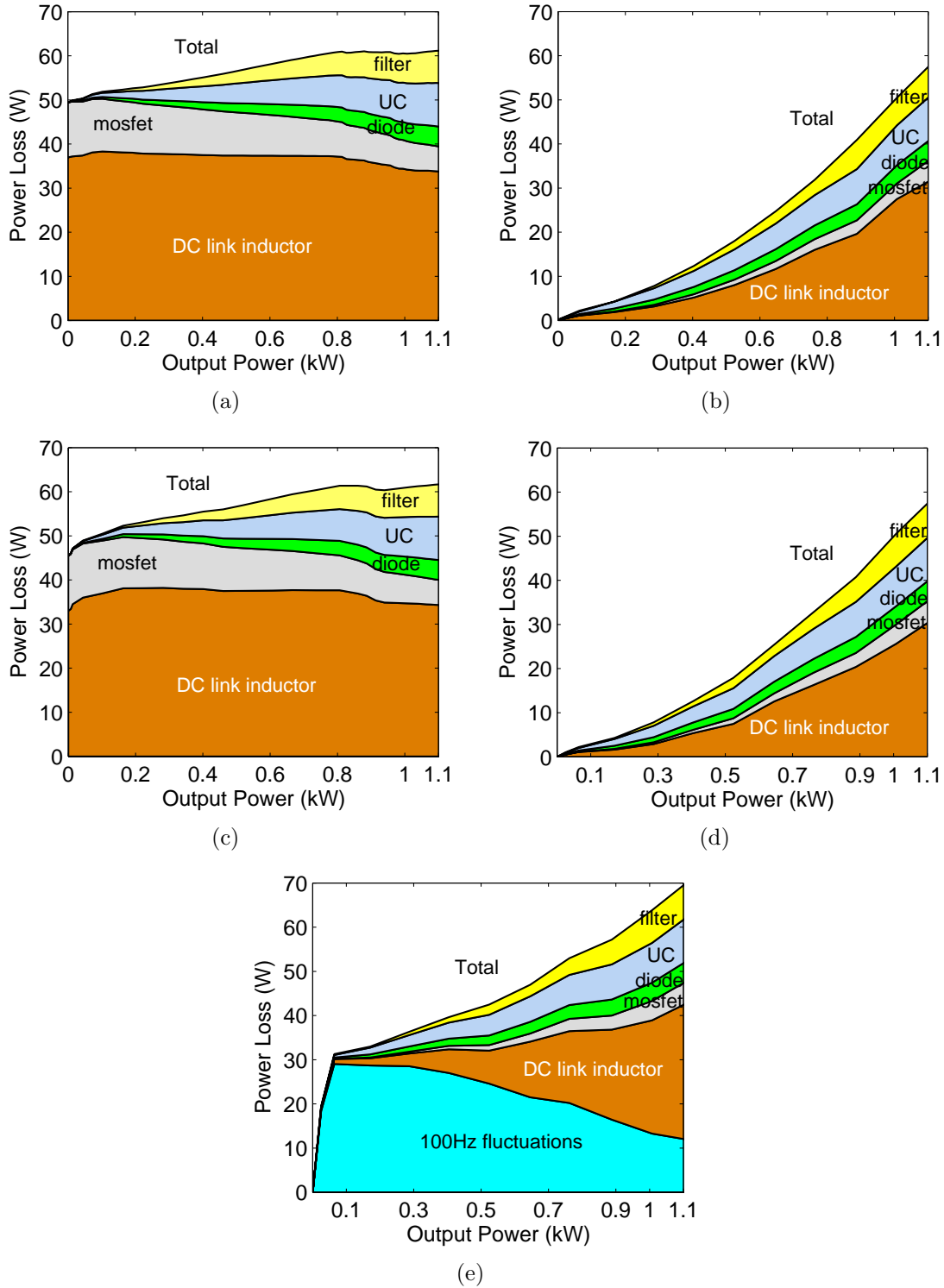


FIGURE 7.12: Designed higher power CSI loss breakdown as a function of output power for various (a)  $m_A$  using OL (b)  $G$  using OL (c)  $m_A$  using FFD (d)  $G$  using FFD and (e)  $G$  using FFD control including 100 Hz power reduction.

The summarised power loss breakdown for the rated output is shown in Fig. 7.13. The 100 Hz power reduction and DC link inductor losses (copper and core) have the largest fraction of the losses at the MPP. This clearly shows how critical is the trade-off between the energy storage losses versus the power reduction. The UC has loss of 13% is much smaller compared to the 31% in the 160 W prototype CSI due to the higher system voltage. Similarly the diode power loss is reduced from 11% to 6% (see Fig. 6.15).

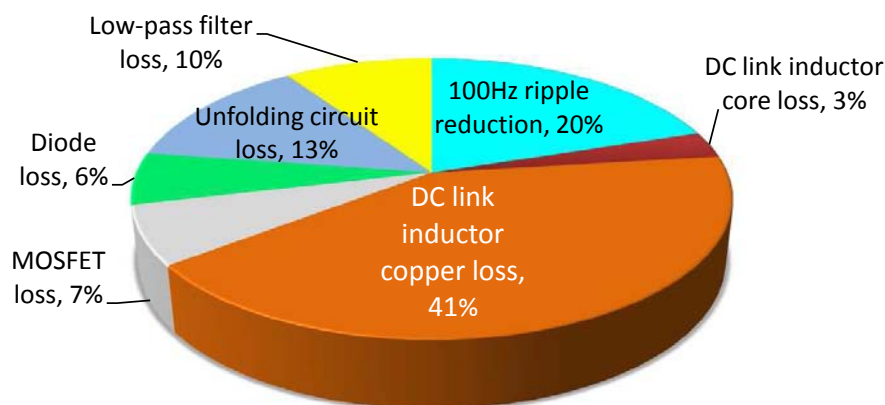


FIGURE 7.13: *Simulated loss pie chart of the designed grid-connected CSI for the rated output power.*

## 7.6 Summary

A 1.2 kW grid-connected inverter based on the proposed CSI topology was designed using the analysis performed in Chapter 4 and 5. The PV array output voltage was chosen to give a nominal modulation index of about 0.85 and the effects of inverter voltage drops on this was examined. The DC link inductor value was chosen to trade-off its copper losses versus the PV array power reduction at rated output power. The low pass filter was designed with a normalised capacitance of 0.12 pu, a quality factor of 4 and a resonant frequency of about 620 Hz.

Simulations were used to show that the inverter could meet the grid THD and power factor requirements when employing either open-loop or feedforward control for constant and variable irradiances.

The FFD control under variable irradiance operation provided the best THD (2.8%) which was constant over a wide range of inverter output power levels. The efficiency at

rated output of the 1.2 kW CSI was 95% which is 7% higher than that for the the 160 W prototype. The overall efficiency is approximately 1% less if the 100 Hz PV array ripple power reduction is taken into account. The DC link inductor copper loss has the biggest fraction of the overall power loss.

In conclusion, the performance of the proposed inverter topology improves significantly when scaled up to the 1.2 kW output power level. At this power level the inverter meets the grid THD and power factor requirements and has a significantly higher rated efficiency than the 160 W prototype.

---

---

# CHAPTER 8

---

## CONCLUSION

### 8.1 Background

This research investigated the analysis, design and performance of a novel single-phase low-cost current-source (CSI) photovoltaic grid-connected inverter topology. The inverter consisted of a DC link inductor and a single boost switch (based on switched-mode rectifier) which was modulated to produce a sinusoidally-varying unipolar output current. A line frequency commutated, thyristor-based H-bridge was then used to convert this to an AC output current and a capacitor-inductor output filter to remove the PWM switching component.

Firstly, alternative models for the PV array were examined and validated with measurements. The PV array power reduction as a function of the DC link energy storage due to the single-phase output power oscillations was analysed in detail. The fundamental performance of the proposed grid-connected CSI topology was examined using simulations to investigate the selection of the nominal modulation index and DC link energy storage and the ability to meet the power factor (PF) and total harmonic distortion (THD) grid requirements. A feedforward control mode was implemented. The design of the low-pass

output filter was studied to show the trade-off between the output current THD, power loss, and quality factor.

A 160 W prototype unit was built and tested to verify the above simulation results using open-loop and feedforward compensation control. The real PV array operation was simulated using the dark I-V test arrangement. Finally a 1.2 kW grid-connected inverter based on the proposed topology was designed and simulated. The simulation results showed that the 1.2 kW system could meet the grid THD and power factor requirements with a rated efficiency of 95%.

## 8.2 Key Results

1. The modelling of a PV array is investigated including irradiance and temperature effects. The results of the non-linear (ideal diode) and four-diode (piece-wise linear) models are compared with the manufacturer's data and dark I-V test results. It was shown that the four-diode model can provide reasonable accuracy while offering fast calculations for computer simulations.
2. The PV array output power reduction as a function of DC link energy storage due to the single-phase power fluctuations is investigated for voltage-source and current-source inverters. It is found that the shape of the normalised PV performance curves and hence the power reduction is not sensitive to irradiance or temperature. The definition of "balanced" current (or voltage) ripple based on equal power reduction at the extreme values gives more realistic estimates of PV output power reduction than assuming the ripple is centred on the optimum value. For this balanced ripple definition, the average power reduction versus ripple magnitude is comparable for voltage and current ripple. The relationship between the amount of energy storage and the PV average power reduction is analysed.
3. A simplified model of the inverter (ignoring the effects of PWM switching and the output filter) is used to perform a fundamental analysis of the proposed topology. This was used to investigate : the appropriate ratio of the rated PV array output voltage to the peak grid voltage; the required ratio of the DC link energy storage to the output power; the effect of output power variation using both modulation index and irradiance changes; and the performance improvement with feedforward

control. It was determined that a modulation index of about 0.85 and DC link energy storage of 12 mJ/W under rated conditions is a good starting point. The varying irradiance case produced significantly larger values of THD at low values of output power than the varying modulation index case, but still could meet the Australian Standards.

4. The selection and optimisation of the grid output filter was examined to meet the grid THD and PF requirements. A capacitor-inductor filter with the damping resistor in parallel with the inductor was found to give the lowest losses. It was shown that a low-pass filter with a normalised capacitance of 0.12 pu, a quality factor of between 2 and 4 and cut-off (resonant) frequency which was about one-tenth of the switching frequency generally gave acceptable values of THD and power-factor while keeping the filter damping losses at a reasonable level.
5. The above modelling approach was validated using a series of tests on a 160 W prototype. A strong correlation between the simulations and the laboratory tests was obtained. It was shown that the prototype inverter could meet the grid power factor requirement over the required 20% to 100% of output power but that the THD of 8.1% at rated output power did not meet the 5% requirement. Using the feedforward control algorithm only reduced the THD by 1%. The higher than predicted THD is likely due to the output filter phase delays causing issues with the unfolding current switching. Some preliminary simulations were performed to investigate modifying the phase angle of the sinusoidal reference waveform used by the waveshaper and unfolding circuit and promising results were obtained. Finally a good correspondence was obtained by the simulated and predicted efficiency results.
6. A 1.2 kW grid-connected inverter was designed and simulation results were used to show it met the grid THD and power factor requirements. The FFD compensation control provides the best THD which is 2.8% over a wide range of the inverter power output levels. The simulated efficiency of the 1.2 kW CSI was 95% which is 7% higher than that for the 160 W prototype.



## 8.3 Future Work

1. Further investigation and modelling is required to better understand the high levels of THD in the prototype unit. This is thought to be due to phase angle differences between the grid voltage (which is used as the reference for the waveshaper and unfolding circuit), and the voltage at the output of the unfolding circuit.
2. The higher-power grid-connected inverter, including the optimised low-pass CL filter and feedforward controller should be constructed and tested to verify its operation. The inverter, combined with a suitable PV array and DC link inductor, should be tested for several irradiance levels, to confirm its performance.
3. Three-phase CSIs have the advantage that the required amount of DC link energy storage (and hence its losses) is dramatically reduced as the total instantaneous output power should now be ideally constant. This should substantially improve the efficiency of the inverter. Further research could be performed in designing and building a three-phase version of the proposed CSI topology.