Memristive Devices and Circuits for Computing, Memory, and Neuromorphic Applications

by

Omid Kavehei

B. Eng. (Computer Systems Engineering, Honours)
Arak Azad University, Iran, 2003

M. Eng. (Computer Architectures Engineering, Honours)
Shahid Beheshti University, Iran, 2005

Thesis submitted for the degree of

Doctor of Philosophy

in

School of Electrical & Electronic Engineering
Faculty of Engineering, Computer & Mathematical Sciences
The University of Adelaide, Australia

December, 2011

Supervisors:

Dr Said Al-Sarawi, School of Electrical & Electronic Engineering

Prof Derek Abbott, School of Electrical & Electronic Engineering

CENTRE FOR HIGH
PERFORMANCE INTEGRATED
TECHNOLOGIES AND SYSTEMS

THE UNIVERSITY
of ADELAIDE

SUB CRUCE LUMEN

Contents

Contents

Contents

Abstract

A memristor, *memory resistor*, is a two-terminal nanodevice that can be made as thin as a single-atom-thick that has become of tremendous interest for its potential to revolutionise electronics, computing, computer architectures, and neuromorphic engineering. This thesis encompasses two major parts containing original contributions, (**Part I**) modelling and fabrication, and (**Part II**) circuit application and computing. Each part contains three chapters. The fundamentals necessary for understanding the main idea of each chapter are provided therein. A background chapter revolving around memristors and memristive devices is given. A system overview links the two parts together. A brief description of the two parts is as follows:

Part I—modelling and fabrication is relevant to modelling and fabrication of memristors. A basic modelling approach following the early modelling by Hewlett-Packard is presented and tested with several simple circuits. Memristor fabrication process and materials are discussed and two different fabrication runs along with initial measurement results are presented. SPICE modelling for two memristive devices, (i) the memristor and (ii) the complementary resistive switch are also provided.

Part II—nanocrossbar array and memristive-based memory and computing provides an analytical approach for crossbar arrays based on memristive devices. Proposed designs for memristor-based content addressable memories and their analysis are given. This part provides a binary/ternary content addressable memory structure based on a new complementary resistive switch. A number of fundamental building blocks for analogue and digital computing are also presented in this section. The observation of implementing a learning process based on a pair of spikes is also shown and an extension of such a process to a relatively large scale structure based on SPICE simulation is reported.

In addition to these original contributions, the thesis offers an introductory background on memristors, in the area of materials and applications. The thesis also provides a system overview of the targeted system (a CMOS-memristor imager system),

which provides a the link between the two parts of the thesis. In addition to the original contributions in the area of modelling and characterisation, an overview on the understanding of the memristor element via the quasistatic expansion of Maxwell's equations is discussed.

Statement of Originality

This work contains no material that has been accepted for the award of any other degree or diploma in any university or other tertiary institution to Omid Kavehei and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

I give consent to this copy of the thesis, when deposited in the University Library, being available for loan, photocopying, and dissemination through the library digital thesis collection, subject to the provisions of the Copyright Act 1968.

I also give permission for the digital version of my thesis to be made available on the web, via the Universitys digital research repository, the Library catalogue, the Australasian Digital Thesis Program (ADTP) and also through web search engines, unless permission has been granted by the University to restrict access for a period of time.

December 28, 2011

_____   _____
Signed   Date

Acknowledgements

The research presented in this thesis has been carried out in the School of Electrical and Electronic Engineering at the University of Adelaide. The path towards this thesis spans three years of a multidisciplinary research covering nanoelectronics, materials engineering, and circuit design. It has been an honour and great privilege to be the first Ph.D. student on the emerging topic of memristive devices and systems in Australia at a university with a solid and strong background in microelectronics. From the outset, many people have been involved and have contributed to the presented ideas and understanding gained. I gratefully acknowledge those who have helped along the way and influenced the formation of the understanding and the approach to representation of materials presented in this thesis.

First and foremost I would like to express my gratitude to my principle supervisor, Dr Said Al-Sarawi. He greatly helped with his open and respectful attitude toward science and technology. He provided me with his quick, thoughtful, effective, and also critical comments upon the drafts. I would like to gratefully acknowledge enthusiastic supervision and encouraging attitude of my co-supervisor, Prof Derek Abbott, who inspired me with his wide range of interests and unconventional thinking, which most of the time turn 'impossible' to be feasible. I appreciate all their contributions, time, ideas, strict requirements, funding, and answering quickly all questions I had about topics of their expertise to make my Ph.D. experience productive and stimulating.

Another key person whom I am strongly indebted to is Prof Kamran Eshraghian. He has been a great influential mentor to my scientific career throughout the past three years. His way of thinking inspires me to approach problems in different ways. I wish to express my deep gratitude for his continued encouragement and invaluable suggestions during this work. He provided me with direction, technical support and became more of a mentor and friend, than an advisor. I would also like to include my gratitude to Profs Kyoungrok Cho, Younggap You, Yeong-Seuk Kim, and Sung-Jin Kim, at Chungbuk National University, Cheongju, South Korea, who have enabled part of this research work together with Prof Eshraghian.

Acknowledgements

I wish to express my warm and sincere thanks to Drs Sharath Sriram, Madhu Bhaskaran, and Prof Arnan Mitchell at the Functional Materials and Microsystems Research Group at RMIT University, Melbourne, Australia, for their fabrication support and thoughtful discussions.

I am indebted to Drs Azhar Iqbal and Nicolangelo Iannella, outstanding scholars at the University of Adelaide, for their kindness, passionate, and patience in discussing long hours around different research issues and also their critical suggestions. I also benefited by works of Drs Azhar Iqbal and James M. Chappell on electromagnetic theory of the memristor. I owe to other great scholars at the university, including Prof Reg Coutts, Assoc Profs Christophe Fumeaux, Cheng Chew Lim, and Drs Withawat Withayachumnankul, Yingbo Zhu, Akhilesh Verma, Thomas Kaufmann, Andrew Allison, Shaghik Atakaramians, Gretel M. Png, and Ajay Tikka for their useful scientific and technical discussions. Drs Jegathisvaran 'Jega' Balakrishnan, Don Wenura Dissanayake and Mr Muammar Kabir also provided me with their Ph.D. thesis LaTeX style files, which has tremendously helped me in preparing this dissertation. I would like to, again, thank Mr Muammar Kabir for his tremendous help for assisting for printing of this thesis while I was in Melbourne.

I also acknowledge help and support Prof Sung Mo Kang and Dr Sangho Shin at the University of California, Merced, through answering questions and providing valuable comments on several topics related to memristive devices. I also acknowledge Profs Yael Nemirovsky and Amine Bermak help and openness in answering my questions regarding image sensors.

Looking back at my *alma mater*, I am surprised and at the same time very grateful for all I have achieved. I can by no means thank Assoc Prof Keivan Navi enough for all the hope he has put on me, before I thought I could do any research at all. It has certainly shaped me as researcher and has led me where I am now. Other scholars who contributed to my academic background are Drs Omid Hashemipour, Tooraj Nikoubin, Ali Zaker-Alhosseini, Islam Nazemi, Mohammad Eshghi, Mohammad Javad Sharifi, Namdar Saniei, Ramak Ghavami Zadeh, Farshad Safaei, Ali Jahanian, Ali Movaghar Rahimabadi, Mohammad Taghi Manzuri Shalmani, Somayeh Timarchi, Ebrahim Afjei, and Fereidoon Shams.

Acknowledgements

My endless appreciation goes to my family, my mother, my father, and my brothers, who always endow me with infinite support, wishes, continuous love, encouragement, and patience. I would like to thank my mother- and father-in-law for their guidances and wishes.

Last but not least, the warmest thank to my dear wife, *Taraneh*. I dedicate this dissertation to her not just because she has given up so much to make my career a priority in our lives, but for being a truly wonderful friend during the entire amazing journey with me.

O. Kavehei

Conventions

Typesetting This thesis is typeset using the LaTeX2e software. TeXnicCenter is used as an effective interface to LaTeX.

Referencing The Harvard style is used for referencing and citation in this thesis.

Spelling Australian English spelling is adopted, as defined by the Macquarie English Dictionary (Delbridge 2001).

System of units The units comply with the international system of units recommended in an Australian Standard: AS ISO 1000—1998 (Standards Australia Committee ME/71, Quantities, Units and Conversions 1998).

Physical constants The physical constants comply with a recommendation by the Committee on Data for Science and Technology: CODATA (Mohr and Taylor 2005).

Publications

Journal publications

KAVEHEI-O., AL-SARAWI-S.F., CHO-K.R., ESHRAGHIAN-K., AND ABBOTT-D. (2011). An analytical approach for memristive nanoarchitectures, *IEEE Transactions on Nanotechnology*, (Accepted on 28th October, 2011), *arXiv preprint: 1106.2927.**

KAVEHEI-O., IQBAL-A., KIM-Y.S., ESHRAGHIAN-K., AL-SARAWI-S.F., AND ABBOTT-D. (2010). The fourth element: characteristics, modelling and electromagnetic theory of the memristor, *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Science*, **466**(2120), pp. 2175–2202.*

ESHRAGHIAN-K., CHO-K.R., **KAVEHEI-O.**, KANG-S.K., ABBOTT-D., AND KANG-S.M.S. (2011). Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **19**(8), pp. 1407–1417.*

ESHRAGHIAN-K., **KAVEHEI-O.**, CHO-K.R., CHAPPELL-J., IQBAL-A., AL-SARAWI-S.F., AND ABBOTT-D. (2012). Memristive device fundamentals and modeling: Applications to circuits and systems simulation, *Proceedings of the IEEE*, accepted.*

LEE-S., **KAVEHEI-O.** HONG-Y., CHO-T., YOU-Y., CHO-K.R., AND ESHRAGHIAN-K. (2007). 3-D system-on-system (SoS) biomedical-imaging architecture for health-care applications, *IEEE Transactions on Biomedical Circuits and Systems*, **4**(6), pp. 426–436.*

NAVI-K., **KAVEHEI-O.**, RUHOLAMINI-M., SAHAFI-A., MEHRABI-S., AND DADKHAHI-N. (2008). Low-power and high-performance 1-bit CMOS full-adder cell, *Journal of Computers*, **3**(2), pp. 48–54.

MOLAHOSSEINI-A.S., NAVI-K., DADKHAH-C., **KAVEHEI-O.** AND TIMARCHI-S. (2010). Efficient reverse converter designs for the new 4-moduli sets $\{2^n - 1, 2^n, 2^n + 1, 2^{2n+1} - 1\}$ and $\{2^n - 1, 2^n + 1, 2^{2n}, 2^{2n} + 1\}$ based on new CRTs, *IEEE Transactions on Circuits and Systems I: Regular Papers*, **57**(4), pp. 823–835.

NAVI-K., MAEEN-M., FOROUTAN-V., TIMARCHI-S., AND **KAVEHEI-O.** (2009). A novel low-power full-adder cell for low voltage, *Integration, the VLSI Journal*, **42**(4), pp. 457–467.

TIMARCHI-S., **KAVEHEI-O.** AND NAVI-K. (2008). Low power modulo $2^n + 1$ adder based on carry save diminished-one number system, *American Journal of Applied Sciences*, **5**(4), pp. 312–319.

NAVI-K., FOROUTAN-V., AZGHADI-M.R., MAEEN-M., EBRAHIMPOUR-M., KAVEH-M., AND **KAVEHEI-O.** (2009). A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter, *Microelectronics Journal*, **40**(10), pp. 1441–1448.

Publications

MOAIYERI-M.H., MIRZAEE-R.F., NAVI-K., NIKOUBIN-T., AND **KAVEHEI-O.** (2010). Novel direct designs for 3-input XOR function for low-power and high-speed applications, *International Journal of Electronics*, **97**(6), pp. 647–662.

NAVI-K., SAJEDI-H.H., MIRZAEE-R.F., MOAIYERI-M.H., JALALI-A., AND **KAVEHEI-O.** (2011). High-speed full adder based on minority function and bridge style for nanoscale, *Integration, the VLSI Journal*, **44**(3), pp. 155—162.

AZGHADI-M.R., **KAVEHEI-O.** AND NAVI-K. (2007). A novel design for quantum-dot cellular automata cells and full adders, *Journal of Applied Sciences*, **7**(22), pp. 3460–3468.

Conference publications

KAVEHEI-O., KIM-Y., IQBAL-A., ESHRAGHIAN-K., AL-SARAWI-S.F., AND ABBOTT-D. (2009). The fourth element: Insights into the memristor, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 921–927.*

KAVEHEI-O., CHO-K.R., LEE-S., KIM-S., AL-SARAWI-S.F., ABBOTT-D., AND ESHRAGHIAN-K. (2011). Fabrication and modeling of Ag/TiO$_2$/ITO memristor, *54$^{\text{th}}$ IEEE International Midwest Symposium on Circuits and Systems, MWSCAS*, pp. 1-4.*

KAVEHEI-O., AL-SARAWI-S.F., CHO-K.R., IANNELLA-N., KIM-S., ESHRAGHIAN-K., AND ABBOTT-D. (2011). Memristor-based synaptic networks and logical operations using in-situ computing, *International Conference Series on Intelligent Sensors, Sensor Networks and Information Processing, ISSNIP*, (Accepted on 26$^{\text{th}}$ September, 2011), *arXiv preprint: 1108.4182*.*

KAVEHEI-O., LEE-S., CHO-K.R., AL-SARAWI-S.F., ESHRAGHIAN-K., AND ABBOTT-D. (2011). Integrated Memristor-MOS (M^2) Smart Sensor for Basic Pattern Matching Applications, *International Conference on Advanced Electromaterials, ICAE*, (Accepted on 5$^{\text{th}}$ August, 2011).*

KAVEHEI-O., LEE-S., CHO-K.R., AL-SARAWI-S.F., AND ABBOTT-D. (2011). Analysis of Pulse-Frequency Modulation CMOS Image Sensors, *International Conference on Advanced Electromaterials, ICAE*, (Accepted on 5$^{\text{th}}$ August, 2011).*

KAVEHEI-O., AL-SARAWI-S.F., ABBOTT-D., AND NAVI-K. (2008). High-performance bridge-style full adder structure, *Proceedings of SPIE*, **7268**, pp. 72680D.

KAVEHEI-O., AZGHADI-M.R., NAVI-K., AND MIRBAHA-A.P. (2008). Design of robust and high-performance 1-bit CMOS Full Adder for nanometer design, *IEEE Computer Society Annual Symposium on VLSI, ISVLSI*, pp. 10–15.

KAVEHEI-O., NAVI-K., NIKOUBIN-T., AND ROUHOLAMINI-M. (2006). A novel DCVS tree reduction algorithm, *IEEE International Conference on Integrated Circuit Design and Technology, ICICDT*, pp. 1–7.

KAVEHEI-O., MIRBAHA-A.P., DADKHAHI-N., AND NAVI-K. (2006). Novel architecture for IEEE-754 standard, *IEEE Conference on Information and Communication Technologies, ICTTA*, **2**, pp. 2601–2606.

KAVEHEI-O., AL-SARAWI-S.F., AND ABBOTT-D. (2009). An automated approach for evaluating spatial correlation in mixed signal designs using synopsys HSpice, *Synopsys Users Group, SNUG Conference*, Singapore. *http://tinyurl.com/snugsing09*

ROUHOLAMINI-M., KAVEHEI-O., MIRBAHA-A.P., JASBI-S.J., AND NAVI-K. (2007). A new design for 7:2 compressors, *IEEE/ACS International Conference on Computer Systems and Applications*, pp. 474–478.

NAVI-K., KAVEHEI-O., ROUHOLAMINI-M., SAHAFI-A., AND MEHRABI-S. (2007). A novel CMOS full adder, *International Conference on VLSI Design, VLSID*, pp. 303–307.

Publications

TIMARCHI-S., NAVI-K., AND **KAVEHEI-O.** (2009). Maximally redundant high-radix signed-digit adder: new algorithm and implementation, *IEEE Computer Society Annual Symposium on VLSI, ISVLSI*, pp. 97–102.

MIRBAHA-A.P., **KAVEHEI-O.**, ASADI-P., AND NAVI-K. (2006). High-speed arithmetic algorithms for multiple-valued logics in mixed-mode, *IEEE Conference on Information and Communication Technologies, ICTTA*, **1**, pp. 1682–1687.

NAVI-K., **KAVEHEI-O.**, HELMI-M., AND MORAVEJI-R. (2006). Multiple-valued Interconnection Network, *IEEE Conference on Information and Communication Technologies, ICTTA*, **3**, pp. 3151–3155.

AZGHADI-M.R., **KAVEHEI-O.**, AL-SARAWI-S.F., IANNELLA-N., AND ABBOTT-D. (2011). Triplet-based spike-timing dependent plasticity in silicon, *The 21st Annual Conference of the Japanese Neural Network Society, JNNS*, P3-35.

AZGHADI-M.R., **KAVEHEI-O.**, AL-SARAWI-S.F., IANNELLA-N., AND ABBOTT-D. (2011). Novel VLSI Implementation for Triplet-based Spike-Timing Dependent Plasticity, *International Conference Series on Intelligent Sensors, Sensor Networks and Information Processing, ISSNIP*, (Accepted on 26th September, 2011).

Note: Articles with an asterisk (*) are directly relevant to this thesis.

List of Figures

List of Tables

Chapter 1

Introduction

THE memristor, *memory-resistor*, is a two-terminal nanodevice that can be made as thin as a single-atom-thick and has become of tremendous interest for its potential to revolutionise electronics, computing, computer architectures, and neuromorphic engineering. It is a relatively unexplored device in terms of modelling, applications, design methodologies, and underlying physics of its switching mechanism(s) between two or more stable states is yet to be understood. This novel technology roughly situated on the border between nanotechnology and electronics, so called *nanoelectronics*. The memristor's application in memory systems promises a useful implementation of an *universal memory*, which has the speed of static random access memories (SRAMs), cost benefits of dynamic RAMs (DRAMs), and non-volatility of flash memories. In a broader perspective, its capability of storing digital data and performing logic functions has potential to fundamentally change the current general purpose computing systems, which are mainly based on the von Neumann computer architecture. The recent advent of the memristor and memristive devices also endows researchers with promising access to a device that is able to mimic biological synaptic behaviour. Therefore, with these wide range of applications, engineering aspects of memristor devices, memristive-based circuits, and system design become significantly important. This introductory chapter offers a brief background of memristor and memristive devices, along with a thesis outline.

1.1   Definition of memristor

The first concept and realisation of a *memory resistor* device was proposed by Widrow (1960), which was named *memistor*. A memistor is a three-terminal device that subtracts currents feeding through its control and input terminals in its output node. A memistor's resistance, which is a variable resistance, is controlled and sensed using the control (DC current) and sensing (AC current) terminals. The significant difference between a transistor and a memistor is that the memistor's resistance is controlled not by instantaneous control current, but the time integral of this current, which is the total charge that has been passed through the device (Widrow 1960). The memistor's concept was never linked to the fundamentals of circuit theory, but introducing the memistor was a fundamental and influential breakthrough in realisation of a physical adaptive neuron. A solid state memistor was later realised by Thakoor *et al.* (1990).

Bi-stable resistance switching was observed four years after the Widrow (1960) paper. Gibbons and Beadle (1964) reported the observation of bi-stable resistive switching in nickel oxide (NiO). This is the first appearance of resistive random access memory (RRAM) in the literature, however, its fundamental link to circuit theory was still then unknown. Four years later, through electromagnetic theory, Fano *et al.* (1968) listed four fundamental circuit elements: resistor, capacitor, inductor, and an unknown element. Later, Chua (1971) published his seminal paper on the memristor's concept and its connection to his nonlinear circuit theory (Chua 1969). Traditionally there are only three fundamental passive circuit elements: capacitors, resistors, and inductors, discovered in 1745, 1827, and 1831, respectively. However, one can set up five different mathematical relations between the four fundamental circuit variables: electric current i, voltage V, electric charge q, and magnetic flux Φ. For *linear* elements, $f(V,i) = 0$, $f(V,q) = 0$ where $i = \frac{dq}{dt}$ ($q = CV$), and $f(i,\Phi) = 0$ where $V = \frac{d\Phi}{dt}$ ($\Phi = Li$), indicate linear resistors, capacitors, and inductors, respectively. Chua (1971) mathematically predicted that there is a solid-state device, which defines the missing relationship between four basic variables. Recall that a resistor establishes a relation between voltage and current, a capacitor establishes a charge-voltage relation, and an inductor realises a current-flux relationship, as illustrated in Figure 1.1. Chua (1971) proposed that there should be a fourth fundamental passive circuit element to set up a mathematical relationship between q ($\int_t i$) and Φ ($\int_t V$), which he named the *memristor*, a portmanteau of *memory* and *resistor*. He predicted that a class of memristors might be realisable in the form of a pure solid-state device without an internal power supply. Chua and Kang

(1976) extended the idea of the memristor to a much broader class of devices and systems that is called *memristive* devices and systems. Therefore, the memristor is special case of a memristive device. Chua (2003) later published one of the fundamental works on nanodevice modelling and he stated that the fundamental circuit elements are all a family of devices with essentially an infinite number of higher order members.

NOTE:
This figure is included on page 4 of the print copy of
the thesis held in the University of Adelaide Library.

Figure 1.1. The 4th fundamental circuit element. The four fundamental two-terminal circuit elements. There are six possible relationships between the four fundamental circuit variables, current (i), voltage (V), charge (q), and magnetic flux (Φ). Out of these, five relationships are known, comprising $i = \frac{dq}{dt}$ and $v = \frac{d\Phi}{dt}$ and three circuit elements; resistor (R), capacitor (C), and inductor (L). Resistance is the rate of voltage change with current, inductance is the rate of flux change with current, capacitance is the rate of charge change with voltage. The only missing relationship is the rate of flux change with voltage (or vice-versa) that leads to the fourth element, the memristor. Adapted from Strukov *et al.* (2008).

In 2008, Strukov *et al.* (2008), at Hewlett-Packard (HP), announced the first physical realization of a memristor device based on a TiO_2 thin film doped with oxygen vacancies. The doping process entails removing the negatively charged oxygen atom from its substitutional site in TiO_2, which creates a positively charged oxygen vacancy. These vacancies are formed at the time of crystallisation. By applying an electric field, ions move in the direction of current flow. The nonlinearity that characterises a memristor implies that the charges which flows through a memristor, dynamically changes its internal state. The new location of the ions can be read out as a change in the resistance (state) of the material thus permitting the realisation of a new class of low power ultra-dense memories (*ITRS* 2009).

Ventra *et al.* (2009) extend the notion of memristor devices and memristive systems to capacitors and inductors. These elements are known as the *memcapacitor* and *meminductor* and the prefix *mem* in both stands for *memory*. Like a memristor, a memcapacitor's or a meminductor's properties depend on the state and history of the system. All of these elements are collectively called *memelements*. All of these memelements show pinched hysteretic loops in the two constitutive variables that define them: current-voltage for the memristor, charge-voltage for the memcapacitor, and current-flux for the meminductor. They have claimed that these devices are common at the nanoscale. Recently, Chua (2011) extended the memristive behaviour further to all resistance switching memories, which itself emphasises the importance of the HP's discovery.

1.2   Applications of memristor

There are many target applications for memristors, ranging from non-volatile memories to neuromorphic engineering. However, as Herbert Kroemer, a Nobel Laureate in Physics in 2000, stated (Kroemer 2001):

> *"The* **principal** *applications of any sufficiently new and innovative technology have always been – and will continue to be – applications* **created** *by that technology."*

These applications may benefit from today's memristor, but the best is still to come. It can be argued that the RRAM's application in neuromorphic engineering is actually a direct result of HP's discovery. Therefore, the already developed theoretical framework of the memristor helped in introducing a totally new application for RRAM technology that has been mainly developed for digital memory applications. Figure 1.2 illustrates an example of the applications that have been created for the already realised RRAM technology by the memristor.

The applications of memristors can be found in many fields, such as programmable logic, signal processing, neural networks, control systems, sensor networks, radio frequency (RF), reconfigurable electronics, tunable (nano-) antennas, early vision processing, edge detection, data encryption, chaotic circuits, neuro-fuzzy systems, and non-volatile memories, which is the most straightforward and developed application of
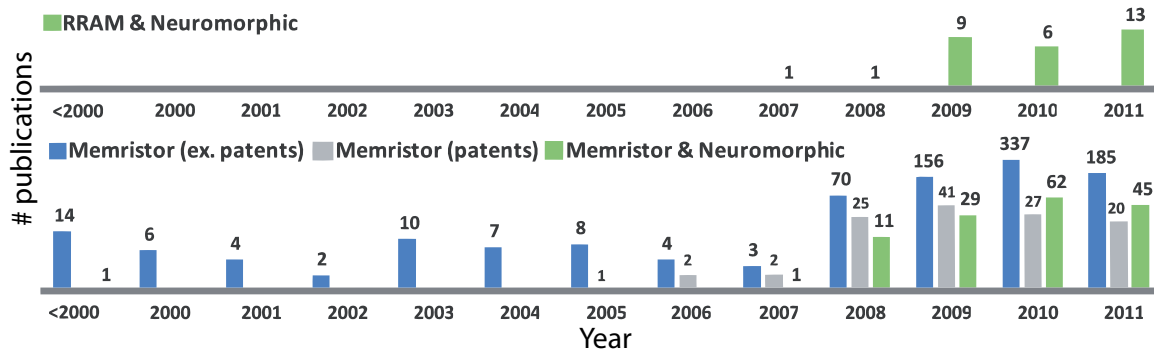
Figure 1.2. Number of publications with memristor as a keyword. Google scholar search results on the number of papers with the keywords: "memristor", "RRAM", and "neuromorphic". The top chart shows that the application of RRAM technology in neuromorphic engineering has been started since HP Labs identified the link between the solid-state realisation and the memristor's concept. Note that the length of each bar in the above figure is drawn logarithmically, however, the corresponding linear number of publications is indicated at the top of each bar.

memristive systems (Pershin and Di Ventra 2011, Kavehei *et al.* 2010, Snider *et al.* 2011, Versace and Chandler 2010, Williams 2008, Xue 2010, Kalinin *et al.* 2011, Seo *et al.* 2011, Park *et al.* 2011, Buscarino *et al.* 2011, Kim *et al.* 2011a, Ebong and Mazumder 2011b, Sacchetto *et al.* 2011, Jeltsema and Do andria Cerezo 2011, Georgiou *et al.* 2011, Gergel-Hackett *et al.* 2011, Rose *et al.* 2011, Krzysteczko *et al.* 2012). In addition, one of the ground shacking applications of memristors and memristive devices proposed by Borghetti *et al.* (2010), which is enabling 'stateful' logic via 'material implication'. This concept entirely opposes the conventional von Neumann computer architectures. One of the most significant problems of the current structure of computers is the growing gap between the speed of computing units (CPUs) and main memories (DRAMs) (Alted 2010). This fact resulted in multi-level cache memories appearing next to the processing or logic units to achieve tighter coupling between memory and logic. However, the gap is still growing due to the fact that the memory and logic entities are still naturally different and therefore they need a data bus to be connected together. This bus creates a bottleneck because of the mentioned speed difference.

The lesson from the last decade of experience tells us a tighter coupling between memory and logic and ideally eliminating the intermediate data buses will result in much lower power computing systems (Alted 2010). The memristor offers an extremely tight coupling between memory and logic owing to its in-situ computational characteristics, which promises an entirely new computer architecture (Kavehei *et al.*

2011b). The is-situ computing capability of memristor and memristive devices have been observed experimentally and have been already used in building logic gate (Borghetti *et al.* 2010, Kavehei *et al.* 2011b, Rosezin *et al.* 2011, Sun *et al.* 2011, Kavehei *et al.* 2011c, Kuekes *et al.* 2005, Kvatinsky *et al.* 2011, Kim *et al.* 2011c, Raja and Mourad 2009).

Since the emergence of the memristor technology, a variety of memristor-based applications have been reported. A more complete review is given in Chapter 2.

1.3   Prospects for memristors

Researchers in material, nanotechnology, and electronic groups worldwide have been working to improve memristor hardware, model, peripheral circuitries, and investigating its potential applications. The Semiconductor Industry Roadmap forecasts that the future of electronics beyond 2012 is going to be less certain (*ITRS 2009)*. Mouttet (2010) provides an informative overview on business perspectives of the RRAM technology. Table 1.1 shows the number of US patents held by major companies around the world on RRAM technology. These patents cover fabrication techniques, novel materials, and new designs. Considering this table and data from Figure 1.2 it is clear that computation, logic, and neuromorphic applications are all right at the beginning of development. At the same time, the table demonstrates great interest of industry for developing the technology. On August 31, 2010, HP announced that it signed a joint development agreement with Hynix Semiconductor Inc., to bring the memristor to market (Williams 2010). Hynix is a world-leading memory supplier. This agreement promises a possible memristor commercialisation by 2013.

Although, outcome of the HP-Hynix joint agreement will be very important for the development and commercialisation of memristor, it can be stated that the future success of the memristive electronics is likely to be independent from the success or the failure of any particular material used in resistive or phase change memories. According to Chua (2011), all resistive memory devices can be classified into a much broader class of memristive devices. This classification implies that even phase change memories (PCMs) can be classified as one branch of memristive technologies because their switching mechanism is also based on resistive switching. Therefore, such predication does not seem to be far from reality.

NOTE:
This table is included on page 8 of the print copy of
the thesis held in the University of Adelaide Library.

1.4   Thesis outline

This thesis encompasses two major parts, as outlined in Figure 1.3. The original contributions, included in (**Part I**) are modelling and fabrication, while **Part II** relates to circuit application and computing. Each part contains four independent chapters. The necessary fundamentals for understanding the main idea of each chapter are provided therein. A background chapter on memristors and memristive devices is given in Chapter 2, modelling and fabrications are discussed in Chapters 3, 5, and 4. A system overview, Chapter 6, linked the two parts together, and circuit application. Computing

architectures are discussed in Chapters 7, 8, and 9. Finally, Chapter 10 summaries the entire thesis. The detailed description for each part of the thesis is as follows:

Background, in Chapter 2, provides the background information on memristor from three aspects, definitions, technologies, and a historical review on applications. Fundamental and principle definitions of memristors, basic underlying switching mechanism, and variants of memelements are given in the first section of this chapter. The second section gives a survey on the emerging non-volatile memory technologies. The third section discusses applications and research activities in this field.

Part I—modelling and fabrication, Chapter 3, a very basic modelling approach following the early HP's modelling is presented and tested with several simple circuits. In Chapter 4, memristor fabrication process and materials are discussed and two different fabrications along with early measurement results are presented. Chapter 5 provides SPICE modelling for two memristive devices, (i) a memristor and (ii) a complementary resistive switch.

Appendix—memristor through electromagnetic theory provides further detail on understanding how the memristor element can be seen from the quasistatic expansion of Maxwell's equations and how this insight resulted in a clearer understanding of the memristor by exploiting a unified form of Maxwell's equations based on geometric algebra. These analysis was carried out in close collaboration with other members of the research group, Drs Azhar Iqbal and James Chappell.

System overview describes a targeted system. The system structure with focus on the two layers of memristive arrays and a CMOS image sensor are discussed. During the course of this thesis and for prototype testing purposes, two image sensors are fabricated. These two implementations are pulse-width modulated and pulse-frequency modulated sensors. These sensors are discussed in this chapter and a possible algorithm to be applied for image feature extraction as part of a pattern recognition system. The main focus of the thesis, regarding the system structure, is on the memristive array. The memristive array implements associative memories, which are discussed in Part II. Generic memristive-based logic operations for arithmetic operation can also be done through a dense memristive array, this concept is further discussed in Part II.

Part II—nanocrossbar array and memristive-based memory and computing

provides an analytical approach for crossbar arrays based on memristive devices in Chapter 7. Proposed designs for memristor-based content addressable memories and their analysis are given in Chapter 8. Chapter 7 also provides a binary/ternary content addressable memory structure based on complementary resistive switch. A few fundamental building blocks for analogue and digital computing are presented in Chapter 9. The observation of implementing a learning process based on a pair of spikes is also shown in Chapter 9 and the extension of such process to a relatively large scale structure based on SPICE simulation is reported.

Background	Chapter 1	Introduction
I Modelling	Chapter 2	Literature review and technologies
Fabrication	Chapter 3	Modelling fundamentals and memristor's characteristics
II Modelling	Chapter 4	Materials and memristor fabrication
System	Chapter 5	Memristor and memristive devices macro-modelling
Crossbar	Chapter 6	System overview
Circuit	Chapter 7	Crossbar architecture analysis
Computing	Chapter 8	Memristive-based accossiative memory
	Chapter 9	Memristive-based computing
	Chapter 10	Thesis summary

Part I covers Chapters 1–5. **Part II** covers Chapters 6–9.

Figure 1.3. Thesis outline. The thesis is composed of ten chapters in total, divided into two major parts, with four chapters in each part. The original contributions are distributed over these two parts.

1.5   Summary of original contributions

This thesis involves several original contributions in the field of memristive electronics, as declared in this section.

Memristors and memristive devices brought a broad range of applications especially in the field of electronic engineering. To enable electronic circuit designers providing a memristor model is the first step. A review on the memristor modelling using a SPICE macromodel are given in Chapters 3 and 5, respectively. For the first time a model for the complementary resistive device is developed and presented (Kavehei *et al.* 2010, Kavehei *et al.* 2011a). The model allows effective analysis of nanocrossbar arrays based on the complementary resistive switches. In another contribution, a unique metal-insulator-metal structure is fabricated and tested, which results in a memristive device with capability of analogue and digital computation (Kavehei *et al.* 2011d). The fabrication is followed by the modelling and characterisation steps that can be found in Chapter 5.

A comprehensive analytical approach for designing and modelling a nanocrossbar structure is also introduced (Kavehei *et al.* 2011a). This analysis helped in the design flow for implementing a memristive-based computing structures. These computing structures in their simplest form performs comparison. This form of operation is used to propose the first memristor-based content addressable memory (Eshraghian *et al.* 2011b) and also the first associative memory based on the complementary resistive switch (Kavehei *et al.* 2011c).

Another contribution is memristor-based digital computing (Kavehei *et al.* 2011b). This contribution provides a basis for an entirely different computer architecture. Furthermore, the ability of the fabricated memristor devices to mimicking the behaviour of a biological synapse is presented. Also for the first time, a demonstration of how the memristor is capable of implementing (additive) competitive Hebbian learning through SPICE simulations. A very basic analogue multiplication-and-accumulation module is also presented (Kavehei *et al.* 2011b).

In addition, this thesis demonstrates the design and fabrication of two CMOS image sensors based on pulse-width and pulse-frequency modulations, which are going to be used as part of the targeted system in combination with the memristive-based associative memory and logic (Lee *et al.* 2010).

1.5 Summary of original contributions

These original contributions serve to advance subdisciplines of memristive electronics, non-volatile memory design, associative memory, computer architecture, and neuromorphic engineering.

In the next chapter memristor and memristive devices and also characteristics of memcapacitor and meminductor are discussed. It also includes an overview on the emerging memory technologies and a comparison between them.

Chapter 2

Memristor and Memristive Devices

MEMRISTOR and memristive devices can be used in a wide range of applications. Since the first attempt for fabrication of a memristor device, a large number of research papers have been published and many ideas have been introduced. Therefore, this chapter aims to provide a timely review on memristor and memristive systems from the first theorisation to recent literature. This chapter also provides an overview and a discussion on emerging non-volatile memory technologies.

[This page has been left blank intentionally.]

2.1   Introduction

Memristor theory was formulated and named by Chua (1971) in his seminal paper on the memristor's concept and its connection to the nonlinear circuit theory (Chua 1969). Chua (1971) predicted that there is a solid-state device, which defines the missing relationship between four basic variables. In 2008, almost forty years later, a team at HP Labs announced the development of a switching memristor based on a thin-film of titanium dioxide (Strukov *et al.* 2008).

This chapter consists of four sections. Section 2.2 discusses memristor and memristive devices as well as a brief overview of a broader class of memelements—memristor, memcapacitor, and meminductor. A review of emerging memory technologies in general, and resistive random access memories in particular as well as a comparison between the state-of-the-art developments in this area are given in Section 2.3. Section 2.4 reviews the appearance of the memristor in literature since 1971 and discusses its characteristics.

2.2   Memristor and memristive devices

A resistor with memory is not a new concept. For example, a memristive device, by Choi *et al.* (2005), exploited a TiO_2 thin layer, and pre-dated the HP work. If taking the example of non-volatile memory, it dates back to 1960 when Bernard Widrow introduced a new circuit element named the *memistor* (Widrow 1960). The rationale for choosing the name 'memistor' is the same as the memristor, a resistor with memory. However, the memistor has three-terminals and its resistance is controlled by the time integral of a current signal, which implies that the resistance of the memistor is controlled by charge. Widrow (1960) devised the memistor as an electrolytic memory element to form a basic structure for a neural circuit architecture referred to as ADALINE (ADAptive LInear NEuron) (Widrow 1960). In the 1960s, Simmons (1963) published the very first report on the Metal-Insulator-Metal (MIM) *I-V* curve, illustrating the hysteresis effect associated with a MIM structure, that characterised tunnelling current behaviour. As we will later see, the physics of "small-scale" therefore, is the foundation for improved understanding of the dynamics of the memristor.

2.2.1 Memristive devices within Chua's periodic table

As part of the modelling process it is necessary to gain sufficient insight into the physical characteristics of the device in anticipation of developing better understanding of the underlying fundamental principle(s) that causes such a device to behave in particular manner.

In 2003, Chua (2003) introduced a 'periodic table' of the fundamental passive circuit elements. The table is based on differentials and integrals of the two basic circuit variables i and V, which can be extended to higher orders as desired. He contended that such a general catalogue of fundamental circuit elements will be required to correctly model molecular and nanodevices of the future. An interesting property of this periodic table, is that vertically it is cyclic with period four. We can see this intuitively, if using sinusoidal functions of time for q or V, in that after four differentials we return to the original function. Figure 2.1 presents an alternative simplified view of the periodic table.

2.2.2 Properties and fundamentals

If we display the memristor behaviour on an *I-V* graph, a hysteresis loop is obtained, as opposed to a 1:1 relationship between the variables produced by a Φ-q graph. Similar arguments regarding their memory behaviour and a unique link between two circuit variables, indicates that the meminductor and the memcapacitor can also be considered fundamental elements. Hence, it may be argued that the memristor begins a subclass of memristive systems (Chua and Kang 1976) based on the integrals of the appropriate circuit variables. Basically, as shown in Figure 2.1, $\int_t i$—$\int_t V$, $\int_t i$—$\int_t \Phi$, and $\int_t V$—$\int_t q$ relationships can be considered as second generation of circuit elements.

This resistance behaviour of memristors can be modelled using highly nonlinear $\sinh(\cdot)$ function as suggested by Strukov and Williams (2009a). Varghese and Gandhi (2009) proposed an amplifier using memristors that utilises the $\sinh(\cdot)$ behaviour. In Shin *et al.* (2009) such a structure was also introduced as an example of a memristive device. The main idea is to characterise a $\sinh(\cdot)$ function type circuit that can be used to linearise a $\tanh(\cdot)$ function type circuit behaviour, e.g. CMOS differential amplifier.

$$\alpha_e = -2 \qquad \int_t \Phi \quad \text{---} \quad \overset{L(q),L(\int_t\Phi)}{\text{---}} \quad C(\Phi),C(\int_t^q) \quad \text{---} \quad \int_t q \qquad \beta_e = -2$$

$$\alpha_e = -1 \quad \Phi = \int_t V \overset{R(q),\ R(\Phi)}{=\!=\!=\!=\!=\!=\!=\!=} q = \int_t i \qquad \beta_e = -1$$

$$R_N \qquad \mathbf{L} \qquad \mathbf{C} \qquad R_N^*$$

$$\alpha_e = 0 \qquad V \overset{\mathbf{R}}{=\!=\!=\!=\!=\!=\!=} \frac{dq}{dt} = i \qquad \beta_e = 0$$

$$L(V),\ L(\tfrac{dV}{dt}) \qquad C(i),\ C(\tfrac{dV}{dt})$$

$$\alpha_e = +1 \qquad \frac{dV}{dt} \overset{R(\tfrac{di}{dt}),\ R(\tfrac{dV}{dt})}{\text{---}} \frac{d^2q}{dt^2} = \frac{di}{dt} \quad \beta_e = +1$$
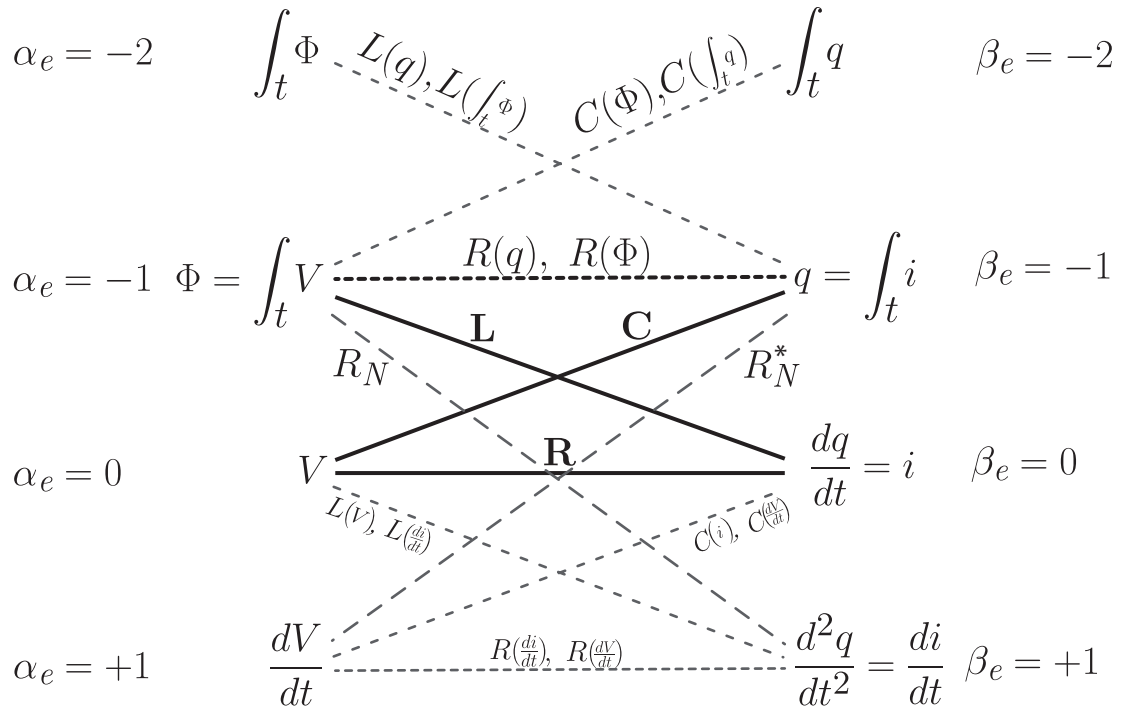
Figure 2.1. Periodic table of the fundamental passive circuit elements. Classification of circuit elements. The two circuit variables, current i and potential V are placed in a sequence of differentials as shown above. The three basic circuit elements C, L, and R are shown in **bold** and link the four circuit variables V, i, Φ, and q. The memristor ($R(q)$, $R(\Phi)$) links flux and charge. The meminductor and the memcapacitor also link the higher order integrals $\int_t \Phi$ and $\int_t q$ (Ventra *et al.* 2009). The α_e and β_e are used for element identification using Chua's periodic table of circuit elements from (Chua 2003). According to the periodic table, these are two types of negative resistances: R_N, directly proportional to frequency, whereas R_N^* has an inverse relationship.

A theoretical analysis, by Tavakoli and Sarpeshkar (2005), shows that a $\sinh(\cdot)$ function significantly reduces the third harmonic coefficient and as a consequence reduces the nonlinearity of the circuit.

Consequently, $\Phi = f_M(q)$ or $q = g_M(\Phi)$ defines a charge-controlled (flux-controlled) memristor. Then, $\frac{d\Phi}{dt} = \frac{df_M(q)}{dq}\frac{dq}{dt}$ or $\frac{dq}{dt} = \frac{dg_M(\Phi)}{d\Phi}\frac{d\Phi}{dt}$, which implies $V(t) = \frac{df_M(q)}{dq}i(t)$ or $i(t) = \frac{dg_M(\Phi)}{d\Phi}V(t)$, respectively. Note that, $M(q) = \frac{df_M(q)}{dq}$ for a charge-controlled memristor and $W(\Phi) = \frac{dg_M(\Phi)}{d\Phi}$ for a flux-controlled memristor, The units of $M(q)$ and $W(\Phi)$ are Ohms and Siemens (Chua 1971), respectively.

Memristance, $M(q)$, is the slope of the Φ-q curve, which for a simple case, is a piecewise Φ-q curve with two different slopes, giving two different values for $M(q)$ at a specified voltage. This property can be used to encode binary information. For detailed information regarding typical Φ-q curves, the reader is referred to Chua (1971).

It is also obvious that if $M(q) \geq 0$, then instantaneous power dissipated by a memristor, $p(i) = M(q)(i(t))^2$, is always positive so the memristor is a passive device. Thus the Φ-q curve is a monotonically-increasing function. This feature was observed in the HP version of the memristor device (Strukov *et al.* 2008). Some other properties of the memristor such as zero-crossing between current and voltage signals can be found in Chua (1971) and Chua and Kang (1976). The most important feature of a memristor is its pinched hysteresis loop *V-i* characteristic (Chua and Kang 1976). A very simple consequence of this property and $M(q) \geq 0$ is that such a device is purely dissipative like a resistor.

Another important property of a memristor is its excitation frequency. It has been shown that the pinched hysteresis loop shrinks when the excitation frequency increases (Chua and Kang 1976). In fact, when the frequency increases toward infinity, the memristor acts as a linear resistor (Chua and Kang 1976).

Five years after Chua (1971) paper on the memristor, him and his graduate student, Kang, published a paper defining a much broader class of systems, named *memristive systems*. From the memristive systems viewpoint, a generalised definition of a memristor is $V(t) = R(w)i(t)$, where w defines the internal state of the system and $\frac{dw}{dt} = f(w, i)$ (Chua and Kang 1976). Based on this definition a memristor is a special case of a memristive system.

The HP memristor (Strukov *et al.* 2008) can be defined in terms of memristive systems. It exploits a thin-film TiO_2 sandwiched between two platinum (Pt) contacts and one side of the TiO_2 is doped with oxygen vacancies, which are positively charged ions. Therefore, there is a TiO_2 junction where one side is doped and the other is undoped. Such a doping process results in two different resistances: one is a high resistance (undoped) and the other is a low resistance (doped). Hence, HP intentionally established a device that is illustrated in Figure 2.2. In conventional semiconductor devices doping is achieved by implantation of ions that are fixed in the lattice. But in the memristor there is an important difference, the memristor allows ionic drift so the width of the doped region is allowed to change with bias. The internal state variable, w, is also the

variable length of the doped region. Roughly speaking, when $w \to 0$ we have non-conductive channel and when $w \to L$ we have conductive channel. The HP memristor switching mechanism is further discussed in Yang *et al.* (2008).

> NOTE:
> This figure is included on page 19 of the print copy of
> the thesis held in the University of Adelaide Library.

Figure 2.2. A simple schematic for the memristor and illustrating memristive behaviour. Schematic of the HP memristor, where L is the device channel length and w is the length of doped region. The size of doped region is a function of the applied charge and is responsible for memristive effect as it changes the effective resistance of the device. Usually w is shown by its normalised counterpart, $x = w/L$ (Strukov *et al.* 2008).

Memristor device characteristics can be defined using a system of two equations,

$$\begin{cases} I = g(w,V) \cdot V \\ \frac{\mathrm{d}w}{\mathrm{d}t} = f(w,V) \, , \end{cases} \tag{2.1}$$

where w is a physical variable indicating the internal memristor state that in theory is such that $0 < w < L$. Here, L is the thickness of a thin-film metal-oxide (memristive) material sandwiched between two metallic electrodes, and I and V represent current through and voltage across the device, respectively. The $g(\cdot)$ function represents the memristor's conductance. The state variable can be expressed using a normalised form $x = 1 - w/L$. In this case, if $w \to 0$ or moving towards higher conductances. On the other hand, if $x \to 1$ and $w \to L$ or moving towards lower conductances then $x \to 0$. In this work, R_{HRS} represents high resistance state and R_{LRS} represents low resistance state. Eq. (2.1) shows that the output of the system (here I), at a given time, depends on w and V. State transition conditions are also explained by the function $f(\cdot)$. To measure this function several time-domain experiments for I and V are required (Pickett *et al.* 2009).

There are two other elements with memory named the *memcapacitor* (Memcapacitive, MC, Systems) and *meminductor* (Meminductive, MI, Systems). Ventra *et al.* (2009) postulated that these two elements also could be someday realised in device form. The main difference between these three elements, the memristor, memcapacitor, and

meminductor is that, the memristor is not a lossless memory device and dissipates energy as heat. However, at least in theory, the memcapacitor and meminductor are lossless devices because they do not have resistance. Ventra *et al.* (2009) also investigated some examples of using different nanoparticle-based thin-film materials. Memristors (Memresistive, MR, Systems) are identified by a hysteresis current-voltage characteristic, whereas MC and MI systems introduce Lissajous curves for charge-voltage and flux-current, respectively. Similar to memristors, there are two types of these elements, therefore, the three circuit elements with memory (mem-systems/elements[1]) can be summarised as follows,

Memristors (MR Systems): A memristor is a one-port element whose instantaneous electric charge and flux-linkage, denoted by q_{mr} and Φ_{mr}, respectively, satisfies the relation $F_{\mathrm{mr}}(q_{\mathrm{mr}}, \Phi_{\mathrm{mr}}) = 0$. It has been proven that these devices are passive elements (Strukov *et al.* 2008). As discussed, they cannot store energy, so $V_{\mathrm{mr}}(t) = 0$ whenever $i_{\mathrm{mr}}(t) = 0$ and there is a pinched hysteresis loop between current and voltage. Thus, charge-flux curve is a monotonically-increasing function. A memristor acts as a linear resistor when frequency goes toward infinity and as a nonlinear resistor at low frequencies. Due to the nonlinear resistance effect, $\frac{dV_{\mathrm{mr}}}{dt} = R(t)\frac{di_{\mathrm{mr}}}{dt} + i_{\mathrm{mr}}(t)\frac{dR}{dt}$ should be utilised instead of $\frac{dV_{\mathrm{mr}}}{dt} = R(t)\frac{di_{\mathrm{mr}}}{dt}$ (Kavehei *et al.* 2010). There are two types of control process:

I. nth order current-controlled MR systems [2], $q_{\mathrm{mr}} = \int i_{\mathrm{mr}}(\tau)\,d\tau$,

$$
\begin{aligned}
V_{\mathrm{mr}}(t) &= R(x, i_{\mathrm{mr}}, t) i_{\mathrm{mr}}(t)\,, \\
\dot{x} &= f_{\mathrm{icmr}}(x, i_{\mathrm{mr}}, t)\,.
\end{aligned}
$$

II. nth order voltage-controlled MR systems, $\Phi_{\mathrm{mr}} = \int V_{\mathrm{mr}}(\tau)\,d\tau$,

$$
\begin{aligned}
i_{\mathrm{mr}}(t) &= R^{-1}(x, V_{\mathrm{mr}}, t) V_{\mathrm{mr}}(t)\,, \\
\dot{x} &= f_{\mathrm{vcmr}}(x, V_{\mathrm{mr}}, t)\,.
\end{aligned}
$$

Memcapacitors (MC Systems): A memcapacitor is an one-port element whose instantaneous flux-linkage and time-integral of electric charge, denoted by

---

[1] Memristors, memcapacitors, meminductors, and the corresponding memsystems.

[2] Current- (and voltage-) controlled is a better definition for memristors because they do not store any charge (Oster 1974). Ventra *et al.* (2009) specified it as current- (and voltage-) controlled instead of charge- (and flux-) controlled in Chua (1971).

Φ_{mc} and σ_{mc}, respectively, satisfy the relation $F_{mc}(\Phi_{mc}, \sigma_{mc}) = 0$. The total added/removed energy to/from a voltage-controlled MC system, $U_{mc} = \int V_{mc}(\tau) i_{mc}(\tau) d\tau$, is equal to the linear summation of areas between q_{mc}-V_{mc} curve in the first and third quadrants with opposite signs. Due to the nonlinear capacitance effect, $\frac{dq_{mc}}{dt} = i_{mc}(t) = C(t)\frac{dV_{mc}}{dt} + V_{mc}(t)\frac{dC}{dt}$ should be utilised instead of $\frac{dq_{mc}}{dt} = C(t)\frac{dV_{mc}}{dt}$, so $U_{mc} = \int V_{mc} C \, dV_{mc} + \int V_{mc}^2 \, dC$. In principle a memcapacitor can be a passive, an active, and even a dissipative[3] element (Kavehei *et al.* 2010, Ventra *et al.* 2009). If $V_{mc}(t) = V_{mc0}\cos(2\pi\omega t)$ and capacitance is varying between two constant values, C_{ON} and C_{OFF}, then the memcapacitor is a passive element. It is also important to note that, assuming zero charged initial state for a passive memcapacitor, the amount of removed energy cannot exceed the amount of previously added energy. A memcapacitor acts as a linear capacitor when frequency approach infinity and as a nonlinear capacitor at low frequencies. There are two types of control process:

I. nth order voltage-controlled MC systems, $\Phi_{mc} = \int V_{mc}(\tau) d\tau$,

$$
\begin{aligned}
q_{mc}(t) &= C(x, V_{mc}, t) V_{mc}(t), \\
\dot{x} &= f_{vcmc}(x, V_{mc}, t).
\end{aligned}
$$

II. nth order charge-controlled MC systems, $\sigma_{mc} = \int q_{mc}(\tau) d\tau = \iint i_{mc}(\tau) d\tau$,

$$
\begin{aligned}
V_{mc}(t) &= C^{-1}(x, q_{mc}, t) q_{mc}(t), \\
\dot{x} &= f_{qcmc}(x, q_{mc}, t).
\end{aligned}
$$

Meminductors (ML Systems): A meminductor is a one-port element whose instantaneous electric charge and time-integral of flux-linkage, denoted by q_{ml} and ϱ_{ml}, respectively, satisfy the relation $F_{ml}(\varrho_{ml}, q_{ml}) = 0$. In the total stored energy equation in a ML system, $U_{ml} = \int V_{ml}(\tau) i_{ml}(\tau) d\tau$, the nonlinear inductive effect, $\frac{d\Phi_{ml}}{dt} = V_{ml}(t) = L(t)\frac{di_{ml}}{dt} + i_{ml}(t)\frac{dL}{dt}$ should be taken into account. Thus, $U_{ml} = \int i_{ml} L \, di_{ml} + \int i_{ml}^2 \, dL$. Similar to MC systems, in principle a ML system can be a passive, an active, or even a dissipative element and using the same approach, under some assumptions they behave like passive elements. There are two types of control process:

---

[3] Adding energy to system.

I. nth order current-controlled ML systems, $q_{\mathrm{ml}} = \int i_{\mathrm{ml}}(\tau)\,d\tau$,

$$\Phi_{\mathrm{ml}}(t) = L(x, i_{\mathrm{ml}}, t) i_{\mathrm{ml}}(t),$$
$$\dot{x} = f_{\mathrm{icml}}(x, i_{\mathrm{ml}}, t).$$

II. nth order flux-controlled ML systems, $\varrho_{\mathrm{ml}} = \int \Phi_{\mathrm{ml}}(\tau)\,d\tau = \int\int V_{\mathrm{ml}}(\tau)\,d\tau$,

$$i_{\mathrm{ml}}(t) = L^{-1}(x, \Phi_{\mathrm{ml}}, t) \Phi_{\mathrm{ml}}(t),$$
$$\dot{x} = f_{\mathrm{fcml}}(x, \Phi_{\mathrm{ml}}, t).$$

The reader is referred to Appendix A for further detail on understanding how the 4$^{\text{th}}$ fundamental element can be seen from the quasistatic expansion of Maxwell's equations. For the first time, our group showed how this insight can be gained by exploiting a unified-form of Maxwell's equations based on Geometric Algebra (GA).

2.3   Emerging non-volatile memory technologies

Scaling of the traditional memory technologies, e.g. static random access memory (SRAM), dynamic random access memory (DRAM), and flash memory, faces significant challenges due to the reliability issues, leakage currents (endurance issues), and profound uncertainty in their performance metrics especially beyond 16 nm technology (*ITRS 2009*).

2.3.1   Significance

Memory processing has been considered as the pace-setter for scaling a technology. A number of performance parameters including capacity (that relate to area utilisation), cost, speed (both access time and bandwidth), retention time, READ/WRITE endurance, active power dissipation, standby power, robustness such as reliability and temperature related issues characterise memories. Recent and emerging technologies such as Phase-Change Memory (PCM), Magnetic RAM (MRAM), Ferroelectric RAM (FeRAM), Resistive RAM (RRAM)[4], and Memristor, have promised SRAM and DRAM replacement and some are already being considered for implementation into emerging products.

---

[4]It can be also called *Resistance Chance Memory* (RCM).

2.3.2   Phase change memory (PCM)

PCM technology is based on a structure called a *phase change element*, a chalcogenide alloy, which is typically a Ge_2–Sb_2–Te_5 (GST) material. PCMs offer compatible integration with CMOS, which makes them a scalable technology. Similar structure can be found in commonly used optical storage devices, such as compact discs. The storage mechanism in PCM technology is based on switching two different resistances, an amorphous (high-resistance) and a crystalline (low-resistance) phase of the material. Furthermore, PCMs offer a denser structure compare to MRAMs, as shown in Table 2.1, with $6 \sim 16F^2$ area per memory cell (*ITRS 2009*), where F is technology feature size. A capacity of 1 Gb (for single-level cell (Villa *et al.* 2010)) and 256 Mb (for multi-level cell (Lee *et al.* 2008)) are achieved, however, PCM devices need further improvement on endurance and density (Li and Chen 2010).

2.3.3   Magnetic RAM

Spin-Torque Transfer RAM (STT-RAM), a new type of MRAM that offers a fast switching speed, non-volatility, and high endurance (Li and Chen 2010, Xie 2011). The core part of this technology is based on the magnetic tunnelling junction (MTJ). In such a structure, a thin tunnelling dielectric, for example MgO, is sandwiched by two ferromagnetic layers. One of them is designed to have its magnetisation pinned, whereas in the other layer the magnetisation can be flipped. This results in a low resistance if the magnetisations of the two layers are parallel and in a high resistance if they are anti-parallel. A new magnetisation mechanism is introduced in STT-RAMs which is called "polarisation-current-induced magnetization switching" in which the magnetization of free layer is flipped by an electrical current (Xie 2011). Although, this technology has shown several potential advantages over PCM and RRAM, its complex structure is one of the barriers toward its potential role in the next-generation on-chip cache or memory (Table 4.1).

2.3.4   Resistive RAM (RRAM)

Resistance switching memories can be classified as memristor-based memories (Chua 2011). Many companies around the world, including HP, IMEC, Unity Semiconductor,

Fujitsu, and Sharp, are working on one or more types of memristive (RRAM) materials. Its function is fairly simple. Two logical values, logic "1" and logic "0", are assigned to its Low Resistance State (LRS) and High Resistance State (HRS), respectively. The resistance is changed by applying a voltage across the device. If it is a bipolar switch, a negative voltage should be applied across the device to force the device switch back. On the other hand, if it is a unipolar switch, two different thresholds exist, hence, there is a need to exceed those thresholds to force the device to switch from one state to another (Kavehei *et al.* 2011d, Kavehei *et al.* 2010).

The underlying switching mechanism in RRAMs is different from PCMs, which use heat to change resistance. Therefore, when it comes to low-power applications, power consumption in PCMs presents a significant disadvantage when compare to RRAMs. Advantages of RRAMs can be classified as: (i) high density, (ii) relatively low manufacturing cost even compared to the available flash technologies, (iii) relatively acceptable endurance compare to predictions for 16 nm flash technology, (iv) architectural flexibility by using a simple and flexible crossbar array, (v) a variety of materials with memristive behaviour can be used, and finally (vi) significant potential in implementing learning algorithms and neuromorphic engineering. RRAM can be an answer to the need for a universal memory device if can be comparable to DRAM's switching speed and flash memory retention time.

Resistive switching in transition metal oxides (TMO) was discovered in thin nickel oxide (NiO) film in 1964 (Gibbons and Beadle 1964). Many materials have been studied since then, including titanium dioxide (TiO_2), strontium titanate ($SrTiO_3$), zirconia (ZrO_2), hafnia (HfO_2), etc. These materials can have two types of switching characteristics, unipolar and bipolar, as observed by Xie (2011).

For the TiO_2, an n-type binary oxide, which is the core material in this thesis, both bipolar and unipolar switching can be observed depending on the Schottky barrier height at the interface between metal electrodes and TiO_2. Two mechanisms are available in the literature for the resistance switching behaviour of the memristive materials: (1) filamentary mechanism, where the conduction path is formed and disappears due to the oxygen vacancy and applied voltage (Kim *et al.* 2011b), and (2) the effect of the potential barrier height in a metal-insulator-metal (MIM)[5] structure from the metal work function and the Fermi level of the oxide layer. Unfortunately, none of these

---

[5]Also known as metal-resistor-metal (MRM).

two mechanisms explain all the experimental observations. Therefore, more than one mechanism may be involved (Kim and Rhee 2010).

2.3.5   Discussion of memory technologies

Table 2.1 summarises a range of performance parameters and salient features of a number of technologies that characterise memories (Freitas 2008, *ITRS 2009)*. A projected plan for memories, in 2020, is aimed at a capacity greater than 1 TB, READ/WRITE access times of less than 100 ns and endurance in the order of 10^{12} or more cycles.

Flash memories suffer from both a slow write/erase times and low endurance cycles. FeRAMs and MRAMs are poorly scalable. MRAMs and PCMs require large programming currents during WRITE cycle, hence an increase in dissipation per bit. Furthermore, voltage scaling becomes more difficult. Memristors, however, have demonstrated promising results in terms of the WRITE operation voltage scaling as demonstrated by Strukov and Williams (2009a) and Kuekes *et al.* (2005).

Memristor crossbar-based architecture is highly scalable (Strukov and Williams 2009b) and shows promise for ultra-high density memories (Vontobel *et al.* 2009). For example, a memristor with minimum feature sizes of 10 nm and 3 nm yield 250 Gb·cm^{-2} and 2.5 Tb·cm^{-2}, respectively.

In spite of the high density, (ideally) zero standby power dissipation, and long life time that have been pointed out for the emerging memory technologies, their long WRITE latency has a negative impact on memory bandwidth, power consumption, and the general performance of a memory system.

2.4   A review of the memristor

Based on the *International Technology Roadmap for Semiconductors* (ITRS) report (*ITRS 2009)*, it is predicted that by 2019, 16 nm half-pitch dynamic random access memory (DRAM) cells will provide a capacity around 46 GB/cm^2, assuming 100% area efficiency. Interestingly, memristors promise high capacity more than 110 GB/cm^2 and 460 GB/cm^2 for 10 nm and 5 nm half-pitch devices, respectively (Williams 2008, Lewis and Lee 2009). In contrast to DRAM memory, memristors provide non-volatile operation as is the case for flash memories. Hence, such devices can continue the legacy of

Table 2.1. Performance of emerging memory technologies. Traditional and emerging memory technologies.

	Traditional Technologies		Improved Flash		Emerging Technologies			
	DRAM	SRAM	NOR	NAND	FeRAM	MRAM	PCM	Memristor
Knowledge level	mature		advanced		product	advanced		early stage
Cell Elements	1T1C	6T	1T		1T1C	1T1R	1T1R	1M
Half pitch (F) (nm)	50	65	90	90	180	130	65	3-10
Smallest cell area	6	140	10	5	22	45	16	4
READ time (ns)	<1	<0.3	<10	<50	<45	<20	<60	<50
Write/Erase time (ns)	<0.5	<0.3	10^5	10^6	10	20	60	<250
Retention time (years)	seconds	N/A	>10	>10	>10	>10	>10	>10
WRITE op. voltage (V)	2.5	1	12	15	0.9-3.3	1.5	3	<3
READ op. voltage (V)	1.8	1	2	2	0.9-3.3	1.5	3	<3
WRITE endurance	10^{16}	10^{16}	10^5	10^5	10^{14}	10^{16}	10^9	10^{15}
WRITE energy (fJ/bit)	5	0.7	10	10	30	1.5×10^5	6×10^3	<50
Density (Gbit·cm^{-2})	6.67	0.17	1.23	2.47	0.14	0.13	1.48	250
Voltage scaling	fairly scalable				no		poor	promising
Highly scalable	major technological barriers				poor		promising	promising

Moore's law for another decade. Furthermore, inclusion of molecular electronics and computing as an alternative to Complementary Metal-Oxide Semiconductor (CMOS) technologies in the recent ITRS report emphasises the significant challenges of device scaling (Jones 2009). Moreover, Swaroop *et al.* (1998) demonstrated that the complexity of a synapse, in an analogue VLSI neural network implementation, is minimised by using a device called the Programmable Metallisation Cell (PMC). This is an ionic programmable resistive device and a memristor can be employed to play the same role.

Research on memristor applications in various areas of circuit design, alternative materials and spintronic memristors, and especially memristor device/circuit modelling have appeared in the recent literature, (i) SPICE macro-modelling using linear and non-linear drift models (Chen and Wang 2009, Zhang *et al.* 2009, Biolek *et al.* 2009b, Benderli and Wey 2009, Kavehei *et al.* 2009, Li *et al.* 2009), (ii) application of memristors in different circuit configurations and their dynamic behaviour (Li *et al.* 2009, Sun *et al.* 2009a, Wang *et al.* 2009a, Sun *et al.* 2009b), (iii) application of memristor based dynamic systems to image encryption in Lin and Wang (2009), (iv) fine resolution programmable resistor using a memristor in Shin *et al.* (2009), (v) memristor-based op-amp circuit and filter characteristics of memristors by Yu *et al.* (2009) and Wang *et al.* (2009b), respectively, (vi) memristive receiver (MRX) structure for ultra-wide band (UWB) wireless systems (Itoh and Chua 2008, Witrisal 2009), (vii) memristive system I/O nonlinearity cancellation in Delgado (2009), (viii) the number of required memristors to compute a $f : \mathbb{R}^n \rightarrow \mathbb{R}^m$ function by Borghetti *et al.* (2010), and its digital logic implementation using a memristor-based crossbar architecture in Raja and Mourad (2009), (ix) different physical mechanisms to store information in memristors (Driscoll *et al.* 2009, Wang *et al.* 2009c), (x) interesting non-volatile memory fabricated using a *flexible memristor*, which is an inexpensive and low-power device solution is also recently reported (Gergel-Hackett *et al.* 2009), (xi) using the *memductance* concept to develop an equivalent circuit diagram of a transmission-line has been carried out by Mallégol (2003, Appendix 2). Furthermore, an electromagnetic (optical) transistor/memristor (EMTM) based on carbon nanotube (CNT) device was proposed in (Sklyar 2009). This magnetometer circuit is a possible through a combination of a superconducting field-effect transistor (SuFET) and molecular nano-wires both operating at or below room-temperature.

Among various memristor's features, two properties have attracted most attention. Firstly, its memory characteristic, and, secondly, its nanometer dimensions. The memory property and latching capability enable us to devise new methods for nanocomputing. The nanometer scale memristor device provides a very high density and is less power hungry. In addition, the fabrication process of nanodevices is simpler and cheaper than conventional CMOS fabrication, at the cost of more device defects (Strukov and Likharev 2005).

At the architectural level, a crossbar-based implementation appears to be the most promising realisation of the nanoscale (Bahar *et al.* 2007). Inherent defect-tolerance capability, simplicity, flexibility, scalability, and high density are the major advantages of this architecture by using a memristor at each cross point. In Lewis and Lee (2009) a comparison between using resistive random access memory (RRAM) and DRAM in a three-dimensional (3D) die-stacked structure was carried out. Advantages of RRAM over DRAM, as mentioned, are the extremely high capacity and potentially ultra low-power operation. As the capacity is growing, the complexity of addressing is also logarithmically growing, so the overhead addressing addressing cost is less for extremely high capacities (Lewis and Lee 2009).

The memristor store-to-write time constant ratio is around 10^3 cycles (Strukov and Williams 2009a), which is much lower than the DRAM cells with 10^6 (*ITRS 2009)*. Therefore, the switching speed of memristors is still behind DRAMs. However, unlike DRAM, RRAM is non-volatile. In terms of yield, DRAM and RRAM are almost equal from a futuristic viewpoint (Lewis and Lee 2009). Generally, endurance becomes very important once we note that the DRAM cells must be refreshed every 16 ms, which means at least 10^{10} WRITE cycles in their life time (Lewis and Lee 2009).

Architectural issues of these nanoelectronic systems are also very important. Designing a nanoelectronic system has to be viable and reliable. As already mentioned, a crossbar architecture delivers a good performance based on its simple structure. However, one of the main concerns at the architectural level, particularly for using nanodevices, is a defect- and fault-tolerance. Fault-tolerance and parallel processing architectural approaches are not in the scope of this thesis. The reader is referred to Han (2004) and Strukov (2006) for more information on this aspect.

It is interesting to note that there are devices with similar behaviour to a memristor, e.g. Buot and Rajagopal (1994), Beck *et al.* (2000), Krieger *et al.* (2001), Liu *et al.* (2006),

Waser and Aono (2007), Ignatiev *et al.* (2008), Tulina *et al.* (2008), but the HP scientists were the only group that found the link between their work and the missing memristor postulated by Chua (1971). Moreover, it should be noted that physically realised memristors must meet the mathematical requirements of a memristor device or memristive systems that are discussed in Kang (1975) and Chua and Kang (1976). For instance, the hysteresis loop must have a double-valued bow-tie trajectory. However, for example in Krieger *et al.* (2001), the hysteresis loop shows more than two values for some applied voltage values. Beck *et al.* (2000) demonstrated one of the perfect examples of memristor devices. Generic prosperities of memristive devices that clearly distinguish a memristive device from other devices can be listed as follows (Kang 1975, Chua and Kang 1976):

Passivity operation. Memristive device is a passive element.

No energy discharge. If the device is a passive device, therefore, the instantaneous power is always nonnegative.

DC characteristics. Memristive device operation under DC operation is equivalent to nonlinear resistor.

Double-valued hysteresis *I-V* loop. Memristive device under periodic operation[6] always gives a current-voltage relationship that $I(V)$ is at most a doubled-valued function of $V(I)$.

Symmetric hysteresis loop. If in a time-invariant voltage-controlled[7] memristive one-port device, e.g. Eq. (2.1), $g(w, V) = g(w, -V)$, then the corresponding *I-V* curve is not a closed loop whenever the state variable, $w(t)$, is periodic of the same period as that of the input $V(t)$ and is half-wave symmetric[8]. The *I-V* curve relationship is odd symmetric with respect to the origin whenever $w(t)$ is periodic of the same period as that of the input $V(t)$ and is quarter-wave symmetric[9].

Limiting linear characteristics. If for all t_0, for all initial states w_0, and for all bounded inputs (V), the state trajectory $w(t)$ is bounded, then the dynamical system,

---

[6]Its operation is periodic when its response and the input are from the same period.

[7]All of the properties apply to the dual current-controlled case.

[8]The state variable function of period T is half-wave symmetric if $w(t + kT/2) = w(-t + kT/2)$ for $k = 1, 2$ for all $t \in [0, T/2]$.

[9]The state variable function of period T is quarter-wave symmetric if $w(t + kT/4) = w(-t + kT/4)$ for $k = 1, 3$ for all $t \in [0, T/4]$.

Eq. (2.1), is stable and its periodic operation degenerates into a linear invariant resistor as the input frequency increases toward infinity.

Details on proofs and small-signal properties can be found in Kang (1975). Kim *et al.* (2009a) recently introduced a multi-level One-Time Programmable (OTP) oxide diode for crossbar memories. They focused on a one-time programmable structure that basically utilises one diode and one resistor, 1D-1R, since obtaining a stable device for handling multiple programming and erasing processes is much more difficult than a one-time programmable device. In terms of functionality, OTP devices are very similar to memristive elements, but in terms of flexibility, memristors are able to handle multiple programming and erasing processes.

2.5 Conclusion

This chapter surveyed key aspects of the memristor as a promising nanodevice. It also reviewed memcapacitor and meminductor elements. A comparison between the emerging non-volatile memory technologies shows that the biggest rival of RRAM technology is PCM, given the fact that, the size and the fabrication costs of MRAM technology is higher than these two technologies. When it come to power dissipation and size, RRAMs promise better quantities than PCMs. MRAMs promise the best speed and endurance performance among the technologies, whereas PCMs show a better outcome in terms of density, cost, and technological compatibility with the current CMOS devices. RRAMs demonstrate the least power dissipation. Its READ and WRITE access times are in an acceptable range and it is very well compatible with the current integrated circuit technology. It is also important to note that memristive electronics cover all possible technologies that provide switching behaviour between two or more stable states by changing the resistance. By this definition, PCMs can also be classified as memristive elements.

This chapter also provides an overview on several applications for memristive devices. The different capabilities might create many opportunities as well as engineering challenges. These challenges should be addressed through modelling and design modifications, which are the context of following chapters. The next chapter discusses a preliminary SPICE model and its switching behaviour as well as introducing resistance modulation index and memristor properties through simulation.

Chapter 3

Memristor's Basic Characteristics and Early Modelling Approaches

THE non-volatile memory property of a memristor enables the realisation of new approaches for a variety of computational engines ranging from innovative memristive based neuromorphic circuitry through to advanced memory applications. The nanometer scale feature of the device also creates a new opportunity for realisation of innovative circuits that in some cases are not possible or have an inefficient realisation in the present and established technologies. The nature of the boundary, the complexity of the ionic transport and tunnelling mechanism, and the nanoscale feature of the memristor introduces challenges in modelling, characterisation, and simulation of future circuits and systems. These new challenges require solution via insight from the designers' perspective, in order to attain accurate estimation of performance. This chapter provides basics for the memristor modelling approaches and its behaviour when combined with other circuit elements.

[This page has been left blank intentionally.]

3.1   Introduction

This chapter provides models for the memristor and memristive devices. Applications of these models in circuits and systems will be shown in the next few chapters. An introduction to the electromagnetic theory of the memristor and a very first demonstration of that approach using Maxwell's equations and geometric algebra can be also found in the Appendix A. The Appendix presents an argumentation based on electromagnetic field theory for the existence of the memristor according to Chua (1971). His motivation was to interpret the memristor in terms of the so-called *quasi-static expansion* of Maxwell's equations. This expansion is usually used to give an explanation to the elements of circuit theory within the electromagnetic field theory.

This chapter consists of four sections. Sections 3.2 and 3.3 discuss the simplest model of memristors, which is based on a linear drift model, and a more complicated model using a nonlinear drift approximation. This section introduces resistance modulation index and some of the memristor properties through simulation. The next section, Section 3.4, presents a basic SPICE model for memristors that shows the basic switching behaviour.

3.2   Linear drift model

The memristor's state equation is at the heart of the HP memristive system mechanism (Wang 2008, Joglekar and Wolf 2009). An attractive property of the HP memristor (Strukov *et al.* 2008), which is exclusively based on its fabrication process, can be deduced from the simple HP memristor mathematical model (Strukov *et al.* 2008) and is given by,

$$M(q) = R_{\text{HRS}} \left(1 - \frac{R_{\text{LRS}}}{\beta_\Phi} q(t) \right), \tag{3.1}$$

where β_Φ has the dimensions of magnetic flux $\Phi(t)$. Here, $\beta_\Phi = \frac{L^2}{\mu_{\text{L}}}$ in units of $\text{sV} \equiv \text{Wb}$, where μ_{L} is the average drift mobility in unit of cm^2/sV and L is the film (TiO$_2$) thickness. Note that R_{HRS} and R_{LRS} are simply the 'ON' and 'OFF' state resistances as indicated in Figure 2.2. Also $q(t)$ defines the total charge passing through the memristor device within a time window, t - t_0. Notice that the memristor has an internal

state (Chua and Kang 1976). Furthermore, as stated in Oster (1974), $q(t) = \int_{t_0}^{t} i(\tau)d\tau$, due to the state variable in a charge-controlled memristor giving the charge passing through the device and not behaving as charge storage channel as in a capacitor. This concept is very important from two points of view. Firstly, a memristor is not an energy-storage element, and secondly, this shows that the memristor is not merely a nonlinear resistor, but is a nonlinear resistor with charge as a state variable (Oster 1974).

Let us assume a uniform electric field across the device, thus there is a linear relationship between drift-diffusion velocity and the net electric field (Blanc and Staebler 1971). Therefore the state equation is,

$$\frac{1}{L}\frac{dw(t)}{dt} = \frac{R_{\mathrm{LRS}}}{\beta_\Phi}i(t) \,. \tag{3.2}$$

Integrating Eq. (3.2) gives,

$$\frac{w(t)}{L} = \frac{w(t_0)}{L} + \frac{R_{\mathrm{LRS}}}{\beta_\Phi}q(t) \,, \tag{3.3}$$

when $w(t_0)$ is the initial length of w. Hence, the speed of drift under a uniform electric field, across the device is given by $v_{\mathrm{L}} = \frac{dw(t)}{dt}$. In a uniform field we have $L = v_{\mathrm{L}} \times t$. In this case $Q_{\mathrm{L}} = i \times t$ also defines the amount of required charge to move the boundary from $w(t_0)$, when $w \to 0$, to distance $w(t_{\mathrm{L}})$, where $w \to L$. Therefore, Eq. (3.3) can be written using the new definition of $Q_{\mathrm{L}} = \frac{\beta_\Phi}{R_{\mathrm{LRS}}}$ as,

$$\frac{w(t)}{L} = \frac{w(t_0)}{L} + \frac{q(t)}{Q_{\mathrm{L}}} \,. \tag{3.4}$$

If $x(t) = \frac{w(t)}{L}$ then,

$$x(t) = x(t_0) + \frac{q(t)}{Q_{\mathrm{L}}} \,, \tag{3.5}$$

where $\frac{q(t)}{Q_{\mathrm{L}}}$ describes the amount of charge that is passed through the channel over the required charge for a conductive channel.

Using Strukov *et al.* (2008) we have,

$$V(t) = \left(R_{\mathrm{LRS}}\frac{w(t)}{L} + R_{\mathrm{HRS}}\left(1 - \frac{w(t)}{L}\right)\right)i(t) \,. \tag{3.6}$$

Therefore, memristance of a charge controlled memristor[10], $M(q)$, can be written as,

$$M(q) = R_{\text{LRS}} \frac{w(t)}{L} + R_{\text{HRS}} \left(1 - \frac{w(t)}{L} \right). \tag{3.7}$$

By inserting $x(t) = \frac{w(t)}{L}$, Eq. (3.6) can be rewritten as,

$$V(t) = \left(R_{\text{LRS}} \, x(t) + R_{\text{HRS}} \left(1 - x(t) \right) \right) i(t). \tag{3.8}$$

Now assume that $q(t_0) = 0$ then $w(t) = w(t_0)$, when $w(t) \neq 0$, and from Eq. (3.8),

$$M_0 = R_{\text{LRS}} \left(x(t_0) + r \left(1 - x(t_0) \right) \right), \tag{3.9}$$

where $r = \frac{R_{\text{HRS}}}{R_{\text{LRS}}}$ and M_0 is the memristance, $M(q)$, value at t_0. Consequently, the following equation gives the memristance at time t,

$$M(q) = M_0 - \Delta R \left(\frac{q(t)}{Q_{\text{L}}} \right), \tag{3.10}$$

where $\Delta R = R_{\text{HRS}} - R_{\text{LRS}}$. When $R_{\text{HRS}} \gg R_{\text{LRS}}$, $\Delta R \approx R_{\text{HRS}}$, and $M_0 \approx R_{\text{HRS}}$, Eq. (3.1) can be derived from Eq. (3.10).

Substituting Eq. (3.10) into $V(t) = M(q)i(t)$, when $i(t) = \frac{dq(t)}{dt}$, we have,

$$V(t) = \left(M_0 - \Delta R \left(\frac{q(t)}{Q_{\text{L}}} \right) \right) \frac{dq(t)}{dt}. \tag{3.11}$$

Recalling that $M(q) = \frac{d\Phi(q)}{dq}$, the solution is

$$q(t) = \frac{Q_L M_0}{\Delta R} \left(1 \pm \sqrt{1 - \frac{2\Delta R}{Q_L M_0^2} \Phi(t)} \right). \tag{3.12}$$

---

[10]These equations are also applicable to the dual voltage-controlled case, where memductance $W(\Phi)$ represents overall conductance of a memristor.

---

then, a valid solution for $q(t)$, if $\Delta R \approx M_0 \approx R_{\text{HRS}}$, can be written as,

$$q(t) = Q_L \left(1 - \sqrt{1 - \frac{2}{Q_L R_{\text{HRS}}} \Phi(t)} \right). \tag{3.13}$$

Consequently, using Eq. (3.5) if $Q_L = \frac{L^2}{\mu_L R_{\text{LRS}}}$, so the internal state of the memristor is

$$x(t) = 1 - \left(\sqrt{1 - \frac{2\mu_L}{rL^2} \Phi(t)} \right), \tag{3.14}$$

then, considering Eq. (3.7) and $x(t) = \frac{w(t)}{L}$, the current-voltage relationship can be written as,

$$i(t) = \frac{V(t)}{R_{\text{HRS}} \left(\sqrt{1 - \frac{2\mu_L}{rL^2} \Phi(t)} \right)}. \tag{3.15}$$

In Eq. (3.15), the inverse square relationship between memristance and TiO$_2$ thickness, L, shows that for smaller values of L, the memristance shows improved characteristics, and because of this reason the memristor require a small value of L.

In Eqs. (3.12)-(3.15), the only term that significantly increases the role of $\Phi(t)$ is a lower value of Q_L. This shows that at the micrometer scale $\frac{1}{R_{\text{HRS}}Q_L} = \frac{1}{r\beta_\Phi} = \frac{\mu_L}{rL^2}$ is negligible and the relationship between current and voltage reduces to a resistor equation.

Substituting $\beta_\Phi = \frac{L^2}{\mu_L}$ that has the same units as magnetic flux into Eq. (3.15), and considering $c(t) = \frac{\Phi(t)}{\beta_\Phi} = \frac{\mu_L \Phi(t)}{L^2}$ as a normalised variable, we obtain

$$i(t) = \frac{V(t)}{R_{\text{HRS}} \left(\sqrt{1 - \frac{2}{r} c(t)} \right)}, \tag{3.16}$$

where $\sqrt{1 - \frac{2}{r} c(t)}$ is what we call the *resistance modulation index*, (RMI) (Kavehei *et al.* 2009).

Due to the current limitation on the accuracy of fabrication of nano device, variability-aware modelling approach should always be considered. Two well-know solutions by

Chen and Wang (2009) were investigated to address the variability problem in memristive systems: 1) Monte-Carlo simulation for evaluating (almost) complete statistical behaviour of device, and 2) Corner analysis. Considering the trade-off between time-complexity and accuracy between these two approaches, demonstrate the importance of using a simple and reasonably accurate model, because finding the real corners is highly dependent on the model accuracy (Chen and Wang 2009). The resistance modulation index, RMI, could be one of the device parameters ($\sqrt{V}$ dependency) in the model extraction phase, so it would help to provide a simple model with fewer parameters.

Joglekar and Wolf (2009) clarified the behaviour of two memristors in series. As shown in Figure 3.1, they labelled the polarity of a memristor by $\eta = \pm 1$, where $\eta = +1$ signifies that $w(t)$ increases with positive voltage or, in other words, the doped region in memristor is expanding. If the doped region, $w(t)$, is shrinking with positive voltage, then $\eta = -1$. In other words, reversing the voltage source terminals implies memristor polarity switching. In Figure 3.1 (a), the doped regions are simultaneously shrunk so the overall memristive effect is retained. In Figure 3.1 (b), however, the overall memristive effect is suppressed (Joglekar and Wolf 2009).
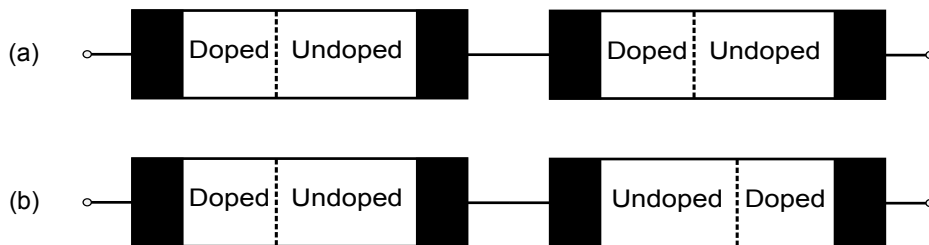
Figure 3.1. Two bipolar memristors in series. Two memristors in series, (a) With the same polarity, both $\eta = -1$ or both $\eta = +1$. (b) With opposite polarities, $\eta = -1$ and $\eta = +1$. Where $\eta = +1$ signifies that $w(t)$ increases with positive voltage or, in other words, the doped region in memristor is expanding and $\eta = -1$ indicates that the doped region is shrinking with applied positive voltage across the terminals Joglekar and Wolf (2009).

Using the memristor polarity effect and Eq. (3.2), we thus obtain

$$\frac{1}{L}\frac{dw(t)}{dt} = \eta \frac{R_{\text{LRS}}}{\beta_\Phi} i(t) \, . \tag{3.17}$$

Then with similar approach we have

$$i(t) = \frac{V(t)}{R_{\text{HRS}}\left(\sqrt{1 - \eta_r^2 c(t)}\right)} . \tag{3.18}$$

There is also no phase shift between current and voltage signals, which implies that the hysteresis loop always crosses the origin as demonstrated in Figure 3.2. For further investigation, if a voltage, $V(t) = V_0 \sin(\omega t)$, is applied across the device, the magnetic flux would be $\Phi(t) = -\frac{V_0}{\omega}\cos(\omega t)$. The inverse relation between flux and frequency shows that at very high frequencies there is only a linear resistor.

Eq. (3.18) was implemented in MATLAB for five different frequencies, where $\omega_0 = \frac{2\pi V_0}{\beta_\Phi}$, using the Strukov *et al.* (2008) parameter values, $L = 10$ nm, $\mu_L = 10^{-10}$ cm^2 s^{-1} V^{-1}, $R_{\text{LRS}} = 100$ Ω, $R_{\text{HRS}} = 16$ kΩ, $V_0 = 1$ V, and $\eta = -1$, the results are shown in Figure 3.2. The *resistance modulation index*, RMI $= \sqrt{1 - \eta_r^2 c(t)}$ simulation with the same parameter values is shown in Figure (3.3).
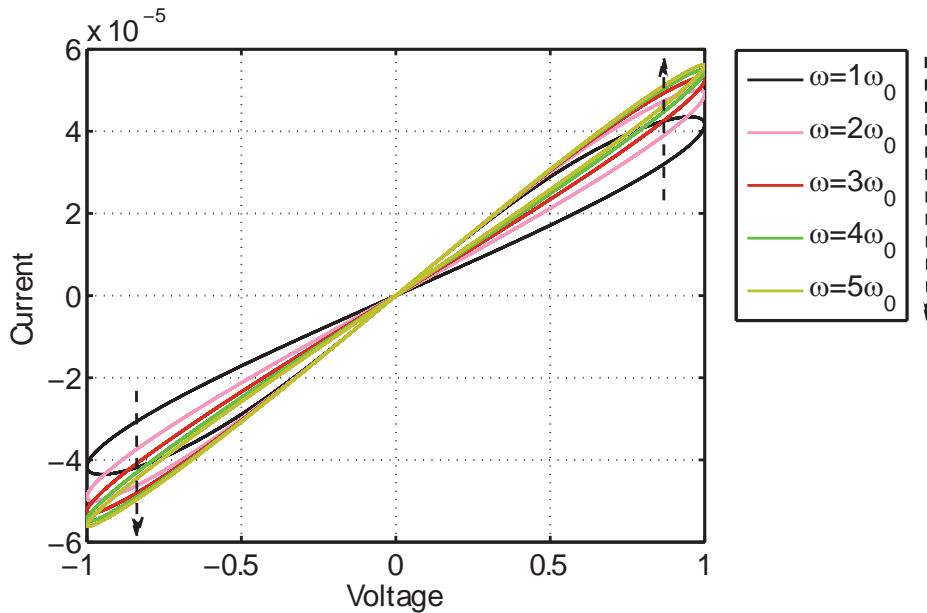
Figure 3.2. Memristor model and its angular frequency response. The hysteresis of a memristor based on Eq. (3.18). This verifies the hysteresis shrinks at higher frequencies. It also shows that the effective resistance is changing, so there is a varying memristance with a monotonically-increasing q-Φ curve. The current value is in Amps (A) and voltage is in Volts (V).

```
┌─────────────────────────────────────────────┐
│                    NOTE:                      │
│   This figure is included on page 39 of the   │
│   print copy of the thesis held in the        │
│   University of Adelaide Library.             │
└─────────────────────────────────────────────┘
```

Figure 3.3. RMI simulation. The hysteresis characteristics of the memristor. It shows that the memristance value is varying from a very low to a very high resistance. It is clear that these values depend on the parameter values, such as R_{LRS} and R_{HRS}. The model is consistent with the HP's model parameters (Strukov *et al.* 2008).

3.3   Nonlinear drift model

The electrical behaviour of the memristor is directly related to the shift in the boundary between doped and undoped regions, and the effectively variable total resistance of the device when an electrical field is applied. Basically, a few volts across a very thin-film, e.g. 10 nm, causes a large electric field. For instance, it could be more than 10^6 V/cm, which will result in a fast and a significant reduction in energy barrier (Blanc and Staebler 1971). Therefore, it is reasonable to expect a high nonlinearity in ionic drift-diffusion (Waser *et al.* 2009).

One significant problem with the linear drift assumption is the boundaries. The linear drift model, Eq. (3.2), suffers from a problematic boundary effects. Basically, at the nanoscale, a few volts causes a large electric field that leads to a significant nonlinearity in ionic transport (Strukov *et al.* 2008). A few attempts have been carried out so far to consider this nonlinearity in the state equation (Strukov *et al.* 2008, Strukov and Williams 2009a, Biolek *et al.* 2009b, Benderli and Wey 2009, Prodromakis *et al.* 2011). All of them proposed a *window function*, $f(w,i)$, which is multiplied by the right-hand side of Eq. (3.2), where w and i are the memristor's state variable and current, respectively.

In general, the window function can be multiplied by the right-hand side of the state variable equation, Eq. (3.2),

$$\frac{dx(t)}{dt} = \eta \frac{R_{\text{LRS}}}{\beta} i(t) f(x(t), p) , \tag{3.19}$$

where $x(t) = w(t)/L$ is the normalised form of the state variable. The window function makes a large difference between the model with linear and nonlinear drift assumptions at the boundaries. Figure 3.4 shows such a condition considering a nonlinear drift assumption at the critical, or boundary, states. In other words, when a linear drift model is used, simulations should consider the boundaries and all constraints on initial current, initial voltage, maximum and minimum w, and etc. These constraints cause a large difference in output between linear and nonlinear drift assumptions. For example, it is impossible to achieve such a realistic curve, as in Figure 3.4, using the linear drift modelling approach.
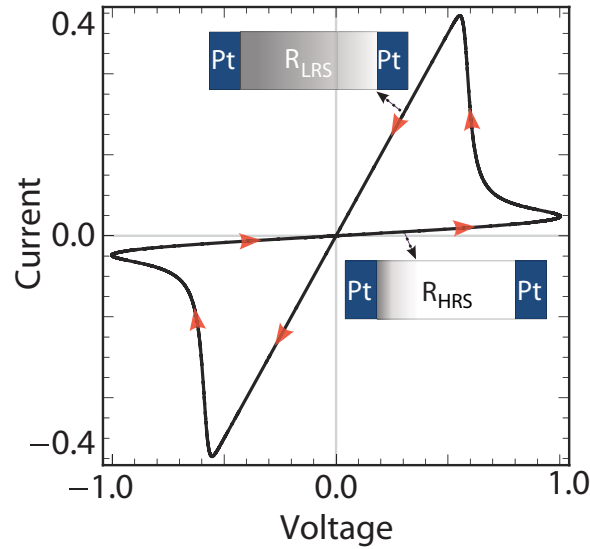
Figure 3.4. Nonlinear I-V characteristics of the memristor. The hysteresis characteristics using the nonlinear drift assumption. This hysteresis shows a highly nonlinear relationship between current and voltage at the boundaries. To model this nonlinearity, there is a need for an additional term on the right hand side of the memristor's state equation, called a *window function*. R_{LRS} represents the low resistance state and it can be shown as G_{ON}, ON state conductance, and R_{HRS} shows the high resistance state and it can be shown as G_{OFF}, OFF state conductance.

3.3.1   Window function

In Strukov *et al.* (2008), the window function is a function of the state variable and it is defined as $f(w) = w(1-w)/L^2$. The boundary conditions in this case are $f(0) = 0$ and $f(L) = \frac{1-L}{L} \approx 0$. It meets the essential boundary condition $f(w \to \text{boundaries}) = 0$, except there is a slight difference when $w \to L$. The problem of this boundary assumption is when a memristor is driven to the terminal states, $w \to 0$ and $w \to L$, then $\frac{dw}{dt} \to 0$, so no external field can change the memristor state (Biolek *et al.* 2009b). This is a fundamental problem of the window function. The second problem of the window function is it assumes that the memristor remembers the amount of charge that passed through the device. Basically, this is a direct result of the state equation, Eq. (3.2), (Biolek *et al.* 2009b).

In Benderli and Wey (2009), another window function has been proposed that is slightly different from that in Strukov *et al.* (2008). This window function, $f(w) = w(L-w)/L^2$, approaches zero when $w \to 0$ and when $w \to L$ then $f(w) \to 0$. Therefore, this window function meets both the boundary conditions. In fact, the second window function imitates the first function when we consider $x = w/L$ instead of w. In addition, there is another problem associated with these two window functions, namely, the modelling of approximate linear ionic drift when $0 < w < L$. Both of the window functions approximate nonlinear behaviour when the memristor is not in its terminal states, $w = 0$ or $w = L$. This problem is addressed in Joglekar and Wolf (2009) where they propose an interesting window function to address the nonlinear and approximately linear ionic drift behaviour at the boundaries and when $0 < w < L$, respectively. Nonlinearity (or linearity) of their function can be controlled with a second parameter, which we call the *control parameter*, p. Their window function is $f(x) = 1 - (2x - 1)^{2p}$, where $x = w/L$ and p is a positive integer. Figure 3.5 (a) demonstrates the function behaviour for different $2 \leq p \leq 10$ values. This model considers a simple boundary condition, $f(0) = f(1) = 0$. As demonstrated, when $p \geq 4$, the state variable equation is an approximation of the linear drift assumption, $f(0 < x < 1) \approx 1$.

The most important problem associated with this model is revealed at the boundaries. Based on this model, when a memristor is at the terminal states, no external stimulus can change its state. Biolek *et al.* (2009b) tackles this problem with a new window function that depends on x, p, and memristor current, i. Basically, x and p are playing the same role in their model and the only new idea is using current as an extra parameter.

The window function is, $f(x) = 1 - (x - \text{sgn}(-i))^{2p}$, where i is memristor current and $\text{sgn}(i) = 1$ when $i \geq 0$, and $\text{sgn}(i) = 0$ when $i < 0$. As a matter of fact, when the current is positive, the doped region length, w, is expanding. Figure 3.5 (b) illustrates the window function behaviour.
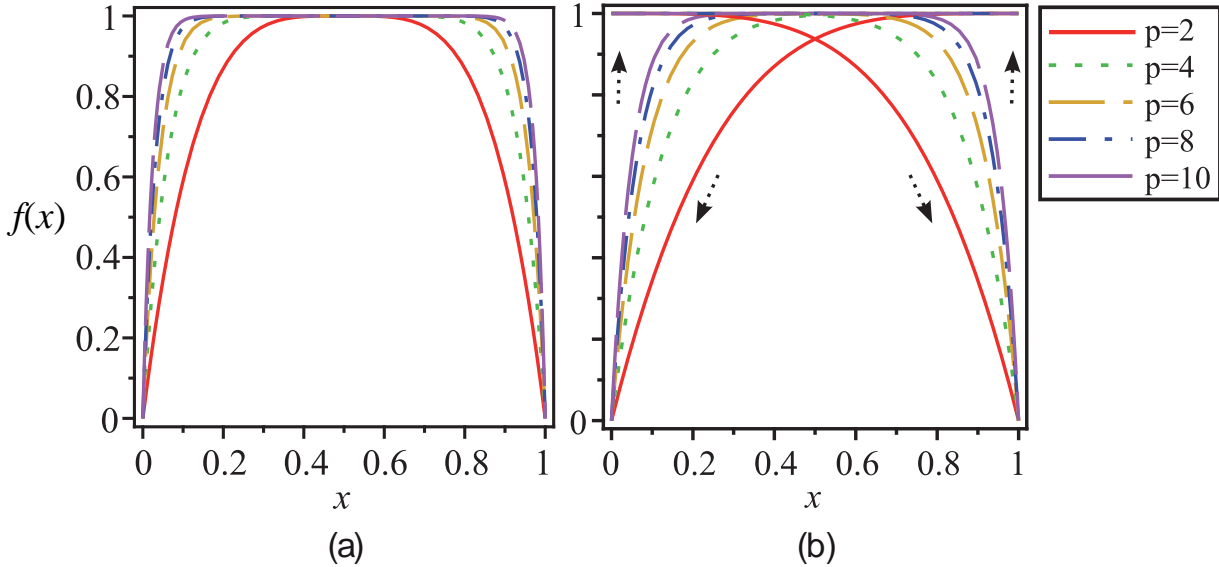
Figure 3.5. Window function $f(\cdot)$. Non-linear window functions, (a) $f(x) = 1 - (2x - 1)^{2p}$, (b) $f(x) = 1 - (x - \text{sgn}(-i))^{2p}$. There are around four window functions in the literature but these two are meet the boundary conditions.

All window functions suffer from a serious problem. They are only dependent on the state variable, x, which implies that the memristor remembers the entire charge that is passing through it. Moreover, based on the general definition of the time-invariant memristor's state equation and current-voltage relation, $\dot{x} = f(x,i)$ or $\dot{x} = g(x,v)$, f and g must be *continuous n-dimensional vector functions* (Kang 1975, chap. 2). However, the last window function, $f(x) = 1 - (x - \text{sgn}(-i))^{2p}$, does not provide the continuity condition at the boundaries, $x \to 0$ or $x \to 1$. Biolek *et al.* (2009b) did not use the window function in their recent publication (Biolek *et al.* 2009a).

In Strukov and Williams (2009a) the overall drift velocity is identified with one linear equation and one highly nonlinear equation, $v = \mu E$, when $E \ll E_0$ and $v = \mu E_0 \exp(\frac{E}{E_0})$, for $E \sim E_0$, where v is the average drift velocity, E is an applied electric field, μ is the mobility, and E_0 is the characteristic field for a particular mobile ion. The value of E_0 is typically about 1 MV/cm at room temperature (Strukov and Williams 2009a). This equation shows that a very high electric field is needed for exponential ion transport. They also showed that the high electric field is lower than the critical field for dielectric

breakdown of the oxide. Reviewing the available window functions indicates that there is a need for an appropriate model that can define memristor states for strongly nonlinear behaviour where, $E \sim E_0$.

In addition to the weakness of nonlinear modelling in the original HP model, there are some other drawbacks that show the connection between physics and electronic behaviour was not well established. Moreover, the currently available electronic models for memristors followed the exact pathway of the HP modelling, which is mostly due to the fact that the underlying physical conduction mechanism is not fully clear yet (Kim *et al.* 2009b). Furthermore, the HP model does not deliver any insight about capacitive effects, which are naturally associated with memristors. These capacitive effects will later be explained in terms of a memcapacitive effect in a class of circuit elements with memory. In Kim *et al.* (2009b) the memristor behaviour was realised using infinite number of crystalline magnetite (Fe_3O_4) nanoparticles. The device behaviour combines both memristive (time-varying resistance) and memcapacitive (time-varying capacitance) effects, which deliver a better model for the nonlinear properties. Their model description for current-voltage relationship is given as,

$$i(t) = \frac{V(t)}{\sqrt{R^2(x,t) + \frac{1}{i^2(t)}\left(\frac{q(t)}{C(x,t)}\right)^2}} \, , \tag{3.20}$$

where $R(x,t)$ and $C(x,t)$ are the time-varying resistance and capacitance effects, respectively. The time-dependent capacitor is a function of the state variable, $x(t) = w(t)/L$ and $\Delta C(t)$, where $\Delta C(t)$ is defined as the additional capacitance caused by changing the value of capacitance (Kim *et al.* 2009b), $C(x,t) = \frac{C_{ON} - \Delta C(t)}{1 - x(t)}$, where C_{ON} is the capacitance at $x = 0$. The state variable is also given by,

$$x(t) = \frac{1}{\beta}\left(q(t)R_{ON} + \frac{\int_{t_0}^{t} q(\tau)\,d\tau}{C_{ON} - \Delta C(t)}\right) . \tag{3.21}$$

Kim *et al.* (2009b) also investigated the impact of temperature variation on their Fe_3O_4 nanoparticle memristor assemblies for different L values (9 nm, 12 nm, and 15 nm). It was reported that the change in electrical resistivity (specific electrical resistance), ρ_r, as an explicit function of temperature can be defined by, $\log(\rho_r) = 1/\sqrt{T}$, which means there is a significantly increasing behaviour as temperature decreases. As a consequence, for example, there is no hysteresis loop signature at room temperature,

$T = 295$ K, $(L = 12$ nm) while at $T = 210$ K it shows a nice bow-tie trajectory. As they claimed, the first room temperature reversible switching behaviour was observed in their nanoparticle memristive system (Kim *et al.* 2009b).

3.4   Basic SPICE macro-model of memristor

There are, generally, three different ways available to model the electrical characteristics of the memristors. SPICE macro-models, hardware description language (HDL), and C programming. The first, SPICE macro-models, approach is more appropriate since it is more readable for most of the readers and available in all SPICE versions. There is also another reason for choosing SPICE modelling approach. Regardless of common convergence problems in SPICE modelling, we believe it is more appropriate way to describe real device operation. Moreover, using a model as a sub-circuit can highly guarantee a reasonably high flexibility and scalability features.

A memristor can be realised by connecting an appropriate nonlinear resistor, inductor, or capacitor across port 2 of an M-R mutator, an M-L mutator, or an M-C mutator, respectively [11]. These mutators are nonlinear circuit elements that may be described by a SPICE macro-model (i.e. an analogue behavioural model of SPICE). The macro circuit model realisation of a type-1 M-R mutator based on the first realisation of the memristor is shown in Figure 3.6 (Chua 1971).

In this model, the M-R mutator consists of an integrator, a Current-Controlled Voltage Source (CCVS) "H", a differentiator and a Voltage-Controlled Current Source (VCCS) "G". The nonlinear resistor is also realised with resistors R_1, R_2, and a switch. Therefore, the branch resistance is 1 kΩ for $V_1 < 2$ V and 2 kΩ for $V_1 \geq 2$ V. The input voltage of port 1, V_1, is integrated and connected to port 2 and the nonlinear resistor current, I_2, is sensed with the CCVS "H" and differentiated and converted into current with the VCCS "G".

SPICE simulations with the macro-model of the memristor are shown in Figures 3.7 and 3.8. In this particular simulation, a monotonically-increasing and piecewise-linear q-Φ function is assumed for the memristor characteristic. This function is shown in Figure 3.7 (b). The simulated memristor has a value of 1 kΩ for flux value of less

---

[11] For further detail about the mutator the reader is referred to Chua (1968).
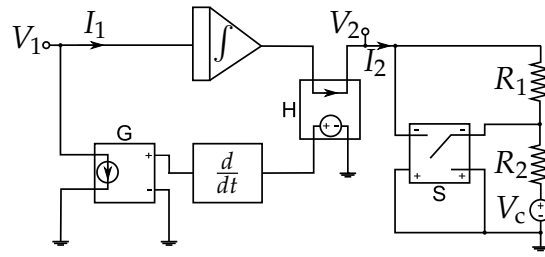
Figure 3.6. Basic SPICE macro model. The SPICE macro-model of memristor. Here G, H and S are a Voltage-Controlled Current Source (VCCS), a Current-Controlled Voltage Source (CCVS), and a Switch ($V_{ON} = -1.9$ V and $V_{OFF} = -2$ V), respectively. $R_1 = R_2 = 1$ kΩ and $V_c = -2$ V. The M-R mutator consists of an integrator, a Current-Controlled Voltage Source (CCVS) "H", a differentiator and a Voltage-Controlled Current Source (VCCS) "G". The nonlinear resistor is also realised with resistors R_1, R_2, and a switch. Therefore, the branch resistance is 1 kΩ for $V_1 < 2$ V and 2 kΩ for $V_1 \geq 2$ V.

than 2 Wb, but it becomes 2 kΩ when the flux is greater than or equal to 2 Wb. The critical flux (φ_c) can be varied with the turn-on voltage of the switch in the macro-model. Figure 3.7 (a) shows the pinched hysteresis characteristic of the memristor. The input voltage to the memristor is a ramp with a slope of $+1$ V/s and -1 V/s. When the input voltage ramps up, the memristance is 1 kΩ and the slope of the current-voltage characteristics is 1 mA/V before the the flux reaches to the Φ_c. But when the flux becomes 2 Wb, the memristance value is changed to 2 kΩ and the *I-V* curve slope is now 0.5 mA/V. After the input voltage reaches a maximum point, it ramps down and the slope is maintained, because the memristance is still 2 kΩ. Figure 3.8 shows the memristor characteristics when a step input voltage is applied. Initially the memristance is 1 kΩ, so the input current is 1 mA. When the flux reaches to 2 Wb (1 V $\times$ 2 s), the memristance is 2 kΩ and so the input current is now 0.5 mA as predicted. The developed macro-model can be used to understand and predict the characteristics of a memristor.

Now, if a 1 kHz sinusoidal voltage source is connected across the memristor model, the flux does not reach to 2 Wb so $M = M_1 = 1$ kΩ and $i = 10$ mA. Figure 3.9(I) shows the memristor characteristics when a sinusoidal input voltage is applied. As it is shown in Figure 3.9(II), when the voltage source frequency reduces to 10 Hz, the flux linkage reaches to 2 Wb within 30 ms. Based on the result, there are two levels of memristance, $M = M_1 = 1$ kΩ and then it changes to $M_2 = 2$ kΩ.
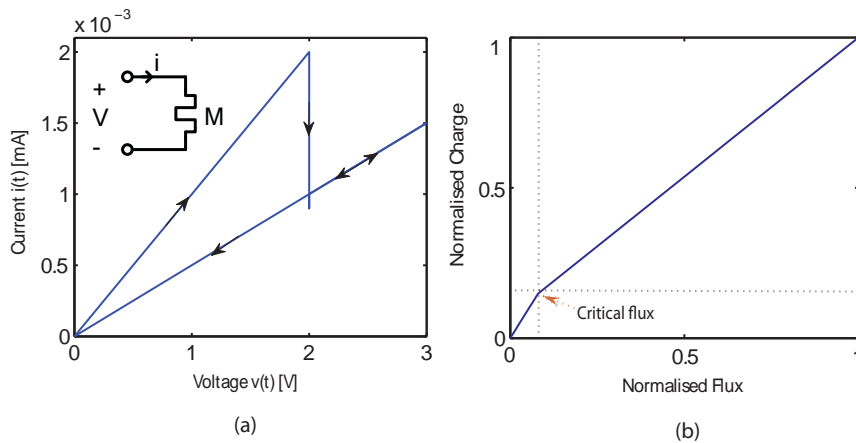
Figure 3.7. Basic memristor characteristics of switching between two high and low resistances. The memristor characteristics. (a) The hysteresis characteristics of the memristor. (b) A monotonically-increasing and piecewise-linear q-Φ function as a basic memristor characteristic, the both axes are normalised to their maximum values. The simulated memristor has a value of 1 kΩ when the flux is less than 2 Wb, but it becomes 2 kΩ when the flux is equal or higher than 2 Wb. The critical flux (Φ_c) can be varied with the turn-on voltage of the switch in the macro-model. The input voltage to the memristor is a ramp with a slope of ± 1 V/s.
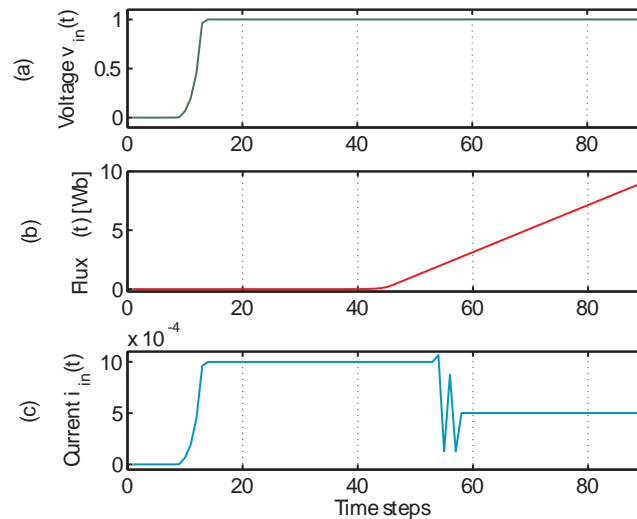
Figure 3.8. Response of the memristor to a step voltage input. The memristor characteristics when a step input voltage is applied. (a) Voltage curve. (b) Flux linkage curve. (c) Current curve. At the first point the memristance is 1 kΩ, so the input current is 1 mA. When the flux reaches to 2 Wb (1 V $\times$ 2 s, 2 s $=$ 50 time steps), the memristance is 2 kΩ and so the input current is now 0.5 mA as predicted.
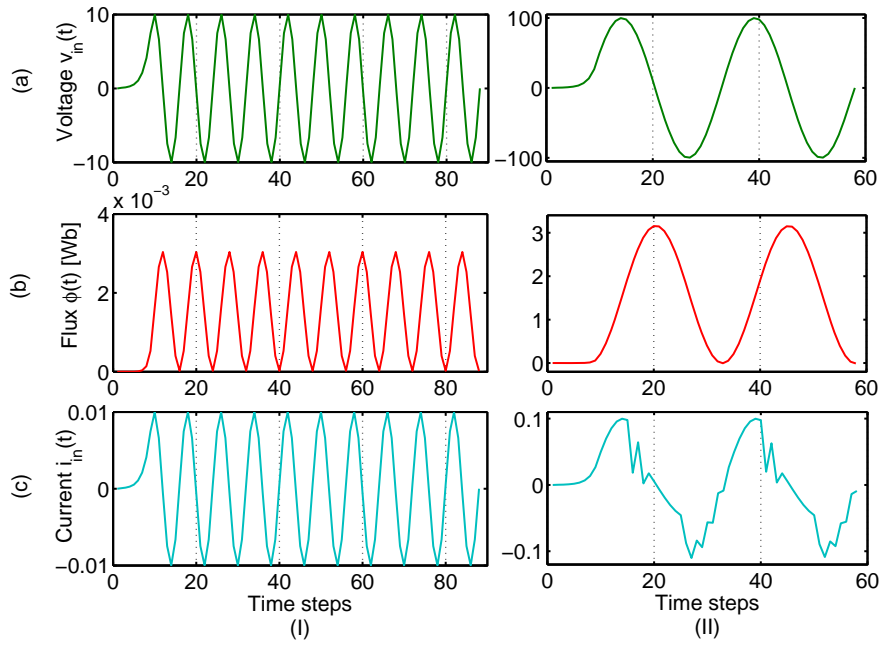
Figure 3.9. Response of the memristor to a sine voltage input. The memristor characteristics when, (I) a 1 kHz sinusoidal voltage is applied. In this case the flux does not reach to 2 Wb so $M = M_1 = 1$ kΩ and $i = 10$ mA. (II) When a 10 Hz sinusoidal voltage is applied. In this case the flux linkage reaches to 2 Wb within 30 ms, or 15 time steps. (a) Voltage curve. (b) Flux linkage curve. (c) Current curve.

Another interesting study is required to verify that the model is working properly when there is a parallel, series, RM (Resistor-Memristor), LM (Inductor-Memristor), or CM (Capacitor-Memristor) network. First of all, let us assume that there are two memristors with the same characteristic as shown in Figure 3.7. Analysing series and parallel configurations of these memristors are demonstrated in Figures 3.10(b) and 3.10(a), respectively. In both figures, the left I-V curve shows a single memristor.

The simulation results show that the series and parallel configurations of memristors are the same as their resistor counterparts. It means the equivalent memristances, M_{eq}, of a two memristor in series and parallel are $M_{\text{eq}} = 2M$ and $M_{\text{eq}} = M/2$, respectively, where M is memristance of a single memristor. The second step is RM, LM, and CM networks. In these cases a 10 V step input voltage has been applied to circuits. As mentioned before for a single memristor based on the proposed model, while the flux linkage is less than or equal to the critical flux, $\Phi \leq \Phi_c$, $M = M_1 = 1$ kΩ and when the flux is more than the critical flux value, $\Phi > \Phi_c$, $M = M_2 = 2$ kΩ. Recall that the critical flux value based on the $q - \Phi$ curve is $\Phi_c = 2$ Wb. Figures 3.11 (R), 3.11 (C),
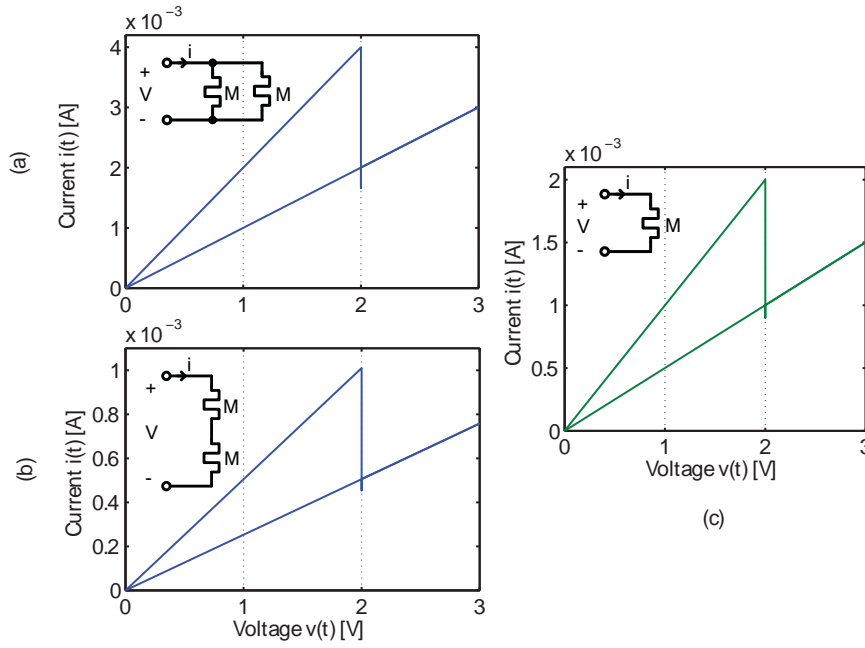
Figure 3.10. Parallel and serial connections of memristors. The I-V curves for, (a) two memristors in parallel, (b) two memristor in series, and (c) a single memristor. In all of the cases there is no difference between a memristor and equivalent resistor in the network. In other words, two memristors in parallel, with the same characteristics, form a single memristor with $M_{\text{equ}} = M_q/2$ as the memristance, and two memristors in series form a single memristor with $M_{\text{equ}} = 2M_q$ as the memristance.

and 3.11 (L) illustrate RM, CM, and LM circuits and their response to the input step voltage, respectively.

If we assume that the memristance value switches at time T_d, then for $0 \leq t \leq T_d$, $\Phi \leq \Phi_c$, and $M = M_1 = 1$ kΩ. Therefore, in the RM circuit we have, $V_M = V\frac{M_1}{R+M_1}$. For $R = 1$ kΩ, $V_M = 5$ V and then $i_M = 5$ mA, so $T_d = \frac{\Phi_c}{V_M} = 0.4$ s. Likewise, when $t > T_d$, $\Phi > \Phi_c$, we have, $V_M = V\frac{M_2}{R+M_2} = 6.7$ V and $i_M = 3.3$ mA. Both cases have been verified by the simulation results.

In the LM circuit we have the same situation, so for $0 \leq t \leq T_d$, $\Phi \leq \Phi_c$, $V_M = V = 10$ V, $i_M = 10$ mA ($R = 1$ kΩ), and $T_d = 0.2$ s. For $t > T_d$, memristor current is $i_M = 5$ mA. Memristor's current changing is clearly shown in Figure 3.11 (L). The CM circuit simulation also verifies a change in time constant from M_1C to M_2C.
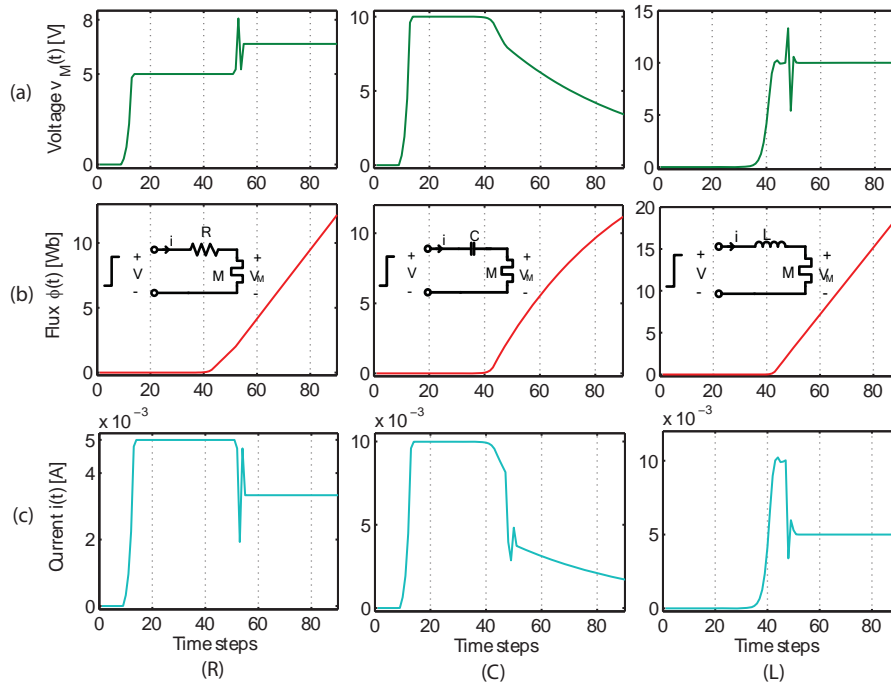
Figure 3.11. Interaction of the memristor with other fundamental elements. Step voltage response curves for (R) Resistor-Memristor, (C) Capacitor-Memristor, and (L) Inductor-Memristor. (a) Memristor voltage curve, $V_M(t)$. (b) Flux linkage curve, $\varphi(t)$. (c) Current curve, $i_C(t)$. The memristance value switches at time T_d, then for $0 \leq t \leq T_d$, $\Phi \leq \Phi_c$, and $M = M_1 = 1$ kΩ. Therefore, in the RM circuit we have, $V_M = V\frac{M_1}{R+M_1}$. For $R = 1$ kΩ, $V_M = 5$ V and then $i_M = 5$ mA, so $T_d = \frac{\Phi_c}{V_M} = 0.4$ s. Likewise, when $t > T_d$, $\Phi > \Phi_c$, we have, $V_M = V\frac{M_2}{R+M_2} = 6.7$ V and $i_M = 3.3$ mA. In the LM circuit we have the same situation, so for $0 \leq t \leq T_d$, $\Phi \leq \Phi_c$, $V_M = V = 10$ V, $i_M = 10$ mA ($R = 1$ kΩ), and $T_d = 0.2$ s. For $t > T_d$, memristor current is $i_M = 5$ mA.

As another circuit example of using the new memristor model, an op-amp based integrator was used. The transient response and circuit configuration is shown in Figure 3.12. If $C = 100$ μC then we have 0.1 s and 0.2 s as the time constant of the circuit at $t \leq T_d$ and $t > T_d$, respectively.

It is worth mentioning that, recently, a few simple SPICE macro-models were proposed by Benderli and Wey (2009), Biolek *et al.* (2009b) and Zhang *et al.* (2009), but none of their models consider the memristor interaction with other fundamental elements. Such an interaction is an important step to verify the model correctness and operation within the context of circuit network.
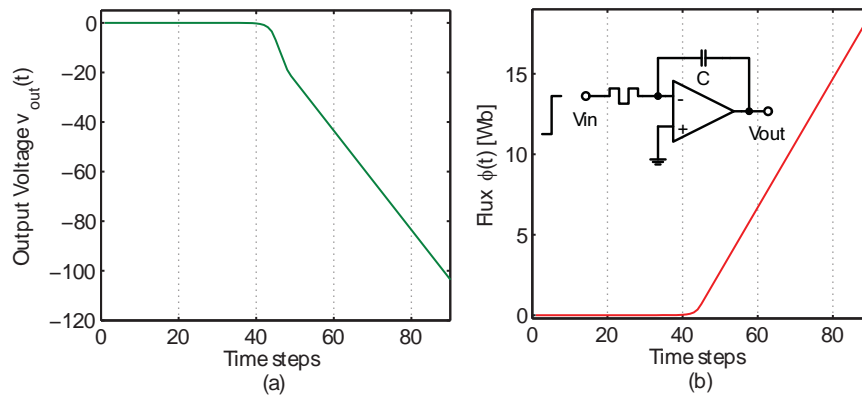
Figure 3.12. **An integrator circuit using memristor.** Memristor-op-amp integrator circuit and its response to the input step voltage. (a) Output voltage curve, $V_{\text{out}}(t)$. (b) Flux linkage curve, $\Phi(t)$. If $C = 100\ \mu C$ then we have 0.1 s and 0.2 s as the time constant of the circuit at $t \leq T_d$ and $t > T_d$, respectively.

3.5   Conclusion

This chapter provided an insight into the basic memristor model, which takes into account the characterisation of memristor and its switching behaviour. A basic SPICE macro-model was also presented and its interaction with other fundamental circuit elements and also active circuitries, e.g. operational amplifiers, are studied. Also a study of boundary impacts on the device operation and its highly nonlinear characteristics. Further detailed discussion will be presented in Chapter 5. The concept of resistance modulation index was also introduced. This index explains the resistance changes as a function of the magnetic flux that emphasises the dependency of such index to the time integral of applied voltage. Some of the important properties of the memristors were also discussed in this chapter.

Before discussing further detail on the memristor modelling and applications, it is necessary to understand underlying switching mechanism of memristive devices, fabrication processes, and applications of different materials as well as discussing some measurement results. These topics are addressed in the next chapter.

Chapter 4

Materials for Memristive Devices

MATERIALS and their properties have a strong impact on the functionality of nanometer scale devices. Different materials can be used and hence different properties can be achieved. This chapter introduces memristive materials and reviews the recent progress in the Resistive Random Access Memory (RRAM) technology. This study is important because the traditional scaling scheme cannot maintain the trend of flash memory miniaturisation. It is observed that for generations beyond 20 nm, endurance is significantly decreased due to the phenomenal increase in leakage currents. Therefore, a technological shift is almost inevitable and it is believed that RRAMs are one of the most promising emerging non-volatile technologies. During the course of this thesis, two arrays of memristors were fabricated and tested, which is reported in this chapter. The aim of this chapter is to provide preliminary information on the switching mechanism in conjunction with device fabrication and measurement.

[This page has been left blank intentionally.]

4.1   Introduction

The most attractive feature of RRAM is its compatibility with the CMOS fabrication process and materials. RRAMs are mostly low-power and have relatively simpler and cheaper fabrication process (Akinaga and Shima 2010). The processes of forming, SET, and RESET occur in unipolar and bipolar forms in these devices. The forming process acts as a soft breakdown of the oxide material. This behaviour has been observed in a variety of materials including group IV and III-V semiconductors and organic compounds (Akinaga and Shima 2010, Hayashi 1980, Sun *et al.* 2004). Figure 4.1 summarised materials that are used in RRAM devices.

This chapter's focus is on the binary metal oxides. To prevent an overloaded number of references, a review by Akinaga and Shima (2010) on the binary oxides is summarised here. This chapter consists of four sections. Section 4.2 summarises different materials and technologies. Also a comparison between available technologies for nonvolatile memories. The next section, Section 4.3, discusses a HP-like memristor that was fabricated in collaboration between our group at the University of Adelaide and the Functional Material Research group at RMIT. Section 4.4 elaborates fabrication of another type of memristors in collaboration with the Chungbuck National University, South Korea. This memristor is tested and characterised for the rest of chapters in this thesis. Finally, Section 4.5 summarises this chapter's content.

4.2   Materials

To illustrate the advantages of RRAMs, a comparison between RRAM and two major rivals, Phase Change Memory (PCM) and Spin-Transfer Torque Magnetic RAM (STT-RAM or STT-MRAM) technologies, is carried out and demonstrated in (Sekar 2010) as presented in Table 4.1. Although, MRAMs (STT-MRAMs) have shown very promising results, their complex structures made them an expensive alternative. But, PCM switching time and WRITE operation power are significantly higher than MRAMs and RRAMs resulting an overall increase in power dissipation. The major weakness of RRAM technology is its endurance. For example, by the time flash memories scale down to 20 nm or less, based on the current technology roadmap, their endurance would not be any better than today's RRAMs (*ITRS 2009).*

Table 4.1. RRAMs compared with other major emerging technologies. A comparison between three major technologies for non-volatile memory (Sekar 2010).

NOTE:
This table is included on page 54 of the print copy of
the thesis held in the University of Adelaide Library.

Oxides like Al$_2$O$_3$, NiO, TiO$_2$, TiO$_x$, TaO$_x$, CuO$_x$, ZnO, and ZnO$_2$ have been constantly used in resistive memories with different thicknesses, ranging from 2 nm up to 130 nm, and electrodes (Akinaga and Shima 2010). Optimising RRAM switching requires a deep study of different materials and also material engineering. RRAM switching optimisation can be carried out through three different steps, (i) optimising the top electrode, (ii) optimising the transition metal-oxide material, (iii) controlling (engineering) the SET current. Therefore, desirable features of the metal-oxide material can be listed as: high ionic conductivity, multiple stable oxidation states, simple and fabrication-friendly material, high Schottky barrier height, and reliability at high temperatures. The top electrode should also meet some specifications such as fabrication-friendly material, oxidation resistance, and high work function. According to recent literature, platinum (Pt) and silver (Ag) are very common (Akinaga and Shima 2010). Titanium dioxide (TiO$_2$) also shows these properties and it has been widely used for RRAM implementations (Akinaga and Shima 2010).

4.3   Pt/TiO$_2$/Pt memristor

Five different sample arrays of memristors have been fabricated during the course of this work in collaboration with the RMIT University (Guanrong 2010). In this section, a brief overview of fabrication steps is presented. Popular fabrication techniques to deposit the TiO$_2$ layer include, sputtering, Atomic Layer Deposition (ALD), and spin-on sol-gel process.

Figure 4.1. Periodic table. RRAM materials for the top and bottom electrodes as well as metal-oxides (memristive) materials. Electrodes are shown in blue colour. Binary oxides are illustrated in red and (perovskite type) ternary oxides are shown in green.

Each array contains 10×10 memristors with contact areas increasing from $20 \times 20 \; \mu m^2$ to $100 \times 100 \; \mu m^2$. Fabrication procedure starts with lithography and preparing masks for three major layers of the top and bottom Pt electrodes and middle layer of TiO_2, as demonstrated in Figure 4.2. After deposition of a 50 nm thick Pt film on a SiO_2/Si substrate using the electron beam (e-beam) evaporation system, a 50 nm thick TiO_2 film was deposited using RF magnetron sputtering as illustrated in Figure 4.3 (f). All samples contains a thin (5 nm) layer of titanium (Ti) below the top and bottom electrodes. The structure of the device without the Ti layer, $Pt/TiO_2/TiO_{2-x}/Pt$, acts like a diode with hysteresis. Therefore, an additional layer is needed to modulate the barrier height and producing oxygen vacancies at the Pt/TiO_2 interface. The structure is then like, $Pt/Ti/TiO_2/TiO_{2-x}/Pt$.

Three different TiO_{2-x} films are used for different samples. Samples (1) and (2) contain 50 nm TiO_{2-x}, where x= 0.04, while samples (3) and (4) contain two layers of TiO_2 and an oxygen deficient layer of TiO_{2-x} each 25 nm thick. Sputtering was performed on a titanium target in a reactive oxygen atmosphere to control the oxygen deficiency in the TiO_2 layer. Sample (5) has similar structure to samples (3) and (4) but the metal-oxide layer thickness is 3 nm. Due to the limited time for further analysis these samples are still under further experimental study. The results, in Figure 4.4, shows the existence

> NOTE:
> This figure is included on page 56 of the print copy of
> the thesis held in the University of Adelaide Library.

(a)   (b)   (c)

Figure 4.2. Masks for Pt/TiO$_2$/Pt memristors. The masks (a) and (c) are used for deposition of the first (top) Pt and second (bottom) Pt electrodes. The mask (b) appears black because it is continuous and is used to cover the whole array. Everything in the black region is protected from etching. Outside of the black region is TiO$_2$ is etched away in order to make space for the pads. The red dashed arrow illustrates that the Pt wires' width is increasing from 20 μm to 100 μm by 20 μm steps every second wire (Guanrong 2010).

of a $\sinh(\cdot)$ characteristics, as discussed in Chapter 5. This implies that further work is required.

According to a classification of the device operation (Kwon *et al.* 2010), three steps can be assumed: FORM, SET, and RESET. At the first step a reduction of TiO$_2$ to TiO$_{2-x}$, is required for forming. This process can be expressed as:

- **FORM**: $\text{TiO}_2 + 2x\text{e}^- \rightarrow \text{TiO}_{2-x} + x\text{O}^{2-}$.
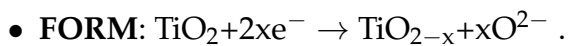
Therefore, with a change in the distribution of O^{2-} (oxygen vacancies) within the TiO$_2$ nano-layer, a change in resistance occurs. This is the first (irreversible cycle) SET operation that is known as, forming. For RESET and SET cycles then,

- **RESET**: $\text{TiO}_{2-x} + x\text{O}^{2-} \rightarrow \text{TiO}_2 + 2x\text{e}^-$
- **SET**: $\text{TiO}_2 + 2x\text{e}^- \rightarrow \text{TiO}_{2-x} + x\text{O}^{2-}$.
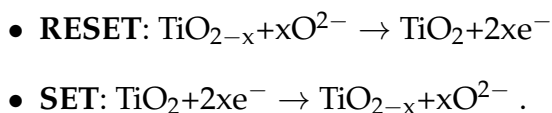
As a result of this operation, it can be understood that any material or combination of materials that has impact on the barrier height at the top electrode and TiO$_2$ interface plays a key role in the shape and uniformity of switching characteristics of the memristor device.

NOTE:
This figure is included on page 57 of the print copy of
the thesis held in the University of Adelaide Library.

Figure 4.3. Fabrication steps for Pt/TiO$_2$/Pt memristor. The cross-section view of the array. Fabrications steps include, (a) preparing the SiO$_2$/Si substrate, (b) coating photoresist, (c) the array after patterning, exposure, and development, (d) Pt deposition, (e) Pt electrodes were patterned onto the substrate by lift-off process using a rinse in acetone, (f) TiO$_2$ deposition, (g) photolithography for TiO$_2$ etching, (h) pattern the photoresist, (i) etching TiO$_2$, (j) Pt deposition and removed undesired regions by repeating the same lift-off process for the bottom electrodes (Guanrong 2010).
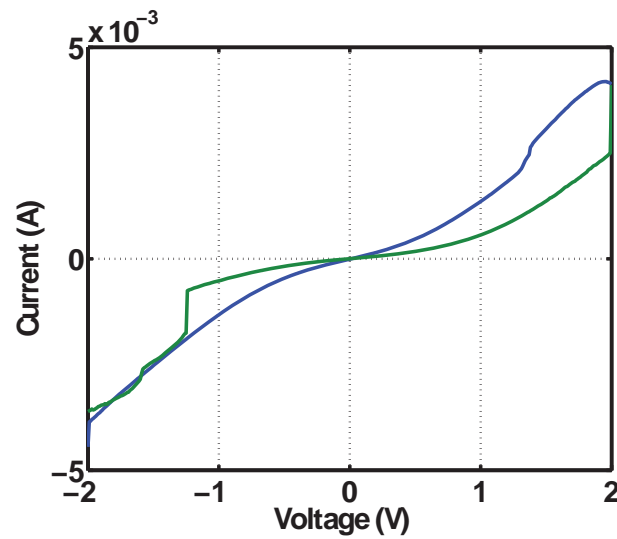
Figure 4.4. Current-voltage characteristics of the Pt/TiO$_2$/Pt memristor. The existence of *I-V* hysteresis loop. Both ON and OFF currents illustrate nonlinear characteristics of the memristive material. These measurements were carried out on a $80 \times 80 \ \mu$m^2 device from the sample (3).

4.3.1   Layer definitions for a Pt/TiO$_2$/Pt memristor

Figure 4.5 (a) illustrates a cross-section of Pt, TiO$_2$, and TiO$_{2-x}$ layers over silicon substrate. This very early fabrication is carried out in collaboration with the Korea National NanoFab Center (NNFC) at KAIST (Korea Advanced Institute of Science and Technology) (Eshraghian *et al.* 2011a). The TiO$_2$ layer thickness is restricted below two nanometers, to prevent separate conduction through the individual layers. The n-type MOS devices are patterned onto a silicon wafer using normal CMOS processing techniques, which subsequently is covered with a protective oxide layer. The Pt memristor wires are patterned and connections are made to the n-type MOS devices. The upper Pt nanowire is patterned and electrical connections made by photolithography and aluminium metal deposition (Eshraghian *et al.* 2011a). This structure was used to create a memristor-based content addressable memory structure, discussed in Chapter 8, Figure 8.8 (b).

Figure 4.5 (b) demonstrates a Transmission Electron Microscopy (TEM) microphotograph of a TiO$_{2-x}$ overlay on a silicon substrate in order to explore the controllability of oxygen ions. The device consists of a top gate Pt, TiO$_2$/TiO$_{2-x}$ layer and back gate Pt on SiO$_2$ layer of silicon. A TiO$_{2-x}$ thin film with a thickness of 9.4 nm was deposited on a silicon wafer using sputtering technique. Table 4.2 shows the deposition result with

(a) Cross section of memristor-MOS layout.

(b) TEM microphotograph.
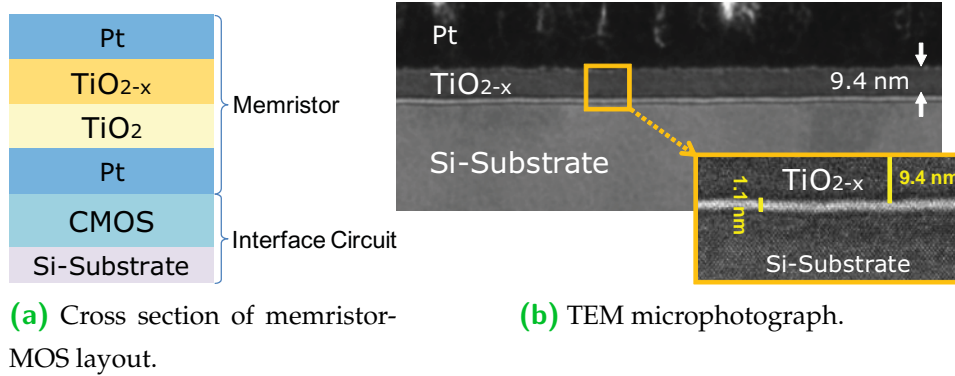
Figure 4.5. Layer definitions for a Pt/TiO$_2$/Pt memristor. A cross sectional view of the memristor-MOS implementation and Transmission Electron Microscopy (TEM) microphotograph of TiO$_{2-x}$ deposition layer. Demonstration of (a) can be better understood together with Figure 8.8 (b).

Table 4.2. Parameters for sputtering. Deposition results using sputtering technique.

	O	Ti	$O - 2 \times Ti$	$(O - 2 \times Ti)/Ti$
	%	%	Normalised	Normalised
1	66.46	33.54	-0.62	-1.85
2	66.67	33.32	0.03	0.09

sputtering technique. Samples show that a 1.85% oxygen (O) vacancy can be achieved, which is within the 2% tolerance need for this device fabrication (Xia 2011).

4.4   Ag/TiO$_2$/ITO memristor

A memristive device array for experiment and modelling purposes was fabricated in collaboration with Chungbuk National University, South Korea (Kavehei *et al.* 2011d). Experimental devices have been fabricated on a glass substrates, percolated with indium thin oxide (ITO) that has 13.7Ω/sq sheet resistance. According to Table 1 in (Akinaga and Shima 2010), this structure was not explored before. The decision to use Ag was made to obtain another top electrode with less work function (Pt 5.6 eV and Ag 4.4 eV) and less electrode potential (Pt 1.2 eV and Ag 0.8 eV) which is a fab-friendly material. The ITO was patterned using chemical wet etching to define the bottom electrode. Then, the substrate was cleaned in sequential ultrasonic baths of soap, acetone, and isopropanol alcohol for 60 minutes each. Subsequently, two layers of TiO$_2$ were deposited on the cleaned ITO substrate.

The upper TiO$_{2-x}$ layer was deposited by ALD using titanium tetraisopropoxide and O$_2$ as the precursor and oxygen source, respectively, having 5% oxygen removed. The lower TiO$_2$ formed is 2 nm thick while the upper TiO$_{2-x}$ layer formed is 20 nm thick. Finally, a 200 nm Ag layer was deposited as a top electrode that was thermally evaporated at room temperature and pressure below 10^{-7} Torr. The side schematic view of memristor together the micrograph of a fabricated device is shown in Figures 4.6 (a) and (b), respectively. When we refer to the nanoscale in the context of memristor and memristive devices we refer to the nanoscale thickness, not the feature size. Note that expounding the fundamentals of memristors and increasing the understanding of these devices is an important step at this stage. Nanoscale feature sizes may then be possible in the future as the technology matures.

(a)   (b)   (c)
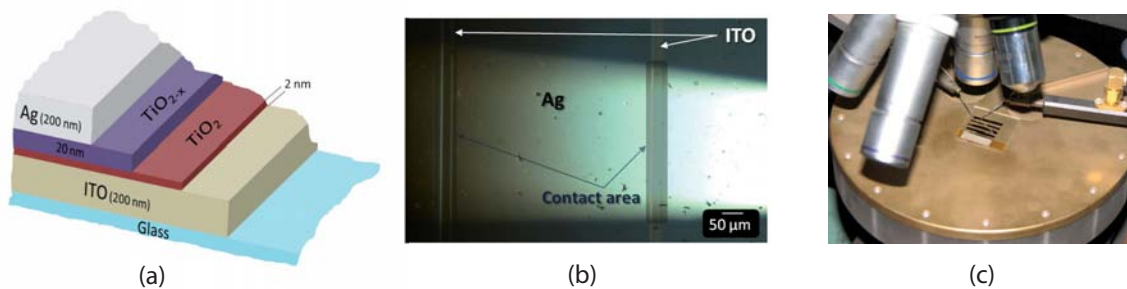
Figure 4.6. Ag/TiO$_2$/ITO memristor. Cross sectional view of a memristor device structure. (a) ITO and Ag are used as bottom electrode and top electrode, respectively, overlaid on glass substrate. (b) The fabricated memristor micrograph. Only two devices with different contact sizes are shown here. Device contact sizes vary from 32×32 μm^2 to 100×500 μm^2. (c) Illustrates a device under test.

Application of appropriate bias changes the device resistance state from a low resistance state (R_{LRS}) to a high resistance state (R_{HRS}) giving a ratio of $r = R_{\text{HRS}}/R_{\text{LRS}}$. Several tests were carried out on different devices to observe their characteristics. It is important to note that an initial irreversible electroforming process is required to activate the switching behaviour of the device under test (Miao *et al.* 2011). The non-linearity, switching behaviour, and reproducibility of a device under test are believed to be related to the forming process. We have achieved significantly higher resistances for the ON and OFF states and higher ratios. However, the functional reproducibility as well as appropriate forming process are items for future investigation. In these experiments, electric fields have been created from around 2.3 MV/cm to 6 MV/cm across devices under test to start the forming step (Kavehei *et al.* 2011d). Figure 4.7 (a)

illustrates three steps of a device's operation. In the forming step, two key phenomena are, oxygen forms at the anode (Ag) and a conductive filament with oxygen vacancies from cathode (ITO). The oxygen vacancy formation results in electron hopping from one vacancy to another. This mechanism will be discussed further in Chapter 5. An atomic Force Microscopy (AFM) image in Joshua Yang *et al.* (2009) shows oxygen bubbles for large devices and also a scan over the device surface with applied pressure increases conductivity close to the filament as shown in Figure 4.7 (e). This is due to the fact that conductive filaments act as channels that allow current to flow. Figure 4.7 (b) shows forming of the memristive device using a 5 V triangular applied voltage.

Although, RRAM's (memristor) switching mechanism is not yet fully understood but, as Figure 4.7 (a) illustrates, three major steps can be considered: (i) electroforming (FORM), (ii) OFF switching (OFF), and (iii) ON switching (SET). After the forming step, which causes a rapid ON switching, we need to break the filament for the first RESET. If the device shows bipolar behaviour, which is the case in the experiments reported here, a bias voltage with negative polarity should be applied. In this case, oxygen vacancies move toward the anode, which is the bottom electrode as it shown in Figure 4.7 (a)-(iii) and (c)-(iii). This process does not result in putting the device in its fresh mode before the forming and residual vacancies always remain, the reason for calling the forming process an *irreversible process*. A virtual anode is then created that makes the next switching possible with much less electric field became the travel distance for the vacancies is now much shorter. A deep study is required on the filament density for a given device area but it is possible to roughly claim that the minimum contact area of a RRAM device can be as small as a filament diameter. However, in practice this is not possible and it is likely that tunnelling can occur between neighbouring cells. Therefore, there are many filaments but most of them are partial filaments as it is illustrated in Figure 4.7 (d).

The RESET process can be alternatively discussed as breaking the filament at the top electrode and TiO_2 interface. The mechanism is a heat-assisted electrochemical reaction. The reason came from the fact that a high RESET current passing through a tiny filament diameter (3 nm to 10 nm) results in a huge current density and as the consequence a high temperature. This process breaks the filament and creates a virtual anode electrode as shown in Figure 4.7 (a)-(iii). Therefore, the Schottky barrier height at the interface between the top electrode and TiO_2 breaks which results in a significant change in conductance that is called, OFF switching. In fact, oxygen vacancies at

the interface reduce the effective barrier height, so when TiO$_{2-x}$ converted to TiO$_2$, the barrier height increases (Joshua Yang *et al.* 2009). The SET mechanism is similar to the forming process but with a smaller required electric field. The barrier height modulation and oxygen vacancies produced at the interface can result in current change from the nA to mA range (Yang *et al.* 2008).

NOTE:

This figure is included on page 62 of the print copy of the thesis held in the University of Adelaide Library.
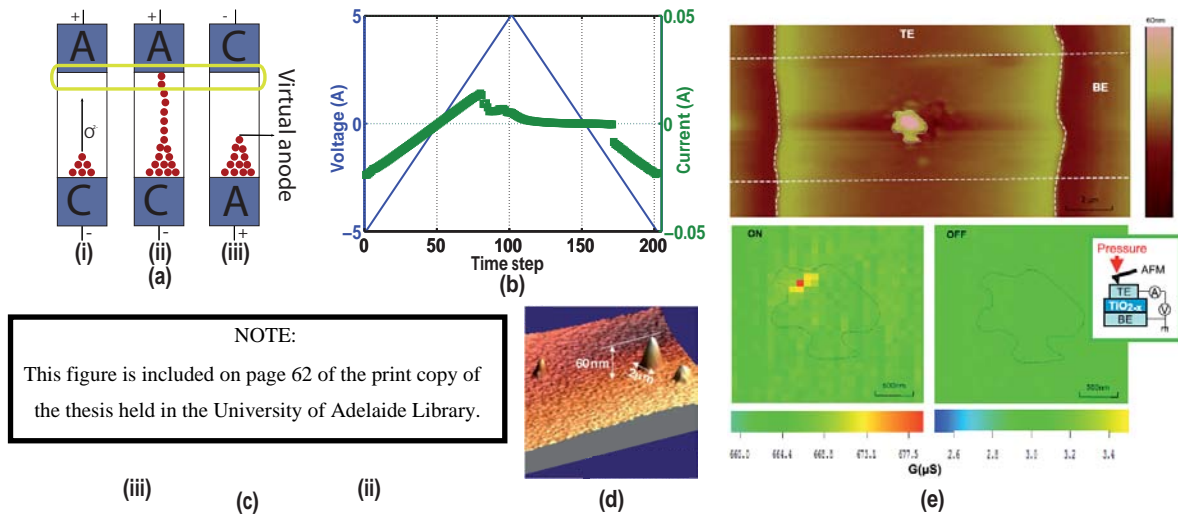
Figure 4.7. Forming and switching mechanism. Memristive device operation and forming. (a) demonstrates three steps of FORM, RESET, and SET in (i), (ii), and (iii), respectively. Here A indicates anode and C stands for cathode. (b) Shows experimental results of the first switching cycle for a Ag/TiO$_2$/ITO device using a 5 V voltage sweep. (c) shows evidence for the existence of the filament between the anode and the cathode from Kwon *et al.* (2010) using TEM after switching. (c)-(ii) and -(iii) are correspond to (a)-(ii) and -(iii), respectively. The red lines show the filament in the solid electrolyte material. The figure (d), from Joshua Yang *et al.* (2009), illustrates further evidence taken from an Atomic Force Microscopy (AFM) image detecting oxygen bubbles with the hight of 60 nm and diameter of 2 μm for devices with large contact area. The figures in (e) are adapted from Joshua Yang *et al.* (2009) which shows that local pressure using AFM tip modulates conductance.

Two control mechanisms should exist for getting a desirable *I-V* characteristics from the fabricated memristor, time and voltage (or current). A closer look at the reported *I-V* curve in Figure 4.8 shows that a series of voltage pulses with magnitude of $+0.5$ V and -0.85 V result in reliable switching at low voltage. A series of 500 pulses were applied across a device from the fabricated memristor array during three continuous days. The device showed a good functional uniformity for the ON and OFF switching thresholds, R_{LRS}, and R_{HRS}. Despite this successful experiment, the process to control

electroforming step, to result in an uniform functionality, is not well described in the literature (Joshua Yang *et al.* 2009). This consideration motivated us to test the idea of asymmetric applied electric field to obtain improved functionality out of the devices. A better idea to improve the uniform functionality is to eliminate the forming step, a successful demonstrations have already shown different possibilities (Kwon *et al.* 2010, Joshua Yang *et al.* 2009).
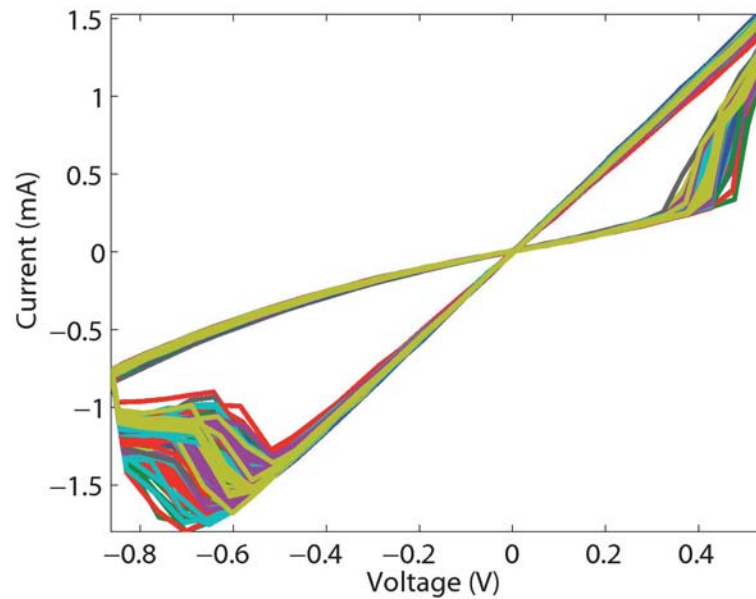
Figure 4.8. Current-voltage characteristics of the Ag/TiO$_2$/ITO memristor. *I-V* curve measurements of the Ag/TiO$_2$/ITO memristor using a time-domain measurement using Keithley 4200-SCS semiconductor parameter analyser and its pulse module, ie. Pulse Measurement Unit (PMU).

4.5   Conclusion and potential extensions

A review on the materials and the emerging technologies is given in this chapter. Two memristive devices fabricated in the course of this project are demonstrated and related fabrication steps and measurement results are discussed. It is also explained that how a metal-insulator-metal can be optimised using different materials and for obtaining the best possible properties for such a structure. At the same time, the structure should be compatible with current CMOS technologies. The two memristor structures satisfy the compatibility. The second memristor, Ag/TiO$_2$/ITO, contains a unique structure among the fabricated memristors so far and its properties show a uniform bipolar switching mechanism with a control on the voltage magnitude in positive and

negative regions. Measurement and experimental results from this chapter is the base to provide a better SPICE modelling approach for the circuit and system applications.

The next chapter discusses SPICE modelling of memristive devices based on a TiO_2 memristor. The following chapter also demonstrates the model against measurement results using the fabricated devices from this chapter. It also introduces the first set of simulations for complementary resistive switches (CRSs).

Chapter 5

Memristive Macromodel and SPICE Implementation

SPICE implementation of a memristor model is the key for enabling circuit designers to work on memristive-based circuits. This chapter provides modelling approaches for memristors and reviews memristor model progression. It also introduces modelling principles, verified through measurements, to extend the memristor circuits by exploiting two memristive devices in series, which forms a new memristive-type integrated device. Verification of this unique structure using simulation and experimental measurement are provided in this chapter.

[This page has been left blank intentionally.]

5.1 Introduction

The memristor and its fundamental behaviour are now among the most promising candidates for delivering a significant advantage for constructing an adaptive nanoscale Cellular Neural Network (CNN) (Chua 2011). As this nanoscale device enables the introduction of new on-chip computation, which is promising for the future of Artificial Intelligence (AI) (Kavehei *et al.* 2011b). One of the very first steps toward this vision is in providing a device model that is compatible with commonly accepted design modelling packages such as SPICE.

This chapter discusses modelling of memristor and memristive devices. The memristor device is a TiO$_2$ type memristor and the memristive device we consider consists of two memristor devices connected in series with opposite polarity. Section 5.2 describes the basic modelling approach consisting of a variable resistor and switching behaviour. Available models and the progression of memristor modelling is discussed in Section 5.3. Proposed model for memristor dynamic behaviour and *I-V* characteristics are explained in Section 5.4. This section includes a comparison between available models and also highlights analogue behaviour of the proposed model. Section 5.5 compares the model against measurement results from the fabricated memristors. This chapter also includes a modelling approach for complementary resistive switches and related measurement, which are discussed in Section 5.6.

5.2 Memristor modelling and characterisation

This section provides a brief review of models available in the community and introduces a new model as well as its verification. This section, is primarily concerned with the development of simple models that will assist in understanding a memristor-based circuits and system behaviour by providing the basis whereby system performance, in terms of signal delays and power dissipation, can be estimated. Here, analytic and empirical models that describe the switching characteristics of a memristor are developed. These models continue to be of use to understand the parameters that affect memristor behaviour. More detailed analysis and simulation are necessary to yield models that accurately predict the performance of today's memristor technologies.

Strukov *et al.* (2008) introduced a physical model whereby the memristor is characterised by an equivalent time-dependent resistor, whose value at a time t is linearly

proportional to the quantity of charge q that has passed through it. This proof-of-concept implementation consists of a thin nano layer (2 nm) of TiO_2 and a second oxygen deficient nano layer of TiO_{2-x} (3 nm) sandwiched between two Pt nanowires, as shown in Figure 5.1. A change in distribution of the vacancies within the nano layer changes the resistance by a tunnelling mechanism through the TiO_2 layer to Pt (Pickett *et al.* 2009).

The device conductance then will change by applying either a positive or negative voltage. As shown in Figure 3.4, by considering tunnelling as the dominant physical mechanism (Waser and Aono 2007), l introduces the initial tunnelling barrier width, which is bounded by a maximum (x_{max}) and a minimum (x_{min}) values, commonly referred to as *state index position*, x. The difference between x_{max} and x_{min}, $l = x_{max} - x_{min}$, is referred to as initial barrier width. As an example, based on the HP measurement (Pickett *et al.* 2009), when $x_{max} = 19$ Å and $x_{min} = 11$ Å, the initial tunnelling barrier width in the TiO_2 layer is 8 Å. In order to promote consistency between the first description of the fabricated memristor and the tunnelling concept, we assign the memristor state as a normalised variable. The approach results in a normalised parameter that indicates the internal memristor state $w = (x_{max} - x)/l$. The barrier position can move from $x_{off} = 18$ Å ("OFF" state) down to $x_{on} = 12$ Å ("ON" state). This results in 0.12 and 0.88 boundaries of the normalised state variable, w, for "OFF" and "ON" switchings, respectively. Interestingly, this piece of the puzzle confers a physical interpretation upon the position of the normalised state variable published in Szot *et al.* (2006), leading to the expected current limits for a 10 nm thin $SrTiO_3$/Pt device.

Application of Ohm's law to Figure 5.1 (c) results in $V = (R_S + R_V)i$. If θ is the resistivity of the TiO_2 region and A is the contact area, then $R_V = \frac{\theta}{A}(x_{max} - x)$, from which we obtain, $\frac{dx}{dt} = -\frac{A}{\theta}\frac{dR_V}{dt}$. Thus, $\frac{dx}{dt} = \frac{A}{\theta G_V^2}\frac{dG_V}{dt}$, where G_V illustrates the variable conductance. In other words, the rate of change in the device conductance is a strong function of the rate of change in the position of the barrier and initial conductance. Therefore, memristor can be treated as a finite state machine. If a uniform distribution of particles and applied electric field (uniform applied force on each particle) is assumed, a factor called the *conductance modulation index* (Kavehei *et al.* 2010) can be shown to follow from the very first HP memristor model.

By applying a positive voltage, to the top platinum nanowire, oxygen vacancies drift from the TiO_{2-x} layer to the TiO_2 undoped layer, thus changing the boundary between

the TiO$_{2-x}$ and TiO$_2$ layers. As a consequence, the overall resistance of the layer is reduced accordingly till it reaches an "ON" state. When enough charge passes through the memristor that ions can no longer move, the device enters a hysteresis region and keeps q at an upper bound with fixed memristance, M (memristor resistance). By reversing the process, the oxygen defects diffuse back into the TiO$_{2-x}$ nano layer. The resistance returns to its original state, which corresponds to an "OFF" state. The significant aspect to be noted here is that only ionic charges, namely oxygen vacancies (O^{2-}) through the cell, change memristance. The resistance change is non-volatile hence the cell acts as a memory element that remembers past history of ionic charge flow through the cell.
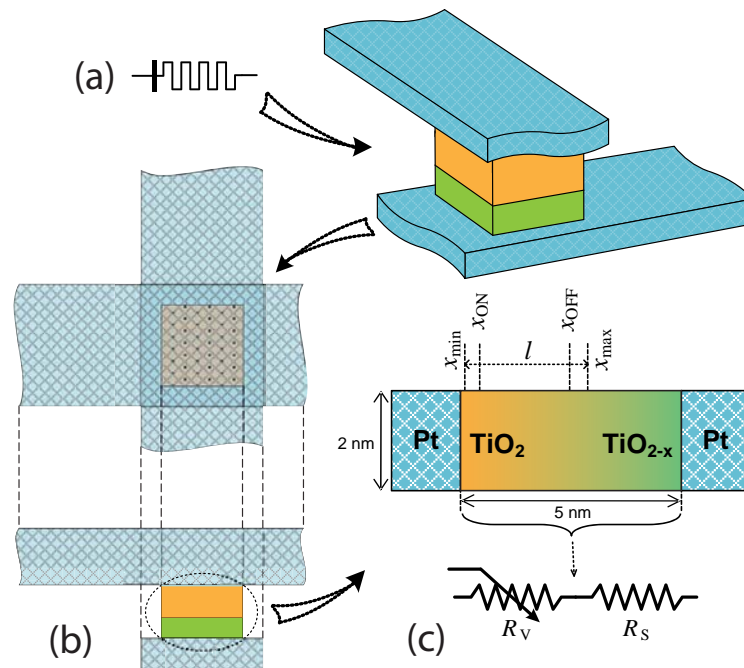
Figure 5.1. Memristor's physical representation. Physical representation of memristor. (a) Memristor symbol and a 3D view of the Pt/TiO$_2$/Pt structure, (b) Top and side cross sections of the structure, (c) Switching behaviour of the memristor, whereby "doped" and "undoped" regions correspond to R_{on} and R_{off}, respectively, being the two extreme states for the variable resistance R_V. The R_S is a series resistor around 200 Ω (Pickett *et al.* 2009). The dopant consists of mobile charges. Assuming the tunnelling (Waser and Aono 2007), l introduces the initial (maximum) tunnelling barrier width, bounded by two extremes (x_{max}) and minimum (x_{min}) possible positions, x indicates the position of the tunnelling barrier. As an example, with $x_{max} = 19$ Å and $x_{min} = 11$ Å, we have $l = 8$ Å. At the same time, x_{off} and x_{on} are 18 Å and 12 Å, respectively.

Despite the current progress, modelling is still in its embryonic stage of development. A good model, however, builds upon a sound understanding of the underlying fundamental principles that facilitates related formulations into a mathematical or behavioural form. The very first step is to prepare a SPICE-like model that can mimic the behaviour of a memristive device. A memristor structure is created by forming a Pt/TiO_2-TiO_{2-x}/Pt layers. Each layer and the boundary display a particular behaviour that is critical in estimating the performance of a circuit or a system. There are a number of approaches that aim to model the memristor behaviour (Prodromakis *et al.* 2011).

5.3   Progression of memristor modelling

Available memristor or memristive device models attempt to characterise both current-voltage behaviour and the device dynamics. As already mentioned in this chapter, a number of memristor models have been introduced. However, only a few address the highly nonlinear nature of the device. It would be useful to review successful models thus far and this section compares them from different point of views. The "normalised" dynamics of a memristive device can be described as the rate of change in the position of state variable w, which over time can be written as

$$\frac{dw}{dt} = h(w, X_M) \, , \tag{5.1}$$

where $h(\cdot)$ is a function of the state variable. Either memristor current (i_M) or voltage (V_M) facilitate rate of change in the device resistance (or conductance) and the rate of change of memristance (or memductance) (Chua 1971, Chua and Kang 1976). A simplified and practical example of a memristor model is $h(w, i_M) = \alpha \cdot i_M$, where α is a constant that depends on device parameters such as the device thickness, carrier mobility, and initial resistance (Strukov *et al.* 2008), hence, the memristor device dynamic is linearly related to i_M. Basically, there is an initial irreversible manufacturing process that is called "electroforming", which is responsible for the dynamic characteristics of the memristive devices. On the other hand, during the electroforming process, the device behaviour is transferred from a static resistor to a dynamic memristor by applying a relatively high voltage or current (Joshua Yang *et al.* 2009, Kim *et al.* 2010). In fact, the existence of different forms of *I-V* curves depending on the position of the filament, according to Kim *et al.* (2010), is another evidence for the existence of a joint mechanism of tunnelling and ballistic conduction.

Available models apply a number of techniques to describe the nonlinear dynamics of the memristor device. These approaches can be simplified in the form of:

$$\frac{dw}{dt} = \alpha \cdot f(w) \cdot i_{\mathrm{M}} \, , \tag{5.2}$$

where $f(w)$ is a normalised nonlinear function of the form $1 - (2w - 1)^{2p}$, commonly referred to as a *window function*, as in Eq. (3.19).

The limitation in adopting the window function is its boundary conditions, whereby one has to ensure that there is little or no change in the memristance when w approaches the boundaries (0,1 states for normalised w), $f(w \to \text{boundaries}) \approx 0$ (Eshraghian *et al.* 2011a). This condition implies an infinite state at the boundaries, identified as a *hard switching* condition (Kavehei *et al.* 2010). The second problem with using such a window function is the highly nonlinear behaviour, obtained at high values of p, changes the exponential nature of the reported relationship (Pickett *et al.* 2009), with the direct relation that exists between the dw/dt and $f(w)$. It deploys the same behaviour pattern for both $0 \rightleftharpoons 1$ transitions, which may not be the case based on recent experimental results for ON and OFF switching (Kavehei *et al.* 2011d). The nonlinearity created by the window function does not appear to comply with presently known physical phenomena. These asymmetries between ON and OFF switching speeds and also the rate of the state variable change toward ON and OFF imply an exponential relationship between initial conductance level and the rate of conductance change (Kavehei *et al.* 2011d). These limitations are associated with other types of window functions, such as $1 - (w - \text{stp}(-i_{\mathrm{M}}))^{2p}$ (Biolek *et al.* 2009b), where the $\text{stp}(\cdot)$ function can be either 0 or 1 depending on the current signature, $\text{stp}(z) = 1$ if $z \geq 0$ otherwise $\text{stp}(z) = 0$. As a consequence, these models continue to have some limitations in modelling the device as they do not allow for a consistent prediction of the memristor behaviour when compared with experimental results. Additionally, a $\sinh(\sqrt{V})$ like behaviour has been observed between the rate of change of differential conductance and the applied voltage at low electric field relative to the tunnelling barrier width (Kavehei *et al.* 2011d).

Generally, the common problem in these models is that there is no threshold consideration, so there is a gap in the knowledge-base for design characterisation. Nonetheless, the models (Strukov *et al.* 2008, Biolek *et al.* 2009b, Joglekar and Wolf 2009) confirm the behaviour of HP's memristor. However, Lehtonen and Laiho (2010) introduced a new

model using the window function of Eq. (5.2). The main advantage of this model is that it provides a programming threshold by using a nonlinear function $g(\cdot)$, which is a function of the applied voltage V. The model is described by:

$$\frac{dw}{dt} = \alpha \cdot f(w) \cdot g(V) \, . \tag{5.3}$$

They concluded that to mimic the behaviour of the memristor reported in Yang *et al.* (2008), the $g(\cdot)$ term must be a nonlinear, odd, and monotonically increasing function. Considering the basic memristor properties discussed in Chua (1971), and Chua and Kang (1976), the memristor experimental data, and some of the mathematical approaches from the literature (Pershin *et al.* 2009, Linares-Barranco and Serrano-Gotarredona 2009), these features must be met in any memristive device modelling. It must also meet the zero-crossing requirements of the memristor device, $g(V \to 0) \to 0$.

Several options are possible, such as $g(V) = V^{2j-1}$, where j is a positive constant, and $g(V) = c_a \cdot \sinh(c_b \cdot V)$, where c_a and c_b are two constants that depend on device characteristics and experimental results, comparable to that in Yang *et al.* (2008). Applying a highly nonlinear $g(\cdot)$ automatically yields a programming threshold voltage. However, applying this nonlinearity has never been linked to a physical phenomenon in the modelling context. It is important to note that the models show similar speed for ON and OFF switching, which seems to be not the case based on the experimental results reported in Pickett *et al.* (2009).

Another model introduced by Linares-Barranco and Serrano-Gotarredona (2009) is:

$$h(w, V_M) = \begin{cases} A \cdot \text{sign}(V_M)\left(e^{\frac{|V_M|}{V_0}} - e^{\frac{V_t}{V_0}}\right) & : |V_M| > V_t \\ 0 & : \text{otherwise} \, , \end{cases} \tag{5.4}$$

where $\text{sign}(\cdot)$ is the signum function and the A and V_0 parameters can be dependent on, or independent of the normalised state variable, w. This model describes the ideal behaviour of a memristor in its OFF mode by taking $dw/dt = 0$ for an applied voltage that is less than the threshold, V_t. This, however, is not a realistic condition as the memristor state can change, if $V_M \le V_t$ is retained for sufficient time (Kavehei *et al.* 2011d).

A piecewise modelling approach was reported in Pershin *et al.* (2009). The reported function is interesting because it is a strong function of the rate of change in memristor's resistance (memristance, M), dM/dt, which is the approach that we have taken in introducing our proposed model.

5.4   Proposed model for memristor dynamic behaviour

The conduction mechanism of metal-insulator-metal (MIM) (or more strictly, metal-resistor-metal (MRM)) structures can be assumed to be based on tunnelling (Yang *et al.* 2008, Miao *et al.* 2009, Stewart *et al.* 2004, Shkabko *et al.* 2010). Simmons (1963) introduced a model that describes the *I-V* characteristics of MIM structures, based on Simmons tunnelling theory. In the modelled device, depicted in Figure 5.2, the conductance, G, is shown as function of the barrier width based on Simmons theory that is in agreement with the experimental results reported by Miao *et al.* (2009). The conductance model is described by:

$$G = \frac{q^2}{4\pi h} \frac{A}{L^2} (\rho \varphi_0 - 2) e^{(-\rho \varphi_0)} \,, \tag{5.5}$$

where q is electron charge, h is Planck's constant, φ_0 is the equilibrium ($V \to 0$) barrier height in eV, ρ is the equilibrium shape factor in eV^{-1}, A is the contact area in μm^2, and L is the energy barrier width (Vilan 2007). The barrier width, L, can be taken as a function of the state variable, x, $L = x - x_{\min}$, where $x \in [x_{\text{on}}, x_{\text{off}}]$, or as a function of the normalised state variable, w, $L = l(1 - w)$, where $w \in (0, 1)$. The shape factor parameter can be related to L using $\rho = \beta_0 L / \varphi_0$, where β_0 is the tunnelling constant (decay parameter) in Å^{-1}, that is presented in a form of normalised state variable $w = 1 - (x - x_{\min})/l$. The resistance of such devices as a function of w presents an exponential behaviour $R \propto e^{(1-w)}$ (Hasegawa *et al.* 2010).

This approach leads to a more in-depth understanding of the underlying mechanism of the memristor dynamics and enables us to better understand the behaviour of physical parameters that are involved. Furthermore, the $\sinh(\sqrt{V})$-like behaviour at low electric fields, according to measurements and reported model in Blanc and Staebler (1971), and the complexity of the available model, in Pickett *et al.* (2009), motivates us to explore a different approach. The exponential form of the conductance in Eq. (5.5) is consistent with the behaviour of characteristics a modified Simmons relation in Vilan
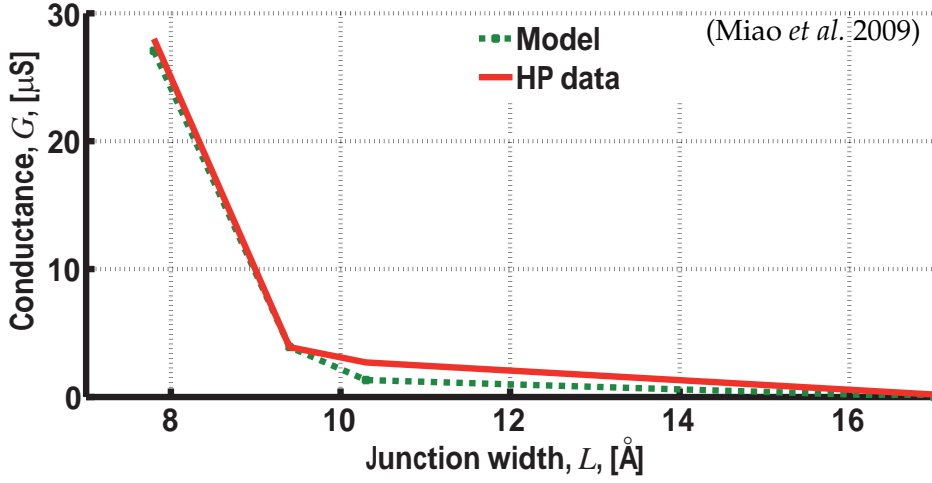
Figure 5.2. Exponential relation between memristor's conductance and junction width. Device conductance, G, in μSiemens (μmho), as a function of junction width, L, in Angstroms. A highly nonlinear change in conductance of the device can be observed based on Simmons theory of tunnelling, Eq. (5.5), which confirms the experimental results shown in Miao *et al.* (2009).

(2007). Therefore, we apply a new $g(\cdot)$ function as follows:

$$g(V, \rho(w), \varphi_0) =$$
$$\left(1 - \frac{V}{2\varphi_0}\right) \exp\left(\rho(w)\varphi_0\left(1 - \sqrt{1 - \frac{V}{2\varphi_0}}\right)\right)$$
$$- \left(1 + \frac{V}{2\varphi_0}\right) \exp\left(\rho(w)\varphi_0\left(1 - \sqrt{1 + \frac{V}{2\varphi_0}}\right)\right). \quad (5.6)$$

The core part[12] of Eq. (5.6) is based on the assumption that in, an asymmetric trapezoidal barrier, the averaged potential, $\overline{\psi}(V) = (\psi_{\text{left}} + \psi_{\text{right}})/2 = \psi_0 + V/2$, there is an asymmetry between the barrier heights at the left and right end of the barrier. However, such asymmetry can be ignored when the applied bias is less than the maximum barrier heights (Vilan 2007). The Eq. (5.6) describes the behaviour of the state variable based on the exponential terms for ON and OFF switching similar to that reported by HP (Pickett *et al.* 2009). From Eq. (5.5) we have that the effective barrier width L is proportional to $1 - w$. Therefore, if $w \to 0$ results an OFF device whereas if $w \to 1$ results an ON switch. Thus, the two exponential parts charge and discharge a capacitor, C, in

---

[12]Similarity of the term $\sqrt{1 - \frac{V}{2\varphi_0}}$ when compared with RMI term in Eq. (3.16) highlights the relation between the modulation index and characterisation of the memristor dynamics.

the SPICE model. This capacitor carries out integration process to achieve w. According to the Kirchhoff's circuit laws $\frac{dw}{dt} = \frac{i_{charge} - i_{discharge}}{C}$, where i_{charge} and $i_{discharge}$ are the exponential terms in Eq. (5.6) and in the forms of $G_{V,ON}$ and $G_{V,OFF}$ in Table 5.1.

In this case there is no need for using a window function, $f(w)$, and the rate of change of the state variable, dw/dt, will be linearly related to the tunnelling phenomenon, which appears to be the case for a memristor [13]. Therefore, Eq. (5.3) can be rewritten as

$$\frac{dw}{dt} = \nu \cdot g(V, \rho(w), \varphi_0) \,, \tag{5.7}$$

where ν is a constant value to identify ON and OFF switching speeds in a normalised distance ($w \in (0,1)$) based on experimental results (Strukov and Williams 2009a, Pickett *et al.* 2009). It has been observed that ON switching is much faster than OFF switching in a memristive device. The most interesting part of the model is that several thresholds, can be programmed by tuning the shape factor, which can also be tuned for a certain range of voltages. It is instructive to note that the $g(V, \rho(w), \varphi_0)$ contains two exponential parts that can be used in symmetric or asymmetric fashion for negative and positive voltages. Figure 5.3 illustrates the proposed model response to a 1 MHz sinusoid voltage across the device. The normalised state variable, w, is limited to a maximum of 0.95 and minimum of 0.05 and an initial state of 0.95 is assumed. These limits can be modified based on experimental results, where the ON and OFF state limits can be extracted as $w_{on} = 0.88$ and $w_{off} = 0.12$, respectively, using the available data in Pickett *et al.* (2009). These limits guarantee that the model operation is always within the memristive regions (Shin *et al.* 2010). Furthermore, there is a threshold around $V_t = \pm 1.7$ V.

Based on the definition, the shape factor parameter, ρ, linearly depends on the tunnelling junction width, L. This relation causes a high nonlinearity in one of the boundaries and low nonlinearity on the other and also the function can be unnormalised. To address this issue and formulate a more robust model, we introduced $\rho(w)$ as a new shape factor function defined as:

$$\rho(w) = \delta + \eta(1 - (2w - 1)^{2p}) \,, \tag{5.8}$$

---

[13]The window function can be used to control the exponential nonlinearities at the boundaries by applying lower values to the shape factor, $\rho(w)$, at the boundaries. In fact, the double exponential relation between the tunnelling barrier width and device dynamics equation in Pickett *et al.* (2009) can be modeled as a highly nonlinear polynomial equation, introduced by Eq. (5.8).

where δ is an offset (positive) constant and it should be adjusted to retain the monotonically increasing condition for Eq. (5.7), η is a positive coefficient to control the $\rho(w)$ nonlinearity. The $1 - (2w - 1)^{2p}$ part is a normalised-nonlinear function, which describes the nonlinear conditions at the boundaries. Introducing this polynomial form in Eq. (5.6) approximate the double exponential form of the velocity equation in Pickett *et al.* (2009). Implementation of this equation in SPICE will not result in a robust model and contains convergence and current overflow problems of small scale array can arise. The SPICE (Mentor Graphics Eldo, PSPICE, or LTSpice) implementation of our model as a sub-circuit is shown in the Table 5.1.

The current-voltage curve, using the model introduced by Yang *et al.* (2008), can now be described by the following equation:

$$i_{\mathrm{M}} = w^n \varkappa \sinh(\vartheta V_{\mathrm{M}}) + \chi (\mathrm{e}^{(\gamma V_{\mathrm{M}})} - 1) , \qquad (5.9)$$

where $\varkappa$ and ϑ are fitting parameters for characterising the ON state, which is essentially based on electron tunnelling through a barrier (Supplementary material in Yang *et al.* (2008)). In the second term, χ and γ are used as fitting parameters to characterise net electronic barrier for the OFF state. Using the proposed model for the state variable it confirms that w is proportional to the history of applied voltage, which is equivalent to the magnetic flux from Faraday's law. The first term of Eq. (5.9) is controlled by the exponent n. Therefore, the nonlinearity between the drift velocity and the ON switching current can be controlled by applying n as a fitting parameter. It can be concluded that the first modelling approach introduced by Strukov *et al.* (2008) is a special case of this particular relation where $n = 1$. Figure 5.4 demonstrates the difference between the two current curvatures, for $n = 1$ (linear HP model) and $n = 4$ (used for this work).

To identify shape factor, ρ, and equilibrium conductance, G_0, from experimental data it is important to have a polynomial approximation for the *I-V* curve and $dI_M/dV_M|_{V_M \to 0}$ information. The equilibrium barrier height is usually reported based on the measurements and it can be found in some of the recent works (Miao *et al.* 2009). There are a good range of available data for G_0 and also impact of temperature on the memristor internal state (Miao *et al.* 2009, Borghetti *et al.* 2009).
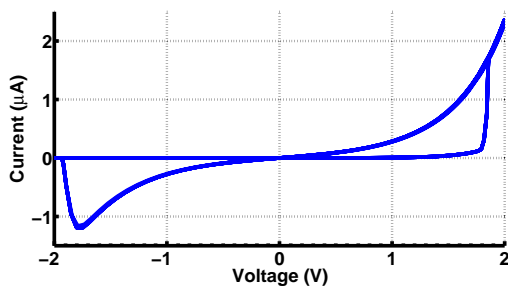
(a) Hysteresis *I-V* curve using the proposed model for the memristor dynamics.
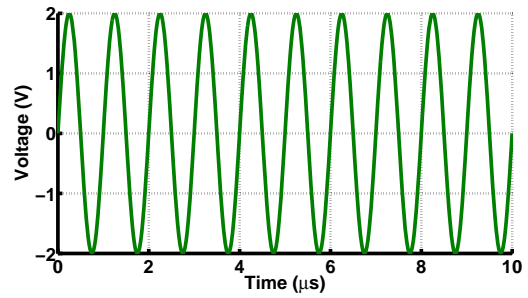
(b) A 2 V, 1 MHz sinusoidal voltage is applied.
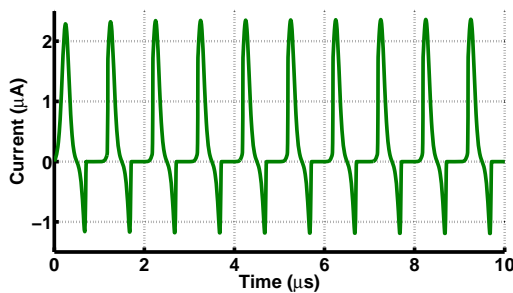
(c) The highly nonlinear memristor current.
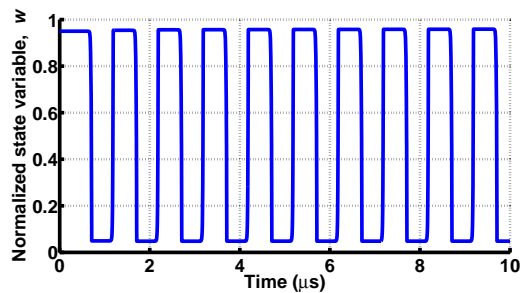
(d) Normalised state variable, between 0 and 1.

Figure 5.3. Proposed model under test. Memristor compact model response to a 1 MHz sinusoid applied voltage. (a) The current-voltage characteristic, shows the existence of a threshold voltage around 1.7 V for an applied voltage of 2 V. The plots in (b) and (c) illustrate the applied voltage and memristor current as a function of time. (d) The normalised state variable, shows switching between 0 and 1 states. Lower values imply proximity to the OFF state and higher values indicate a more conductive device. Basically, a memristor in its digital (binary) regime acts as a two-state device with high and low regions for ON and OFF states, respectively.

A possible way of characterising a memristive *I-V* curve is to plot the relation on a log-log scale. Using this approach the curve will yield two functional (fitting) parameters, *a* (*c*) and *b* (*d*). Basically, this can be considered as another signature of high nonlinearity at the boundaries and one way to characterise different implementations of memristors. Figure 5.5 depicts an *I-V* curve on its log-log scale (Choi *et al.* 2009).

5.4.1   Comparison of models

Table 5.2 summarizes the comparison between different available models. The four models provide the threshold programming and SPICE-like model, are V^{2j-1},
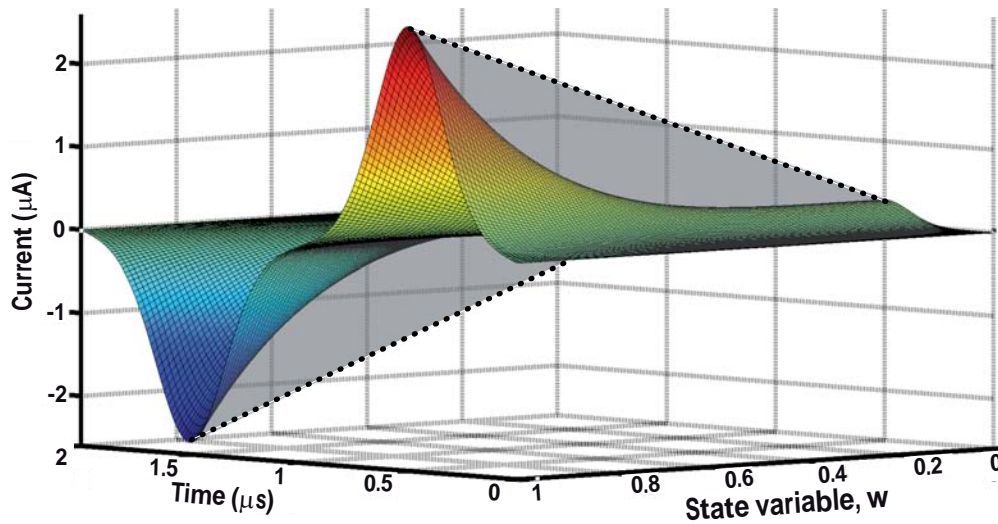
Figure 5.4. Investigating the impact of the parameter n on the nonlinearity. The memristor current, i_{M}, in Eq. (5.9) as a function of time and normalised state variable, w, in response to a sine input voltage. The gray scale curve, which its curvature is highlighted by a dashed line, shows how Eq. (5.9) can mimic the linearity of the model proposed in Strukov *et al.* (2008) by applying $n = 1$. The colored curve, on the other hand, illustrates a highly nonlinear behaviour of this current when $n = 4$.

NOTE:
This figure is included on page 78 of the print copy of
the thesis held in the University of Adelaide Library.

Figure 5.5. Proposed model I-V characteristics in a log-log scale. The memristor I-V curve on a log-log scale linearizes the current as a function of applied voltage. In this case the current-voltage curve can be rewritten as a polynomial function, $i_{\mathrm{M}} = k_1 V_{\mathrm{M}} + k_2 V_{\mathrm{M}}^2$, where x_1 and x_2 are fitting parameters. This graph shows that switching occurs when the memristor current is highly nonlinear. In other words, at the boundaries a highly nonlinear behaviour is observed. Due to the limitation of facilities, the state variable measurements were done using I-V curve as a signature through an iteration of programming by V pulses and measuring I (Kavehei *et al.* 2011d).

$\sinh(c_b V)$, (Pickett *et al.* 2009), and this work. Our proposed model is the only approach that addresses programming threshold, SPICE-friendly approach, adaptation of Simmons theory of tunnelling, and the memristive operation regime limits. Our approach significantly improves the robustness of SPICE implementation in terms of convergence and overflows for i_{charge} and $i_{\text{discharge}}$. The model in Pickett *et al.* (2009) suffers from convergence and current overflow problems in SPICE implementation form, therefore, it is extremely sensitive to the applied signal (Abdalla and Pickett 2011).

Trimming is another important factor in comparing the models. Basically, a model without limits for the state variable may introduce complexity with convergence in SPICE-like simulators and furthermore the modelled device most likely will violate the boundary conditions (Shin *et al.* 2010). Only four of the models, (Pickett *et al.* 2009, Shin *et al.* 2010, Lehtonen and Laiho 2010), and this work address this issue. The state variable equation of memristor in Strukov and Williams (2009a), in a more detail demonstration is equal to $\vartheta \cdot e^{-\frac{U_A}{qV_0}} \cdot \sinh(\frac{\varrho E}{2V_0})$, where ϑ is velocity, U_A is activation energy, V_0 is thermal voltage, and E is electric field. The E_0 in the equation indicates a point between linear and nonlinear electric field and μ_v shows the mobility. This nonlinearity can be large, it is stated that a 20 orders of magnitude of change in the drift velocity due to a small change in the applied electric field (Strukov and Williams 2009a).

In Pickett *et al.* (2009) two equations in the form of $v \cdot \sinh(\zeta) \cdot e^{-e^{(\pm \omega_a - \zeta_b)} - \omega_c}$ are defined to separately explain the OFF and ON switching behaviour. In these equations, v is ON or OFF switching velocity, ζ and ζ_b are dimensionless parameters depending on i_M, and ω_a and ω_c are dimensionless parameters based on the device state variable, x, and ON and OFF limits, x_{on} and x_{off}. In the Shin *et al.* (2010) model, δ is a positive constant, and w_q is a normalised memristive charge. The $\sinh(\cdot)$ part of the equation cannot be found in Lehtonen and Laiho (2010). In fact the $\sinh(\cdot)$ describes the memristor behaviour in a more generic way than their proposed V^{13} function.

It worth noting that the modelling approach presented in this section can be extended to memcapacitor and meminductor (Ventra *et al.* 2009) modelling using a similar technique that has been proposed by Biolek *et al.* (2011).

Table 5.1. Subcircuit model for memristor. SPICE subcircuit of a memristor

```
.SUBCKT memristor Pos Neg PARAM:
```
Parameters:
```
n=4 a1=9 a2=0.01 b1=2 b2=4 l=10n
wmin=0.05 wmax=0.95 p0=1.2 fon=40E-3 foff=40E-3
```
* Shape factor, sf, can be a function of tunnelling barrier width (normalised state variable)
```
sfo=4 sfm=20 p=5 *** sf(w)=sfo+sfm(1-(2w-1)**2p)
```
State variable:
```
Gvon 0 w value =
    signm(wmax-V(w))*signm(V(Pos,Neg))*gon(V(Pos,Neg),sf(V(w)),p0)
Gvoff 0 w value =
    signm(V(w)-wmin)*signm(V(Neg,Pos))*goff(V(Pos,Neg),sf(V(w)),p0)
```
* *Initial (internal) state*:
```
.IC V(w) 0.5
```
Integration:
```
Cw w 0 8e-5
Rw w 0 0.01T
```
Current equation:
```
Gmem Pos Neg value =
    l*((V(w)**n)*a1*sinh(b1*V(Pos,Neg))+a2*(exp(b2*V(Pos,Neg))-1))
```
* Series resistor, R_S, can be implemented here, between two Neg1 and Neg2 nodes.

Functions:
```
.func signm(v) = (sgn(v)+1)/2
.func gon(v1,v2,v3) =
    fon*((1-v1/(2*v3))*exp(v2*v3*(1-sqrt((1-v1/(2*v3))))))
.func goff(v1,v2,v3) =
    foff*(-((1+v1/(2*v3))*exp(v2*v3*(1-sqrt((1+v1/(2*v3)))))))
.func sf(v1)=sfo+sfm(1-(2*(v1)-1)**2p)
.ENDS memristor
```

Table 5.2. Memristor models comparison. Progression in the development of memristive device modelling. Key: Ⓥ Programming threshold Ⓢ SPICE-like Ⓣ Adaptation of tunnelling phenomena.

Models	State variable	$f(\cdot)$	I-V	Ⓥ	Ⓢ	Ⓣ
Strukov et al. (2008)	$\alpha \cdot i_M$ and $\alpha \cdot f_H(w) \cdot i_M$	$w(1-w)$	$V_M/M(q_M)$	-	-	-
Kavehei et al. (2010)	$\alpha \cdot f_H(w) \cdot i_M$			-	+	-
Joglekar and Wolf (2009)	$\alpha \cdot f_J(w) \cdot i_M$	$1-(2w-1)^{2p}$		-	-	-
Biolek et al. (2009b)	$\alpha \cdot f_B(w) \cdot i_M$	$1-(w-\text{stp}(-i_M))^{2p}$		-	+	-
Shin et al. (2010)	$\alpha \cdot i_M$ and $\alpha \cdot f_S(w_q) \cdot i_M$	$\delta+1-(2w_q-1)^{2p}$		-	+	-
Strukov and Williams (2009a)	$\mu_v E_0 \cdot \sinh\left(\frac{E}{E_0}\right)$	-	-	+	-	-
Pickett et al. (2009)	$v \cdot \sinh(\zeta) \cdot e^{-e^{(\pm\omega_a-\zeta_b)}-\omega_c}$	-	Supplementary material in Pickett et al. (2009)	+	+ (Abdalla and Pickett 2011)	+
Linares-Barranco and Serrano-Gotarredona (2009)	$A \cdot \text{sign}(V_M)\left(e^{\frac{\lvert V_M\rvert}{V_0}} - e^{\frac{V_t}{V_0}}\right):\lvert V_M\rvert>V_t$; $0:\text{otherwise}$	-	$V_M/M(q_M)$	+	-	-
Lehtonen and Laiho (2010)	$\alpha \cdot f_J(w) \cdot V^{2j-1}$; $\alpha \cdot f_J(w) \cdot \sinh(c_b V)$	$1-(2w-1)^{2p}$	$i_M = w^n\delta\sinh(\vartheta V_M)+\chi(e^{(\gamma V_M)}-1)$	+	+	-
This work	$v \cdot g(V,\rho(w),\varphi_0)$	-		+	+	+

5.4.2   Analogue characterisation

The function of biological synapses in the brain can be likened to the behaviour of memristors (Jo *et al.* 2010, Kavehei *et al.* 2011b, Ohno *et al.* 2011, Snider *et al.* 2011, Choi *et al.* 2009, Linares-Barranco and Serrano-Gotarredona 2009). This implies that memristor-based systems have the potential to form basic building blocks for neuromorphic analogue processors. So device models must be able to adequately simulate the analogue behaviour of them these devices. Initialisation would be the first step in programming an analogue memory. The next step is to apply a series of successive positive voltages. The shape of the applied signal is not important as far as there is a reasonably good control on the time integral of the applied voltage. The number of levels that we are able to encode and decode is application dependent. For example, pattern-recognition presents unique application were enhanced edge information, can be encoded into a matrix of memristive-states as analogue data. The analogue nature of the state variable helps to implement a fully analogue pattern recognition structure. In an oversimplified manner, by using a front-end memristive convolution and analogue storage layers and a back-end analogue winner-takes all (WTA) layer (Hammerstrom and Zaveri 2010). This part of the thesis illustrates the application of the proposed model in mimicking the analogue behaviour of the memristors. The results from this part will be utilised in the design of a memristor-based circuit designs and simulations in Chapter 8.

Figure 5.6 (a) highlights the change in the amount of current that can pass through a memristor after a succession of 10 positive and negative voltage sweeps (5 each). The magnitude of current can be tuned for a range of microamperes up to a few hundred milliamperes (Jo *et al.* 2010). Figure 5.6 (b) demonstrates the internal states of a memristive device after applying couple of positive and negative signals. This characterises the behaviour of *analogue memristor*, which can be synonymous with an *analogue memory*. Figure 5.7 illustrates the current-voltage behaviour of a memristive device as an analogue device.

5.5   Measurements and I-V modelling

It is important to note that an initial irreversible electroforming process is required to activate switching behaviour of the device under test. The nonlinearity, switching
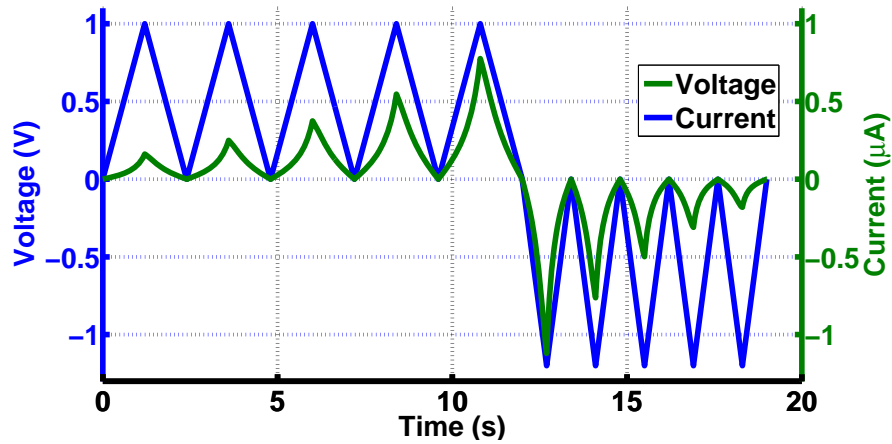
(a) The current and voltage versus time.
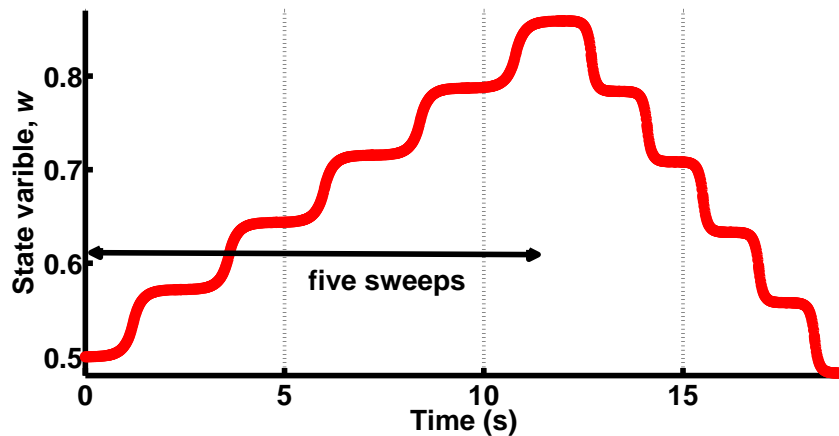
(b) Normalised state variable, w, position during the sweeps.

Figure 5.6. Memristor response to a number of successive triangular voltages. The magnitude of the negative applied voltages are 1.2 V, while the positive voltages are 1 V. The reason for that is to adjust the memristor's state to be in the same position as it was before the test. Due to the different speeds and current for ON and OFF switching, different voltage values to adjust the memristor state are expected. It is found that due to the nanostructure of the memristor and existence of a high electric field by applying a few hundred millivolts, a large uncertainty in adjusting the memristor's state is expected. The memristor mathematical expression allows us to assume that the connection of two memristors in series can help to compromise the process variation side effects.
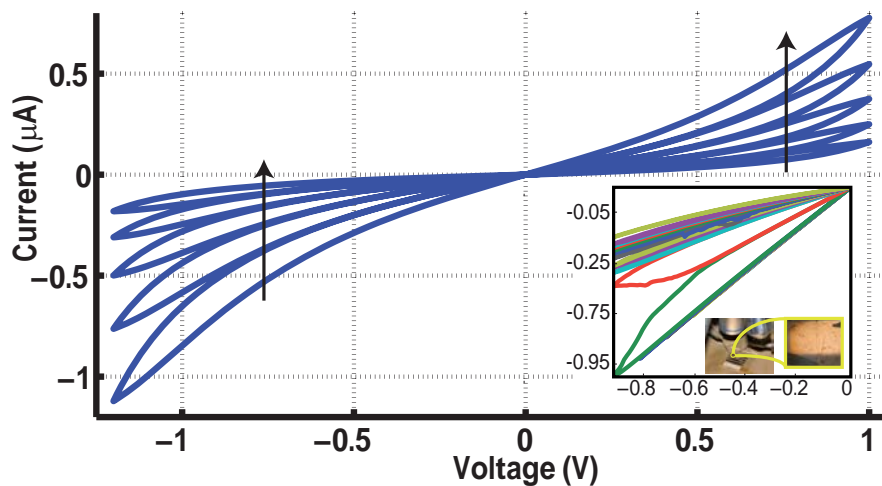
Figure 5.7. Memristor operation in its analogue regime. The memristor I-V curve in its analogue regime of operation. Positive hysteresis loops start from $w = 0.5$ and by applying a 1 V triangular voltage pulse w changes to 0.58. Successive pulses then change w to different values. Here the change in w for each positive step are similar. To adjust w around 0.5 both applied voltage and the time are different from the positive side. When the last positive voltage pulse is applied maximum current can be observed since w is close to ON state. The negative hysteresis then starts with a high amount of current which is gradually decreasing by further application of successive pulses. The existence of multi-stable memory state are experimentally observed and is shown in the inset figure. The x and y-axes in the inset are voltage and normalised current (to a maximum of 35 μA), respectively. It clearly shows that the rate of change in the conductance is related to the initial conductance in a nonlinear manner. This is the result measured using a Keithly 4200-SCS for the fabricated Ag/TiO$_2$/ITO memristor in Figure 4.6. More information about the inset figure is given in Section 9.3.2.

behaviour, and reproducibility of a device under test is related to the forming process as discussed in Chapter 4. We have achieved significantly higher resistances for the both ON and OFF states and higher ratios but their functional reproducibility as well as appropriate forming process continue to be under further investigations. In this particular case, we have created an electric field around 2.3 MV/cm across the device ($L = 22$ nm) to carry out the forming step.

The analogue properties of the device are measured at 100 mV incremental steps as part of presetting the device. Figure 5.8 (b) illustrates several programming steps that were taken above 500 mV with 100 mV increments. The device is programmed at its low resistance state. Using this technique, the analogue values can be stored in the memristor as an internal state. The incremental rate is around 10%. The positive

sweeps (0 to 200 mV) did not contribute to any noticeable change in the device resistance state. Data were collected using a Keithley 4200-SCS semiconductor parameter analyser. Both of the graphs in Figure 5.8, confirm the application of the Ag/TiO$_2$/ITO memristor in digital and analogue applications. The state variable equation confirms the experimental data in Figure 5.8 (b). Preliminary results of this structure as a synaptic connection and a full consideration of a memristor-based spike-timing-dependent plasticity (mSTDP) are discussed in Chapter 8. It worth mentining that analogue and digital behaviours of a memristor device can be controlled with a careful control of the applied voltage (electric field) and integration time.

The model for *I-V* curve in Eq. (5.9) can be improved to a general form of $I = x^n I_{ON} + (1 - x)^n I_{OFF}$ to describe the *I-V* curve of memristive devices, where I_{ON} and I_{OFF} are ON (LRS) and OFF (HRS) currents, respectively. Therefore, *I-V* can be given by:

$$I = x^n(aV + b) + (1 - x)^n(c_1 \exp(d_1 V) - c_2 \exp(d_2 V)) , \tag{5.10}$$

where a, b, c_1, c_2, d_1, and d_2 are parameters related to the device structure, materials, and dimensions. Here we fit appropriate values for these parameters for the ON and OFF currents. The parameter n defines the nonlinearity between x and I. This parameter is defined to address the non-uniformity of the step changes in Figure 5.8 (b). For sake of simplicity, it is assumed that $n = 1$. The SPICE macromodel parameters are provided in Table 5.3. In several experiments we have set the completion current to 10 mA to protect the device reaches to the breakdown condition, however, in this particular case no completion current was set. The approach is consistent with the measurement results as illustrated in Figure 5.8. From Figure 5.8 it is clear that the presented simulated device is consistent with measured device characteristics and shows a highly non-linear behaviour.

5.6   Complementary resistive switch

Although the memristor has introduced new possibilities for memory applications within the simple and relatively low cost crossbar array architectures, the inherent interfering current paths between neighbouring cells imposes limitations on the scalability of such arrays (Kavehei *et al.* 2011a, Linn *et al.* 2010). Linn *et al.* (2010) addressed these limitations, through adaptation of two series memristive elements connected with opposing polarities. This structure is referred to as Complementary Resistive
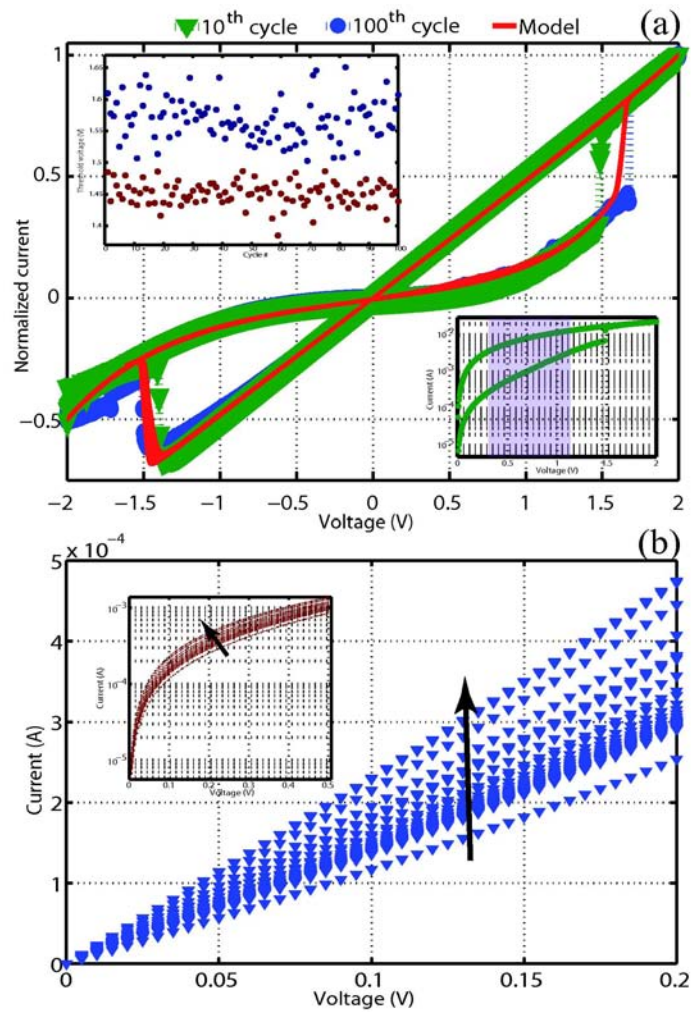
Figure 5.8. Memristor modelled and measured characteristics. Ag/TiO$_2$/ITO memristor characteristics. (a) current-voltage hysteresis loop. The green and the blue lines illustrate measured *I-V* curves at 10 and 100th switching cycles, respectively, using Keithley 4200-SCS Semiconductor characterisation System. The narrow red curves in (a) shows the model using our model highlighting good agreement. The top-left corner inset illustrates variation of switching threshold for SET (blue) and RESET (red, absolute value) processes for 100 cycles analysis. The bottom-right corner inset demonstrates log scale *I*-linear *V* and the highlighted region identifies safe region for READ operation (linear line and no switching). After 100 cycles of switching, a standard deviation of 26 mV in threshold voltage was observed. (b) analogue memory property. The arrow in (b) shows that the evaluations commences with a low state to high state. Analogue memory property of the fabricated memristor confirms implementation of a multistable states device which is able to retain its internal state for long term (days) either after disconnecting power supply or under stress situation of continuous reading using 0.01 V DC. Each curve was measured two times, just before disconnecting the power supply and after connection. Inset demonstrates applied voltage up to 500 mV and log scale current.

Table 5.3. Parameters for the model. Parameters and related values for the model

Parameter	Value	Parameter	Value
V	-2 V to 2 V	a	$1.2e-2$
x	Normalised state variable	b	$4.3e-6$
φ_0	1.2 eV (Miao *et al.* 2009)	c_1	$3.3e-4$
δ	6	c_2	$4.8e-4$
η_{ON}	22	d_1	2.1
η_{OFF}	28	d_2	1.6
p	5	v	$4.0e-3$

Switch (CRS) as shown in Figure 5.11. The unique aspect of this device is in using a series of high resistance states (HRS) and low resistance states (LRS) to introduce logic "0" and logic "1". As an example, a LRS/HRS combination represents "1" and a HRS/LRS state represents "0". Using this approach, the net resistance of the device is always around the HRS, which helps in reducing parasitic (sneak-path) currents and at the same time overall currents in the system. The advantage of using CRS as a fundamental element originates from its excellent READ voltage margin, even with small HRS to LRS ratios. Moreover, it facilitates a comparable WRITE margin Yu *et al.* (2010). There is also a lack of SPICE model verification for CRS devices and a statistical analysis considering the mentioned operational uncertainties. This section provides the first model for CRS device using a filamentary-based model for memristors.

An appropriate $h(\cdot)$ function, in Eq. (5.1), seems to be either a double exponential or related forms (Pickett *et al.* 2009, Kavehei *et al.* 2011d, Yu and Wong 2011), or a $\sinh(\cdot)$ function (Strukov and Williams 2009a), for a filamentary-based model, which defines intrinsic threshold voltages. A commonly accepted $\sinh(\cdot)$ function is applied to the experimental data and the outcome shows a good agreement between the measured data and the modelled *I-V* hysteresis.

To address this modelling problem we use the Mott and Gurney (1964, Chap. 2) model of ionic conduction in terms of the theory of lattice defects that has been already used in several studies in this area. In this case,

$$\frac{dw}{dt} = v_0 e^{-\frac{U}{kT}} \sinh\left(\frac{\rho V}{kT}\right),$$ (5.11)

where v_0 is initial velocity, U is the potential barrier height, k represents the Boltzmann constant, T temperature, and V applied voltage in eV. The parameter $\rho = a/2L$, which

is a dimensionless parameter that relates the distance between adjunct lattice positions, a, and the solid-electrolyte thickness L.

A detailed comparison between the model and experimental data is given by Heuer *et al.* (2005). The applied voltage polarity identifies the channel orientation (Strachan *et al.* 2011, Valov *et al.* 2011, Kim *et al.* 2011b). The forming step (more information is available in Chapter 4) is carried out by applying an electric field around 6.2 MV/cm across TiO$_2$. This forming step creates a difference in atomic percentage ratio of oxygen in TiO$_2$ close to one of the electrodes. Conduction mechanism is then stated out through a channel known as conducting filament (CF). The conducting filament is highly localised (e.g. for a cylindrical CF, like in Figure 5.9, $A_{CF} \approx 80$ nm^2 at the cathode, if R_1 is 10 nm) compared to the metallic contact area, A, and the filament (ON) resistance R_{LRS} is proportional to A_{CF}^{-1} (Ielmini *et al.* 2011).

Figure 5.9 represents an alternative switching mechanism, which is a metallic filamentary based (Yu and Wong 2011). In this approach, the electroforming step can be eliminated because the top metal can act as an active electrode. The model developed with this approach is able to produce the expected behaviour of a CRS structure. According to this mechanism, the active electrode supplies metal ions (Ag$^+$) for migration in the solid electrolyte during the SET process, as shown in Figure 5.9 (a). The RESET process can occur when a negative bias is applied to the top electrode. This applied bias forces the ions in the filament to laterally dissolve into the active electrode again.

A Verilog-A implementation of this model is used as a macro-model in Cadence. The macro-model implements the function $h(\cdot)$ as $I = (x)I_{ON} + (1 - x)I_{OFF}$. These experiments show a linear I_{ON}-V, which is in agreement with measurement results for an area of 100×100 μm^2 memristor device (Kavehei *et al.* 2011d). This differences between ON and OFF currents can be even much larger. For instance, Inoue *et al.* (2005) reported $I_{OFF} \propto \sinh(\cdot)$ and $I_{ON} \propto \sinh^{-1}(\cdot)$.

Figure 5.10 illustrates the modelling results for a memristor based on experimental data from the Ag/TiO$_2$/TiO$_{2-x}$/ITO measurement implementation (Kavehei *et al.* 2011d). This implementation yields a bipolar cell with nearly 200 successful cycles. Besides asymmetry, recent studies shows that the inherent Joule heating effect is responsible for (RESET) switching mechanism in a way that sufficient heat induces a crystallization of the oxide surrounding the channel (Strachan *et al.* 2011, Russo *et al.* 2007), which is also
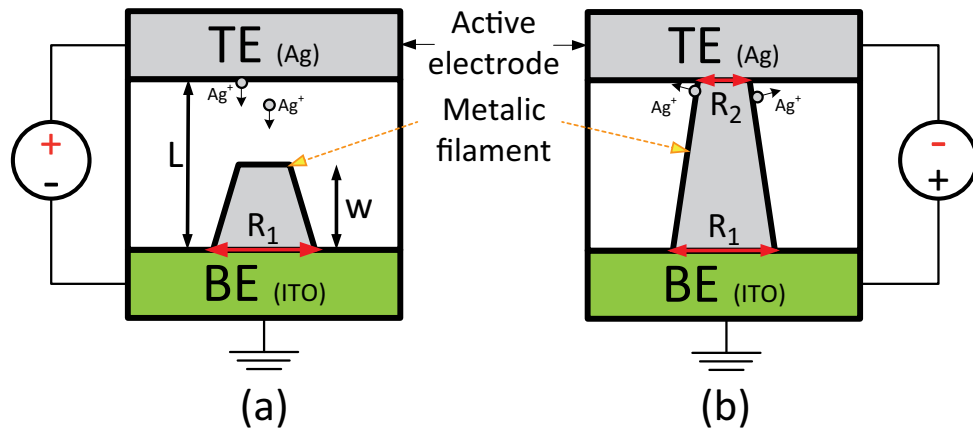
Figure 5.9. Existence of the metallic filament. The top electrode ions creates the metallic filament in which that the diameter at the bottom electrode, R_1, is larger than the top diameter R_2. This can be considered as a switching mechanism for devices known as Conducting-Bridge Random-Access Memory (CBRAM). The top electrode here is known as an active electrode which supplies metal ions to create metallic filament, as shown in (a). These ions laterally dissolve under a negative voltage bias for the RESET process, as demonstrated in (b).

Table 5.4. Physical parameters for filamentary-based modelling of the memristor. Physical parameters for the filamentary model. A basis for CRS modelling approach.

Parameter	Value	Unit	Reference
a	1.5	Å	(Strukov and Williams 2009a)
f_e	10^{13}	attempts/s	(Strukov and Williams 2009a)
E_{ai}	1.1	eV	(Miao et $al.$ 2011)
v_0	1500	m/s	calculated
L	22	nm	fabricated
ρ	0.0034	no unit	calculated
k_{th}	1.5	W/(Km)	(Xia et $al.$ 2011b)
A	100×100	μm^2	fabricated
A_{CF}	10	nm^2	(Ielmini et $al.$ 2011)
R_{th}	4.5×10^6	K/W	calculated

discussed in Chapter 4. This crystallization time frame is exponentially related to temperature (Strachan *et al.* 2011). The exact equation can be extracted from Ielmini *et al.* (2011). Therefore, as Joule heating increases in the hysteresis, the CF diameter (hot spot) shrinks and this effect would lead to a reset. We include this effect in the macro-modelling approach using a relation introduced in Russo *et al.* (2009),

$$T - T_0 = PR_{\text{th}} \,, \tag{5.12}$$

where $T_0 = 300$ K, $R_{\text{th}} = L/(8k_{\text{th}}A_{\text{CF}})$ is the thermal resistance, $P = IV$ is Joule dissipation at reset, and k_{th} is TiO$_2$ thin film thermal conductivity. According to experimental data, as A_{CF} decreases, RESET current decreases, so the RESET threshold voltage would increase (Russo *et al.* 2007). In order to increase simulation convergence Eq. (5.11) can be rewritten as,

$$\frac{dw}{dt} = v_1 V + v_3 V^3 + v_5 V^5 + \dots \,, \tag{5.13}$$

where v_1, v_3, and v_5 are low-field and higher order coefficients. This approach also combines the effects of Joule heating and $L - w$ (on the effective electric field) in v_i coefficients. Note that $dw/dt = v_1 V$ usually defines a pure memristive behavior, as described in Chua (1971).

These properties then raise the following questions, (i) how to address the asymmetric characteristic in WRITE and READ operations, (ii) what is the impact of using more realistic model for cross-point array evaluation, and (iii) what is the effect of different device level *I-V* characteristics on the array performance? Here we are aiming to answer the first two questions using the explained model and an answer to the third question is currently under review by our research group and will be the topic of another paper. The second question can be answered using a worst-case consideration for R_{ON}. In this case, this a comparison of a memristor array with a CRS-based array will be given. Using the developed model of the memristor that accurately models the nonlinear behavior of the device, the CRS operation can be explained as detailed in the following section.

5.6.1   Complementary resistive switch modelling

A CRS is a resistive switching device that is built using two memristor devices connected in series with opposite polarities (Linn *et al.* 2010). Figure 5.11 (c) illustrates the
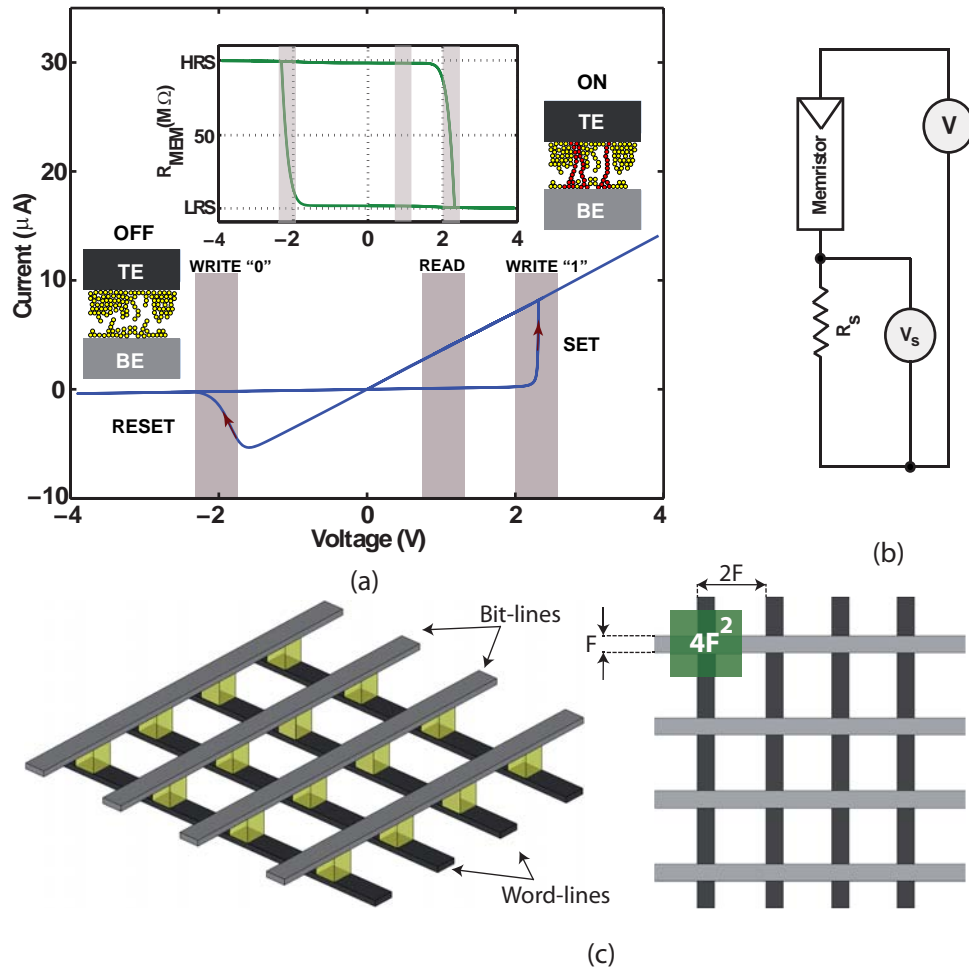
Figure 5.10. Memristor measurement and its model approximation. Memristor cross-point implementation and array presentation. (a) Memristor model result verified by experimental data of a fabricated Ag/TiO$_2$/TiO$_{2-x}$/ITO (Kavehei *et al.* 2011d). Inset shows memristor device resistance vs applied voltage. TE and BE represent the top-electrode and bottom electrode, respectively. The reason for choosing -4 V to 4 V is related to CRS device functionality that is explained in Section 5.6.1. The curve shows asymmetric characteristics. The measurement data was collected using a Keithley 4200 Semiconductor Characterisation System. Red paths (inset (a)) show filament paths, like what is reported in Figure 4.7 (c). The probability that a conductive path is broken can be calculated through a set of (independent) Boltzmann probabilities (Zhirnov *et al.* 2010). Due to the internal dynamics of the memristor, we applied similar voltage (time-domain triangular) signal to the model and device. The diagram (b) conceptually shows the measurement setup. The arrays in (c) illustrate three-dimensional (3D) and two-dimensional (2D) view of a RRAM (memristive) array. RRAMs introduce smaller cell size, $4F^2$/bit, where F is the lithography feature size.

Table 5.5. CRS logic and ON states. State transitions in CRS

R	ΔV	R'	Output
H ("1")	$V_{\text{th,S1}} < \Delta V < V_{\text{th,R1}}$	L (ON)	pulse
H ("1")	$V_{\text{th,R1}} < \Delta V$	H ("0")	spike
H ("0")	$V_{\text{th,R2}} < \Delta V < V_{\text{th,S2}}$	L (ON)	pulse
H ("0")	$\Delta V < V_{\text{th,R2}}$	H ("1")	spike
L (ON)	$V_{\text{th,R1}} < \Delta V$	H ("0")	–
L (ON)	$\Delta V < V_{\text{th,R2}}$	H ("1")	–

modelling results. The figure's inset illustrates a CRS based cross-point array. Each memristor in the figure follows a *I-V* curve that is shown in Figure 5.10 (a). The minimum applied voltage for a switch is around ± 2.0 V. Considering the CRS structure as a simple voltage divider, for a LRS/LRS situation[14] minimum ± 2 V is applied across either of the memristors. Please refer to Table 7.1 for the crossbar memory array parameters. CRS's ON state resistance is $R_{\text{CRS,LRS}} = R_{\text{ON}} \approx 2R_{\text{LRS}}$, where R_{LRS} represents memristor's LRS and CRS's high resistance, $R_{\text{CRS,HRS}} = R_{\text{LOGIC}} \approx R_{\text{HRS}}$, where R_{HRS} indicates memristor's HRS (see Table 5.5). Figure 5.12 highlights the resistance switching of the CRS device. The initial state is programmed to be slightly below $R_{\text{CRS,HRS}}$, so there is a difference at the initial curve and the rest of the sweeps. In a memristor device, logic "0" and "1" are represented with R_{HRS} and R_{LRS}, respectively, whereas a CRS device represents logic "0" and "1" using a combination of low and high resistances which results in overall resistance of R_{HRS} (R_{OFF}) for the both logical values.

A fresh CRS device shows a HRS/HRS resistance for memristors A and B. This combination occurs only once (this is not shown in the figure) (Valov *et al.* 2011). After applying a positive or negative bias, depending on the polarity of memristors, the device switches to either the "0" or "1" state. In Figure 5.11 (c), red lines are threshold voltages for SET $V_{\text{th,S1}}$ and $V_{\text{th,S2}}$ and for RESET $V_{\text{th,R1}}$ and $V_{\text{th,R2}}$. In an ideal CRS device, $V_{\text{th,SET}} = V_{\text{th,S1}} = |V_{\text{th,S2}}|$ and $V_{\text{th,RESET}} = V_{\text{th,R1}} = |V_{\text{th,R2}}|$. Here $V_{\text{th,SET}} = 2.4$ V and $V_{\text{th,RESET}} = 3.6$ V. A successful READ operation occurs if $V_{\text{th,SET}} < V_{\text{READ}} < V_{\text{th,RESET}}$. For a successful WRITE, $V_{\text{th,RESET}} < V_{\text{WRITE}}$. Consequently, every voltage below $V_{\text{th,SET}}$ should not contribute any change in the device state. Possible state transitions are shown in Table 5.5, where R' shows the next resistance state, R illustrates the initial

---

[14]This situation is defined as the ON state. This is not a stable state so it does not represent a logic state but plays an important role in the switching, READ, and WRITE processes.
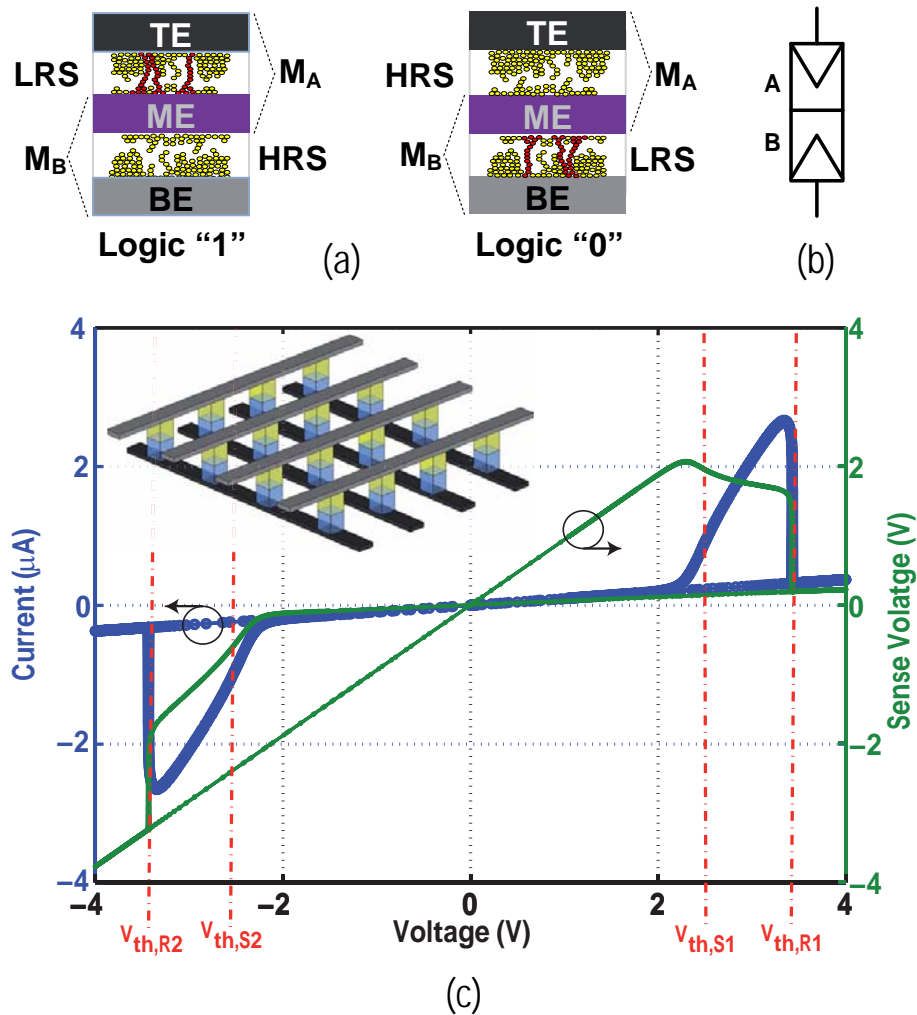
Figure 5.11. CRS *I-V* **characteristics.** CRS functionality using the described memristor model. (a) Fundamental behaviour of switching between logic "0" and logic "1". TE, BE, and ME are the top, bottom, and middle electrodes, respectively. The reading procedure can be carried out by sensing ME. M_A and M_B are memristors A and B. Here, (b) A symbol for the CRS device. (c) *I-V* sense voltage curve of the simulated device that shows the characteristics described in Linn *et al.* (2010). The inset shows a 3D schematic of a CRS array.

resistance state, and output is a current pulse or spike. In this table, H represents high resistance (either logic states, Logic "0" or Logic "1"), and L indicates low resistance.

The simplest analytical model of a CRS can be defined in a relative velocity form, when $dw/dt = dw_A/dt + dw_B/dt$ and the two memristors (A and B) form a voltage divider.
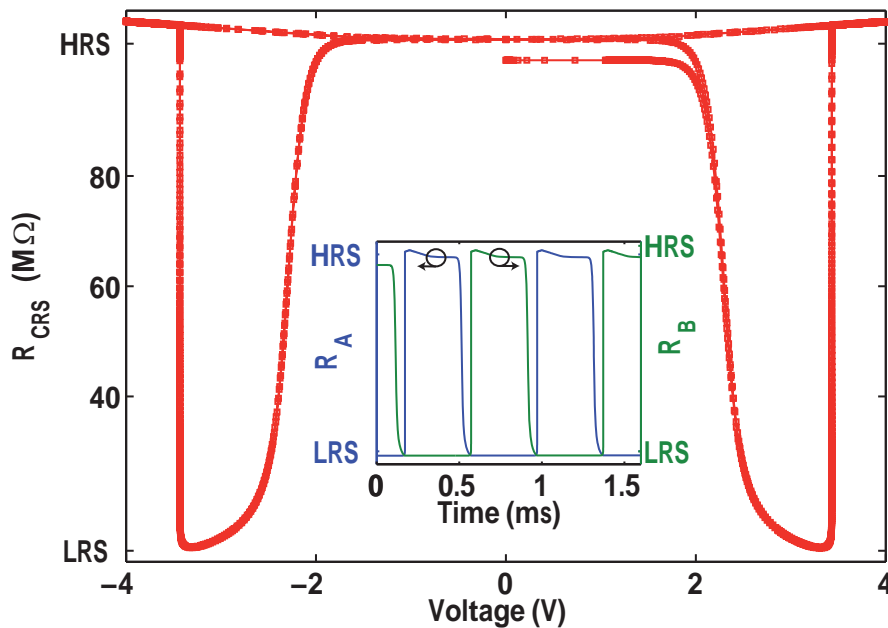
Figure 5.12. CRS resistance behaviour. CRS effective resistance for a triangular applied voltage. The inset clearly shows the switching mechanism for memristors A and B. The initial state is slightly less than $R_{OFF}(= R_{HRS} + R_{LRS})$. The device is initially programmed close to its HRS and not exactly the HRS value to highlight the initial state conditions.

The first feature that appears from the CRS simulation, and device fabrication (Linn *et al.* 2010, Rosezin *et al.* 2011), is a perfectly symmetric *I-V* curve out of an asymmetric memristor *I-V* curve. The device is programmed initially at logic "1", LRS/HRS, ($R_A \approx$LRS and $R_B \approx$HRS). An appropriate READ pulse creates a high potential difference across R_A while the voltage difference across R_B is not beyond its memristive threshold. Therefore, R_A switches to LRS and an ON current (pulse) passes through the CRS device. After a resting time, a negative WRITE pulse is applied to restore "1", which can be defined as refreshing procedure. Figure 5.13 (b) shows that the R_{CRS} settled close to HRS with a logic "1" stored in the device. Then a positive WRITE pulse tends to write logic "0", which can be defined as programming step. Depending on the switching speed of the memristors, a short term ON state occurs that causes a relatively large current spike (encircled by red dots in Figure 5.13 (a)). There are other

functional characteristics that have to be met. For instance, a HRS/HRS state should not appear in any of the situations that are demonstrated by the presented simulation (Yu *et al.* 2010).

5.6.2   CRS measurement using Ag/TiO$_2$/ITO memristor

Figure 5.14 illustrates the behaviour of a three terminal CRS device that uses two memristors, functioning with ± 1 V applied voltage, connected in series with opposite polarities. The asymmetry of the *I-V* curve is mainly due to: (1) using two different memristors instead of one CRS device[15], (2) different contact sizes of the two memristors, (3) and perhaps fluctuations that affect memristive behaviour during the electroforming process. The structure is more like a memistor device (Widrow 1960). A relatively high (effective) electric field results CRS behavior. A three-terminal resistive switch fabrication technique is introduced in Xia *et al.* (2011a), and Xia (2011).

5.7   Conclusion and potential extensions

Emergence of a new nano devices such as the memristor brings numerous challenges from the design formulation phase through to its final implementation. This chapter provided an insight into memristor fundamentals and physical behaviour from which we addressed an overview of modelling approaches being pursued by the design community. It compared features of these models using HP's published TiO$_2$ platform and finally our fabricated memristors in Chapter 4 as the basis of such comparisons. This chapter reviewed modelling options that have been published over the past three years to motivate reconciliation of some of the unexpected behaviours of MIM thin films such as those encountered in a memristor. It also introduced a modelling approach based on tunnelling, which includes the concept of programming threshold and SPICE-friendly model. Based on this model a unique device that uses two memristors, commonly referred to as CRS, was discussed and both simulation and measurements were presented and discussed. This device will later be utilised in the design of high density memory array structures.

---

[15]The device is an integrated device itself and it is not fabricated using two memristors in series. The two memristor in series is just one way in simulating the CRS behaviour.
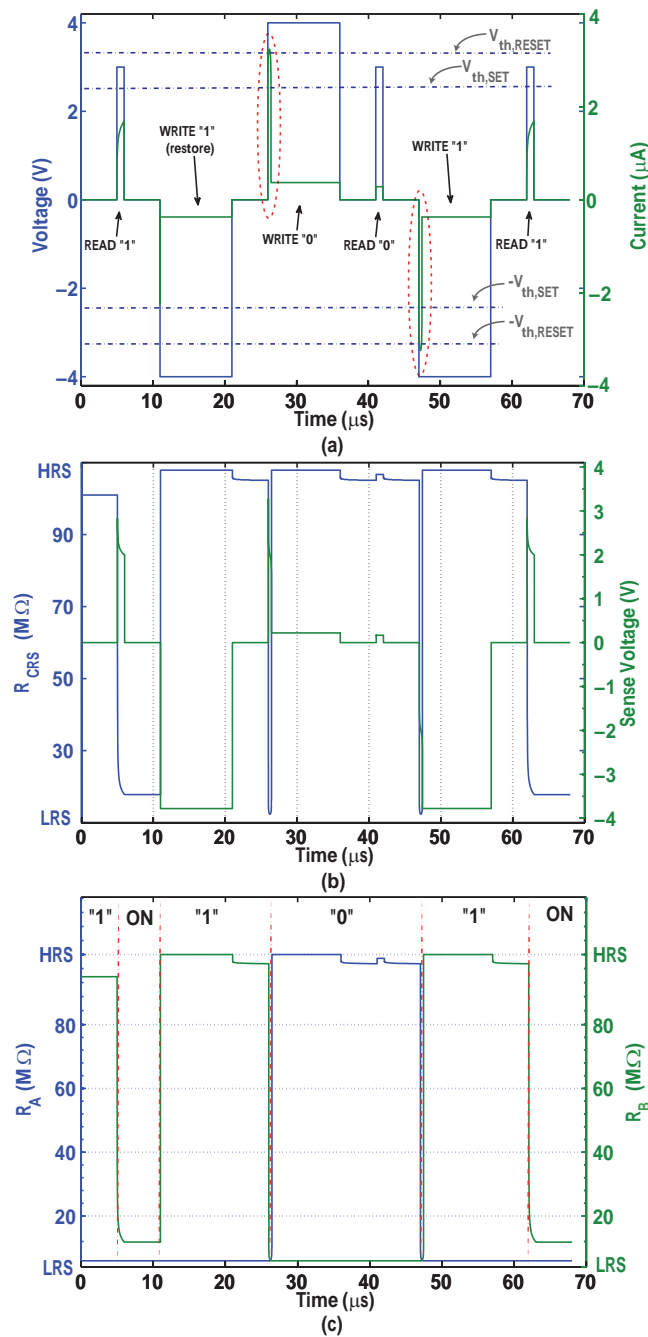
Figure 5.13. CRS response to a sequence of pulses. CRS response to a sequence of pulses for READ and WRITE operations. (a) Current response to applied voltage pulses. The dash lines indicate threshold voltages. The 1 μs READ pulses lie between the $V_{\text{th,SET}}$ and the $V_{\text{th,RESET}}$. A 5 μs WRITE pulse provides a voltage amplitude beyond $V_{\text{th,RESET}}$. (b) Illustrates the total CRS resistance and sense voltage (sensing from middle electrode). As can be seen from the figure, for most of the time $R_{\text{CRS}} \approx$ HRS. (c) Shows the logic in terms of memristive state for A and B memristors. memristors. Appropriate READ and WRITE pulse widths have been already discussed in Yu *et al.* (2010).
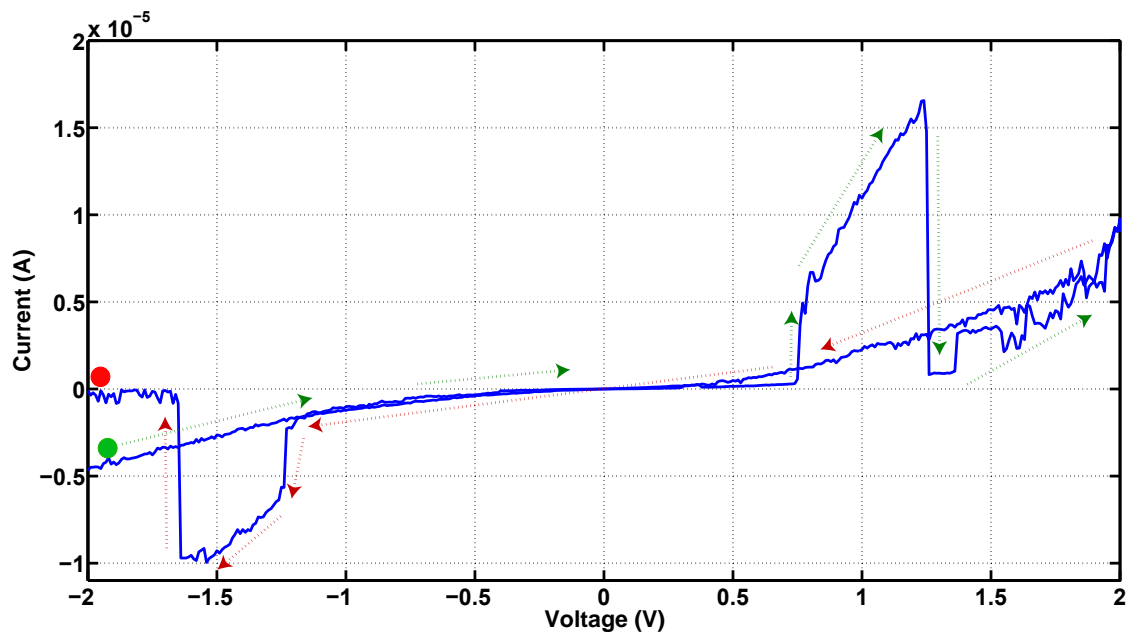
Figure 5.14. Three-terminal memistor acting as a CRS. CRS device measurement using two memristor devices connected in series forming a memistor type device with no control applied to the middle electrode. The green dot demonstrates starting point and the red dot shows final point of the experiment.

This project was part of a multi-layer three-dimensional system. The system overview and my contributions in designing CMOS image sensor layer and connections between layers of the system and memristive crossbar are discussed in the next chapter.

Chapter 6

System Overview

SYSTEM overview of the targeted structure for the contributions of this thesis are given in this chapter. This system consists of several layers of integrated circuits stacked on top of each other and connected via the Through Silicon Via (TSV) technology. The first and the second layers are included in the context of this thesis. The first layer is a CMOS image sensor array, which produces digital outputs corresponding to the incident light. The imager functionality is carried out through two different concepts, pulse-width and pulse-frequency modulations. Both of the designs were fabricated and tested and related reports are available in this chapter. The second layer is a memristive based array that implement an associative memory as well as memristive-based computational modules. These two layers will be connected using a hardware interface for image feature generation. The image feature generation algorithm is adopted from the literature. It is a rotation-invariant scheme that makes it suitable for any image recognition purposes and in particular the targeted system's application.

[This page has been left blank intentionally.]

6.1   Introduction

Mobile health care monitoring systems and services are rapidly growing as the result of advances in silicon CMOS scaling as well as rapid improvements in the availability of broadband communication systems and networks. Video images such as Magnetic Resonance Imaging (MRI), computed tomography (CT), and X-rays introduce heavy demand on the storage capacity of the memory layer of a processing engine. The dynamic range and bandwidth requirements of medical sensor data vary significantly in addition to the fact that medical sensor data rates are increasing exponentially (Lee *et al.* 2010). The conventional 2D Systems-on-a-Chip (SoC) technology that has characterised implementation strategies of industry over the last decade has numerous challenges in terms of area utilisation, long signal paths, overload bus data, complex signal routing large number of I/Os (inputs and outputs) all result in a significant increase in power consumption. Addressing these challenges present a number of constraints that limit the design of high speed and low power portable multimedia-based biomedical imaging systems.

Recent advances in 3D multilayered fabrication together with the progress in vertical interconnect technology such as that of the Through Silicon Via (TSV) and the emerging non-volatile memory technologies, makes the 3D architectural mapping a viable option for gigascale integrated systems demanded by the health care applications. Therefore, the combination of 3D integrated architectures with multilayer silicon die stacking (Al-Sarawi *et al.* 1998) itself is a promising solution to the severe problem faced by the integrated circuit industry as geometries are scaled below 32 nm.

In this chapter we explore the possibilities for the applications of memristors (RRAMs) in such system. Figure 6.1 presents a system overview of such system. Although, the application is in health care monitoring, the contributions in this thesis are not limited to this system. This work helps to move towards a realisation of a terabit memristor array, which is able to carry out early processing. Considering the fact that, 3D integration technology promises and realised many interesting systems, the technology suffers from a high power density problem (Lee *et al.* 2010). Therefore, the presented work is one step forward for the physical realisation of a ultra-low power memory systems with the ability of storing analogue information and carry out basic computing, such as pattern matching and early edge detection.

As is clear from Figure 6.1 (b), the first layer of this system is an imager. During the course of this thesis, two CMOS Image Sensors (CIS) were fabricated and tested in order to combine with the memristor layer. Measurement resutls for the CMOS image sensor are discussed further in Section 6.2. These two image sensors are both digital and based on the fact that programming of a memristor can be done either through a pulse-width modulation (PWM) or a pulse-frequency modulation (PFM). This chapter provides information about the image sensor layer and a general system level description of how the imager and memristor layers are integrated.

A systematic view of how this image sensor can be integrated with an underlying memristor layer to carry out learning process for patter recognition can be found in Snider (2011). In this case, the image sensor can act as a light-to-thermometer code converter. Then this code can be applied to an array of memristive devices (this part is not covered in this research). The CIS digital output can be even passed through a memristor-based Content Addressable Memory (CAM), a ternary CAM (TCAM), for pattern matching purposes. The detail structure of memristor-based CAM and CRS-based CAM are discussed in Chapter 8.

This chapter consists of three sections. Section 6.2 describes the CMOS image sensor designs and fabrications and includes parts for PWM and PFM sensors. A hardware friendly feature generation algorithm is discussed in Section 6.3. Finally, Section 6.4 summarises this chapter's content.

6.2   CMOS image sensor

Low-voltage operation is essential for working with memristor layer as they need to an interact without interface. Two types of inverter-based CMOS image sensors are studied in this section. This structure was selected to allow for low-voltage and low-power operations. Even though this is not the core part of this thesis, a brief review on the performance metrics of these CIS chips are provided to highlight the needed performance requirement.

The light intensity can be encoded via pulse-frequency modulation (PFM), pulse-width modulation (PWM), pulse-amplitude modulation (PAM), or pulse-phase modulation (PPM) of the output signal. Since the plan is to pursue an early visual processing system using a CMOS image sensor and memristor-based crossbar array, two of the
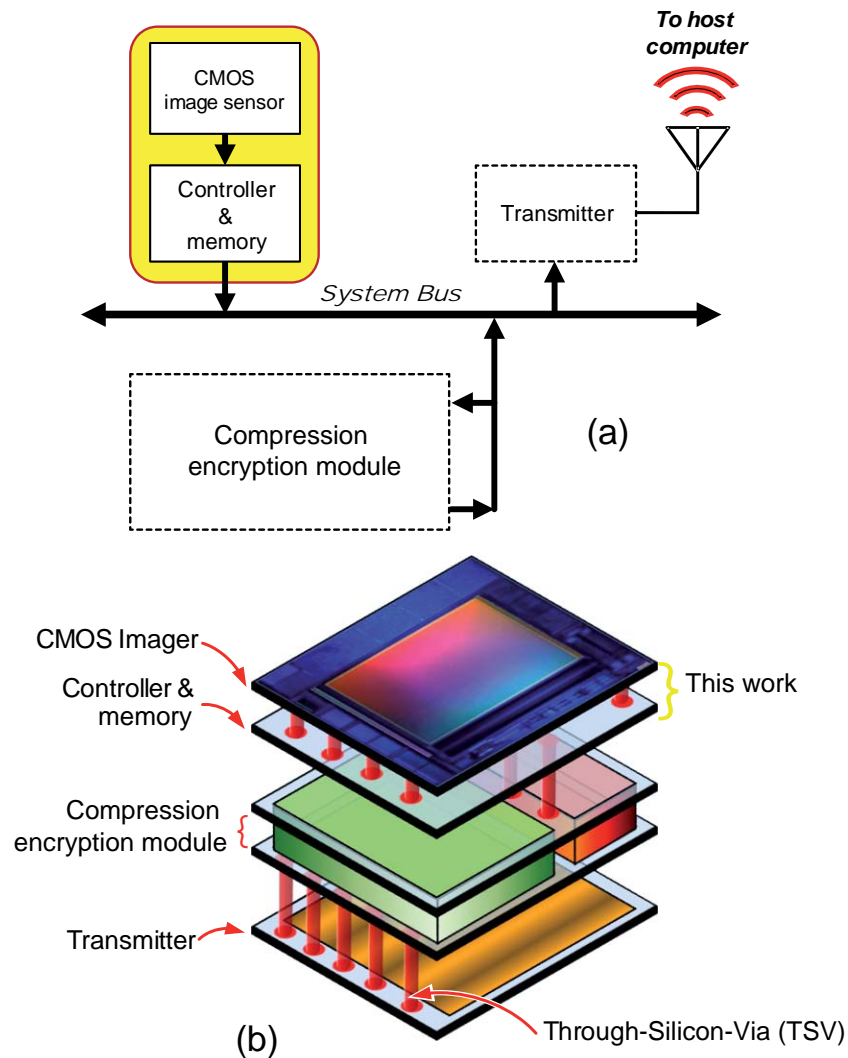
Figure 6.1. System overview. Targeted system schematic. (a) Logical architecture where domain of this thesis is highlighted in yellow, and (b) physical implementation using TSVs for connecting the layers. Our work covers the second layer from the top and the memory layer. The aim is to implement the memory layer using memristive devices, which give us the ability to perform an early visual image processing as well as an analogue non-volatile capability.

possible options are PWM and PFM sensors. According to Figures 2 and 7 in Ohta *et al.* (2000), PWM and PFM sensors can be used for building a vision chip in combination with a resistive network that uses memristive devices.

6.2.1   Pulse-width modulation sensor

This section proposes a novel pixel architecture based on a single inverter with a small readout circuitry. The novel architecture requires only 6 transistors per pixel with the pixel size of $5 \times 5 \ \mu m^2$, and present 58% fill factor when fabricated in 130 nm CMOS technology. In this approach, the inverter performs a one bit analogue to digital converter using "one time" sampling scheme. The small readout circuitry is integrated within the pixel area, which contains a photodiode (PD) and a select part. This novel pixel can operate effectively at 500 mV supply voltage with a wide dynamic range and low power consumption as low as 27 nW/pixel.

The proposed CIS architecture is pixel-based that utilises a single inverter sensor circuitry. The basic pixel design, depicted in Figure 6.2 (a), includes a photodiode (PD), reset transistors M1 and M2, nMOS transistors M3 and M4 used for enabling pixel output, and a single CMOS inverter. The operation sequence is initiated with the reset signal being asserted. Node PD (Figure 6.2 (a)) commences to charge up towards V_{DD}. This is followed by an integration phase whereby the reset is switched to logic-0 and the enable signals is switched logic-1. Thus, the photodiode enters a floating mode. Upon illumination on the photodiode, photocurrent created by the generation of electron-hole pairs results in the voltage at node PD to decrease from $(V_{DD} - V_{th})$ to the ground level. The amount of decrease is a function of the intensity of incident light that falls on PD. In Figure 6.2 (b), the time duration trigger is modulated by illumination amount as PWM that is converted to a voltage. High illumination results in a faster voltage drop while low illumination result in a low discharge. The output of the inverter is mapped into a digital pulse with variable width according to the change of the voltage at node PD. As the consequence, architectures that implement this approach do not require a high resolution analogue-to-digital converter (ADC).

Dynamic power dissipation is proportion to V_{DD}^2, so by operating at low voltage a significant power is achieved, specially when considering a large array. Using a 500 mV supply voltage the Fixed Pattern Noise (FPN) was evaluated as the standard deviation
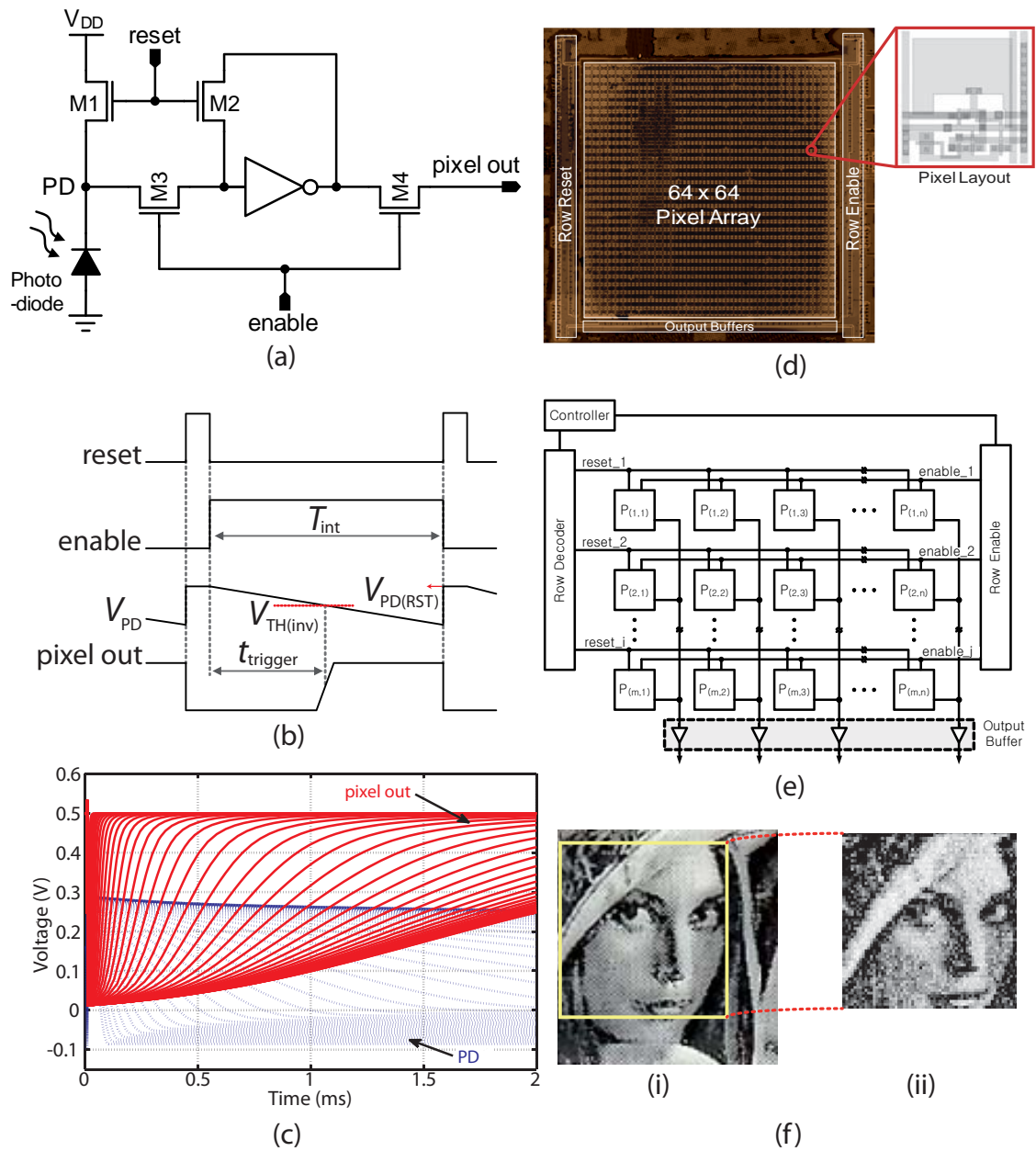
Figure 6.2. PWM CMOS imege sensor. Pulse-width modulation CMOS image sensor. (a) Shows the circuit structure, (b) timing diagram, and (c) experimental results outputs of a single pixel for different light intensities. Micrograph of the fabricated 64×64 CMOS image sensor test chip and the single inverter pixel layout are illustrated in (d). (e) shows the architecture of the design and (f) illustrates (i) the original image, and (ii) captured image by the sensor.

Table 6.1. Features of fabricated CIS. Main features of the fabricated 64×64 CIS array.

Technology	130 nm 6-Metal 1-Poly CMOS
Supply	Voltage 500 mV—1.2 V
Pixel	Size $5 \times 5 \ \mu m^2$
Photodiode	N-diff/P-sub
Fill-Factor	58%
Dynamic Range	83 dB
Sensitivity	225 LSBs/s-Lux(0.44 V/s-Lux)
FPN	$< 1 \times$LSB
Power Consumption	27 nW/pixel

of pixel values from the normalised mean value of a frame data, under flat field illumination. In order to minimise random noise, 54 frames of the same image were acquired and averaged from the flat field images. Histogram results are shown in Figure 6.3 (a). The standard deviation was found to be $1 \times$LSB for the measured FPN. Off-chip digital FPN correction could further reduce the level of FPN (Shoushun *et al.* 2008).

The transfer characteristic of the proposed pixel, shown in Figure 6.2 (b), has a logarithmic like response. This is much similar to the response to illumination of human eyes. There are other reported DPSs having nonlinear transfer behaviour by multiple capturing of the output signal with different integration time (Lai *et al.* 2006). The complexity of some of the approaches necessitate more signal processing circuitry can result in a more complicated readout and more dynamic power dissipation. The proposed pixel architecture also provides a nonlinear transfer curve with simple operation within one single sampling operation.

Figure 6.3 (b) shows dynamic illumination response of the fabricated sensor. It is a wide dynamic range that have a maximum detectable illumination intensity of higher than 10,000-Lux. The measured dynamic range with 8-bit resolution has been limited to 83 dB due to large dark current of the PD fabricated in standard CMOS process. A captured image from the test chip is illustrated in Figure 6.2 (d) The chip characteristics and performance are summarised in Tables 6.1 and 6.2. The later shows performance comparison with the prior works (Lai *et al.* 2006, Hanson *et al.* 2010, Xu *et al.* 2002, Bermak and Yung 2006). The power consumption for the 64×64 array is 112 μW at 500 mV nominal power supply. This corresponds to a
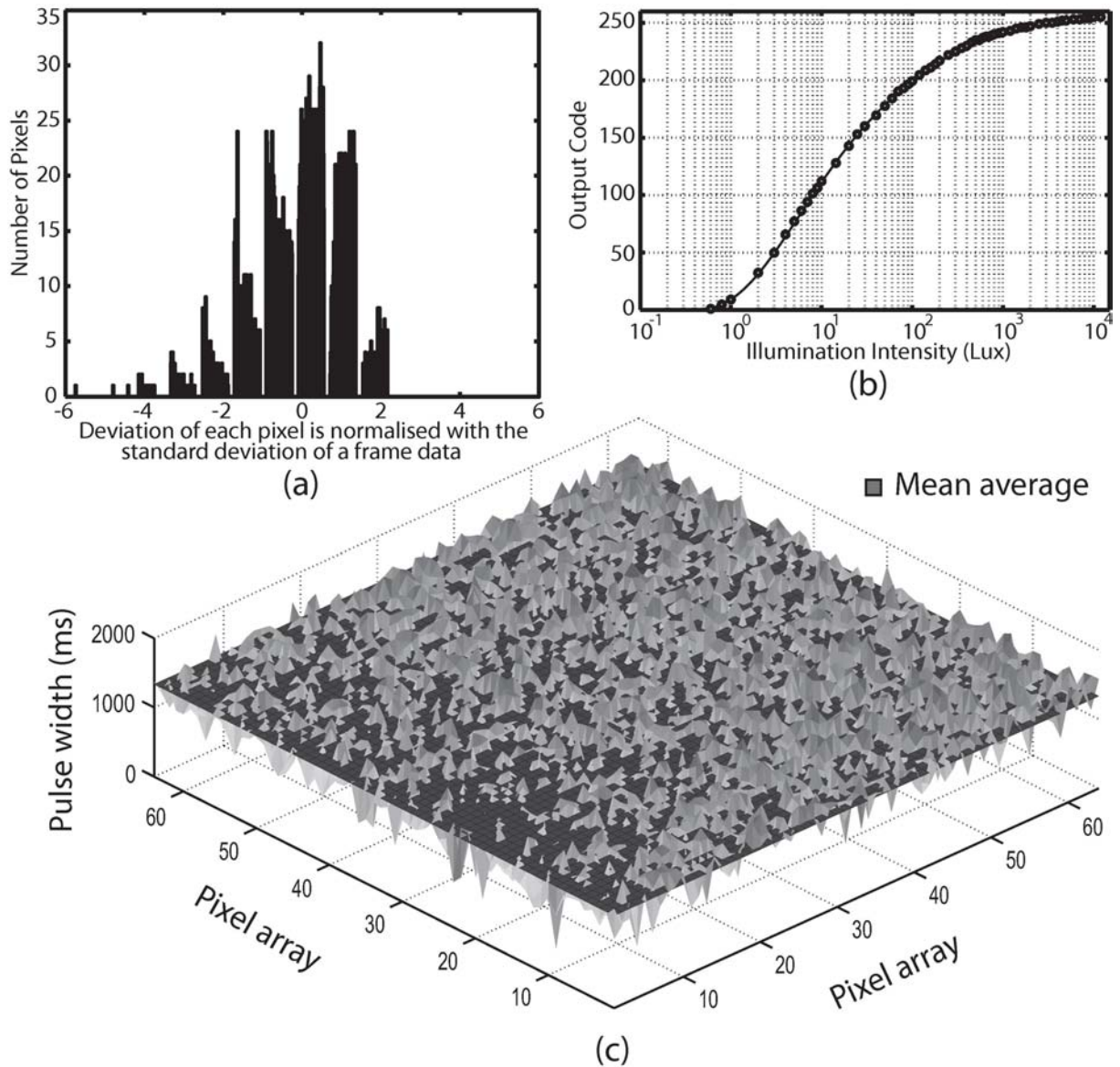
Figure 6.3. PWM CMOS imege sensor FPN and output code simulation. FPN measurements histogram showing number of pixels that has same deviation of the digital pixel value from a frame image, shown in (a). The curve in (b) demonstrates the pixel's output measurement. The 3D pattern in (c) illustrates the array's output under a fixed (dark) light pattern.

pixel consumption of approximately 27 nW. Hanson *et al.* (2010), in Table 6.2, used a current limiter for every pixel, so lower power consumption can be achieved. Simulation results of their circuit compare pixel response presented in this work shows that the inclusion of a current limiter in the pixel circuit reduces the output voltage swing of the comparator and it reduces the dynamic range. Although the approach presented by Hanson *et al.* (2010) consumes small energy, it has disadvantage a limited output voltage dynamic range, and requires an additional ramp signal generator as part of it operation.

6.2.2 Pulse-frequency modulation sensor

A new inverter-based pulse-frequency modulation (PFM) design is presented to reduce power consumption while keeping high dynamic range. The study shows that in comparison to previous published designs, the proposed design presents a 21% reduction in the mean value of total power consumption with a linear dynamic range of 119 dB. Simulations were performed using 0.13 μm technology and 0.75 V supply voltage.

The core part of a PFM sensor is an oscillator. One of the first oscillators is current-controlled oscillators. Due to a direct relation between frequency and power in these oscillators, a large amount of power will be consumed to produce a high rate frequency and, therefore, they are not suitable for biomedical applications. The conceptual schematic of the PFM digital pixel, which is also known as light-control oscillator (LCO), is shown in Figure 6.4 (a). When the voltage across the photodiode is recharged to V_{DD}, the V_{pd} voltage decreases in proportion to the incident light intensity. Once the V_{pd} reaches to the reference voltage level, V_{ref}, the comparator's output switches from a high voltage (logic "1") to a low voltage (logic "0").

The PWM can be achieved by removing the feedback loop and resetting the photodiode using an external input. One of the basic differences between the two structures is that there is no initial reset phase in PFM while in PWM the reset signal is controlled externally so the photodiode can be precharged to V_{DD}. The operation of a PWM structure can be defined as

$$T_{pd} = \frac{(V_{DD} - V_{ref})C_{pd}}{i_{tot}} \, , \tag{6.1}$$

Table 6.2. CIS performance comparison. Performance comparison betweeb this work and the other available PWM CISs.

	Lai *et al.* (2006)	Hanson *et al.* (2010)	Xu *et al.* (2002)	Bermak and Yung (2006)	This work
Technology (μm)	0.25	0.13	0.25	0.35	0.13
Pixel area (μm²)	9.4 × 9.4	5 × 5	12 × 10	50 × 50	5 × 5
# of transistors/pixel	10T (5N, 5P)	6T (5N, 1P)	5T (2N, 3P)	13T (7N, 6P)	6T (5N, 1P)
Photodiode	N-diff/P-sub	N-diff/P-sub	-	N-well/P-sub	N-diff/P-sub
Fill factor (%)	24	31	30	20	58
Dynamic range (dB)	76	68	71	90	83
V_{DD}	2.5-1.2	0.5	1.0	3.3	0.5
Avg. power/pixel	11 μW	357 pW	520 nW	10 mW	27 nW

where T_{pd} represents the discharge time of the photodiode capacitor, C_{pd}, node voltage, V_{pd}, from V_{DD} to V_{ref}, i_{tot} shows the total current which is the sum of photocurrent, i_{pd}, and dark current, i_d. Therefore, the pulse width of the comparator's output can be modulated as a function of the light intensity. Therefore, the comparator's output pulls the feedback node (fb) voltage down, so the photodiode is recharged to V_{DD} through the reset transistor, M_{rst}. This scheme shows a multiple-reset structure which reduces the photo-current saturation problem and produces a digital pulse frequency as a result of the iterative resetting scheme. Thus, the operation of a PFM structure then can be define as

$$f = \frac{i_{tot}}{(V_{DD} - V_{ref})C_{pd}} \, , \tag{6.2}$$

where f is the output frequency that acts as input clock for an n-bit in-pixel counter.

There are several advantages of using a PFM pixel. Firstly, the digital output is far more robust compared to its analogue counterpart in terms of the overall noise effects. Secondly, it is far less sensitive to the supply voltage scaling since the pixel directly converts the optical energy into the form of digital frequency, so the pixel's performance constraints are no longer dependent on the supply voltage range. This advantage significantly helps to increase both the dynamic range and linearity of the conversion (Bermak *et al.* 2002, Wang *et al.* 2006, Kagawa *et al.* 2004, Koppa *et al.* 2010, Park *et al.* 2010, Hinckley *et al.* 2002). These advantages motivated us to design a new PFM pixel that consumes less power, capable of real-time digital signal processing, and relatively high frame rate applications. Despite of all these advantages, there is a big disadvantage which is related to the fill-factor (FF) and fixed-pattern noise (FPN). The combination of p-type transistor, comparator, feedback circuitry, and the in-pixel counter ends up with a relatively low FF and larger pixel size. These drawbacks can increase the FPN level of PFM structures. Various approaches for designing a PFM image sensor are investigated. These approaches vary in terms of the main signal and feedback paths comprising components. A new design for an inverter-based PFM (iPFM) which consumes less power while meet a high dynamic range requirement is proposed. To obtain this efficient PFM, various Schmitt trigger gates are used in the main signal path and the power consumption and the dynamic range are investigated. Simulation results show that, the proposed design which uses a non-symmetric Schmitt trigger, Figure 6.4 (e), is a low-voltage PFM which can work at 0.75 V and have a low-power consumption along with a high dynamic range.

PFM sensors

Several parameters should be considered when choosing a comparator style image sensor. These parameters includes, offset, voltage gain variation, area, slow rate, minimum and maximum detectable illuminations, and low-voltage operation. An experimental study by Wang *et al.* (2006) shows a two-stage comparator and a symmetric OTA-based designs. These designs have variable reset delay and the reset delay of the Schmitt trigger is more constant. However, due to the Schmitt trigger high switching threshold, there is a need for higher integration time, and hence lower frame rate. Bermak *et al.* (2002) proposed an adaptation technique for digital pixel sensors using an in-pixel analogue-to-digital converter (ADC), which is the basis for the future 3D sensor structure presented in Figure 6.1. The adaptive integration approach is used to increase the dynamic range. As result, they improved the low-light performance of the PFM pixel by adapting a wider counting period. Furthermore, this approach enables a read-out speed of up to 1K frames/sec for a 32×32 array. This high frame rate obtained at a cost of 85 μW power consumption per pixel with 95% of this power is consumed in the counting period. They implemented the structure using 0.25 μm standard CMOS technology and a relatively large pixel size, 45×45 μm^2, indicating 23% fill-factor. Reference voltage of the comparator in their design was obtained internally, hence the supply voltage noise has less affect on the reference voltage, so the design is insensitive to the supply voltage variation. This feature is very important in the high-resolution images where the voltage variation sensitivity is significantly higher than low to medium resolution imagers.

In order to design a new low power PFM, previous designs were examined and possible potential improvements were identified. Firstly, a design that is shown Figure 6.4 (b) and is named "pix-conv1" in simulations (Kagawa *et al.* 2004). This design employs conventional inverters. In this design, all inverters are placed in the main signal path. The first two inverters in this chain are for discharging the photodiode and the last one is to reset the photodiode and start a new pulse. The other inverter that is out of the chain is just a signal shaping inverter. This design can be improved if the PMOS reset transistor is replaced with a NMOS transistor. This replacement helps having lower power consumption due to removing the short circuit current when the reset transistor is on, at the cost of using more silicon area. Note that a significant amount of consumed power is dissipated by the first inverter. Therefore, the first inverter could be replaced with a controllable conventional Schmitt trigger gate as in Figure 6.4 (c). In

this figure, only the main path is shown and the photodiode, reset transistor, and the feedback path are omitted to focus on the main part of the circuits, and named "pix-conv2". Simulation result shows that, in order to have a reasonable dynamic range similar to the conventional designs, the supply voltage should be 0.9 V. Therefore, this design consumes higher power because of the need for higher voltage drives. Furthermore, the standard deviation of power consumption is relatively high, as shown in Figure 6.5.

One idea that results in lower power consumption is inserting a simple inverter, as in Figure 6.4 (d) as "pix1." This design is also simulated and the results are reported for the comparison, in Figures 6.5 and 6.6. The simple inverter could be replaced by either a low power Schmitt trigger in Figure 6.4 (e) (Al-Sarawi 2002) or Figure 6.4 (f) (Zhang *et al.* 2003). The inverter-based PFM (iPFM) structure is a promising option for low-voltage operation and low-power applications such as implantable devices and mobile applications (Wang *et al.* 2006, Kagawa *et al.* 2004). A few types of iPFM pixels have been introduced in Kagawa *et al.* (2004), and Uehara *et al.* (2003) but despite all of these advantages, all of them suffer from two disadvantages: 1) Considerable power consumption, 2) Feedback inverters were placed in the main signal path. The design with the pix2 (Figure 6.4 (e)) circuit shows a better power consumption in terms of variation and mean value, as demonstrated in Figure 6.5. Figure 6.4 (d) and (e) illustrate the application of one single inverter and a low power Schmitt-trigger circuit in the design of a PFM pixel. According to the available information, the outcomes are novel and there is no available implementation using these approach.

Comparison of the PFM pixels

The proposed cell was simulated using mixed-signal CMOS 0.13 μm technology. The operational supply voltage is 0.75 V while the nominal V_{DD} is 1.2V. The feedback inverter chain is also operating at 0.75 V. The control transistor is shared between the three feedback inverters and is controlled using $V_{CTRL} = 0.6 \times V_{DD}$ (in Figure 6.4 (a)), while the reset supply voltage has been set to roughly the same value. Thus, the control signal can be directly connected to the reset supply voltage. Implemented layout that is shown in Figure 6.4 (e) demonstrates around 65% fill-factor. A larger photodiode helps in detecting lower light intensity.
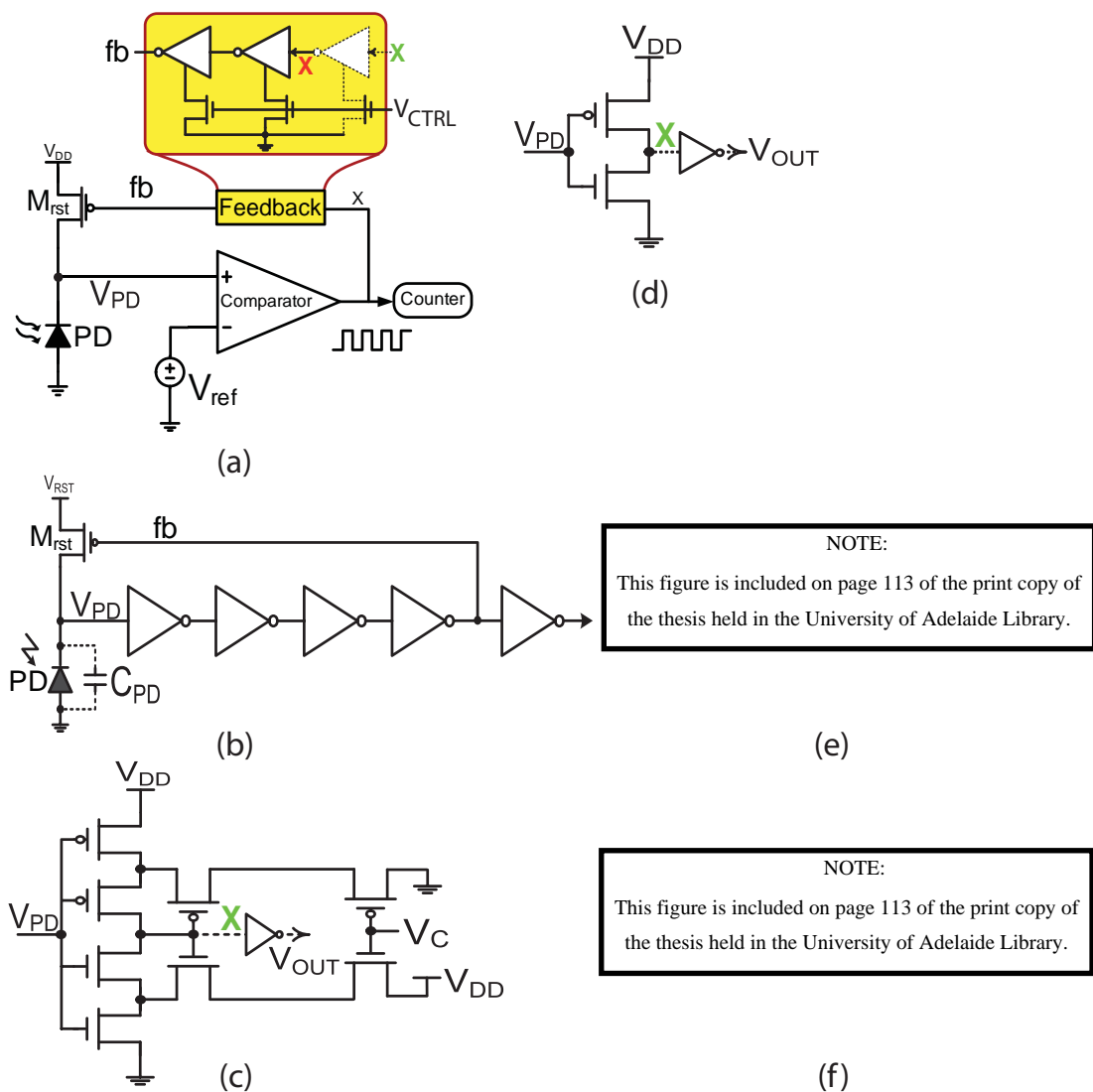
Figure 6.4. Generic schematic of a PFM pixel and circuit implementations. Pulse-frequency modulation pixels. (a) A generic implementation, indicating the feedback and the main path branches. The yellow box illustrates the feedback inverter chain. If the X signal is shown in green in (c)-(f) the signal passes three inverters and if it is red the signal passes only two inverters. Voltage control, V_{CTRL}, is applied to control the speed of feedback. (b) An inverter-based pixel with all inverters in the main path (pix-conv1) (Kagawa *et al.* 2004). (c) Schmitt-trigger circuit for replacing the comparator in (a). This is a conventional implementation of a Schmitt-trigger circuit (pix-conv2). (d) A single inverter implementation of the main path (pix1). (e) (From Al-Sarawi (2002)) and (f) (From Zhang *et al.* (2003)) show two types of low power Schmitt-trigger circuits to be used as a replacement for the first inverter. The designs are called pix2 and pix3 in simulations and experiments. This is the first try to combine the pix2 circuit in (e) with a PFM pixel implementation. A 10×10 μm^2 layout of the PFM pixel based on (e) is also shown.

A comparison is carried out among the cells in Figure 6.5. A post-layout simulation at 0.75 V shows better than 21% reduction in the mean value of total power consumption for the proposed structure while the dynamic range and the frequency response linearity are still comparable with the conventional design, as illustrated in Figure 6.6.
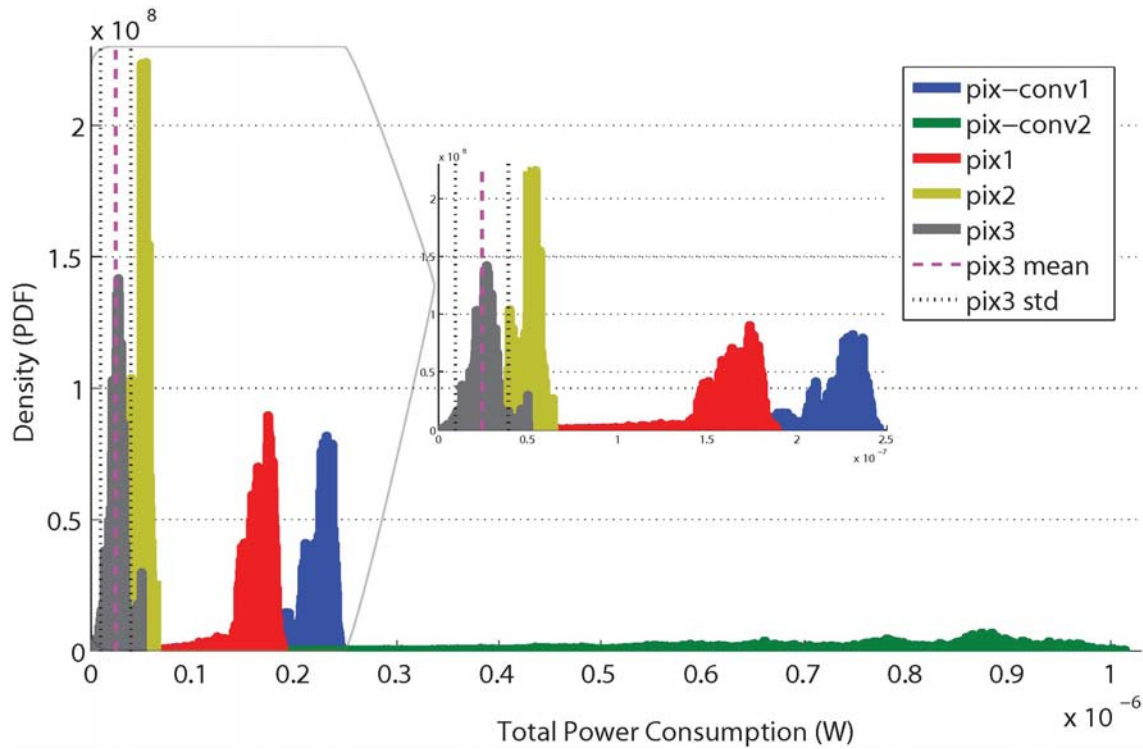
Figure 6.5. Power consumption analysis of the PFM pixels. Power dissipation of the PFM pixels in Figure 6.5 under a wide range of light intensities. It is clear that the pix2 (Figure 6.4 (e)) and pix3 (Figure 6.4 (f)) are far more improved than the other circuits in terms of both mean power dissipation and also predictability of power dissipation under a wide range of light intensities. The pix2 shows the lowest and the pix-conv2 demonstrates the highest deviation from their mean power consumption.

Low photodiode currents range are not shown in Figure 6.6. The simulations have been carried out using different light intensities. Low frequencies can be measured (from the actual fabrication) down to a few Hz but a linear frequency response corresponding to the log-scale light intensity (mW·cm^{-2}) starts around 100 Hz. Therefore, early results show a minimum (detectable) frequency of $f_{min} = 100$ Hz and $f_{max} = 50$ MHz, which results a 113 dB dynamic range. The simulations, however, only carried out in the range of 1 pA to 10 nA to get detectable frequency response from all the circuits. Moving towards high light intensities causes a large nonlinearity at the output pulse-width which should ideally keep a constant value. This nonlinearity then causes a significant

degradation in dynamic range, as Figure 6.6 shows the maximum detectable current for both of the designs is around 6.7 nA which corresponds to 60 MHz for the pix2. Clearly, the ratio of the low and high frequencies for all the circuits indicate very close results in terms of dynamic range. Therefore, the pix2 can be considered as a design that provides comparable dynamic range with lower power consumption. The pix3, however, shows a better overall performance in Figures 6.5 and 6.6. The main reason that the pix3 is not a good option is because of its layout complexity. Connecting body contacts of the MOSFET transistors to any other voltages than the lowest and highest potentials creates a significant complexity in terms of layout implementation[16] and also consumes more silicon area.
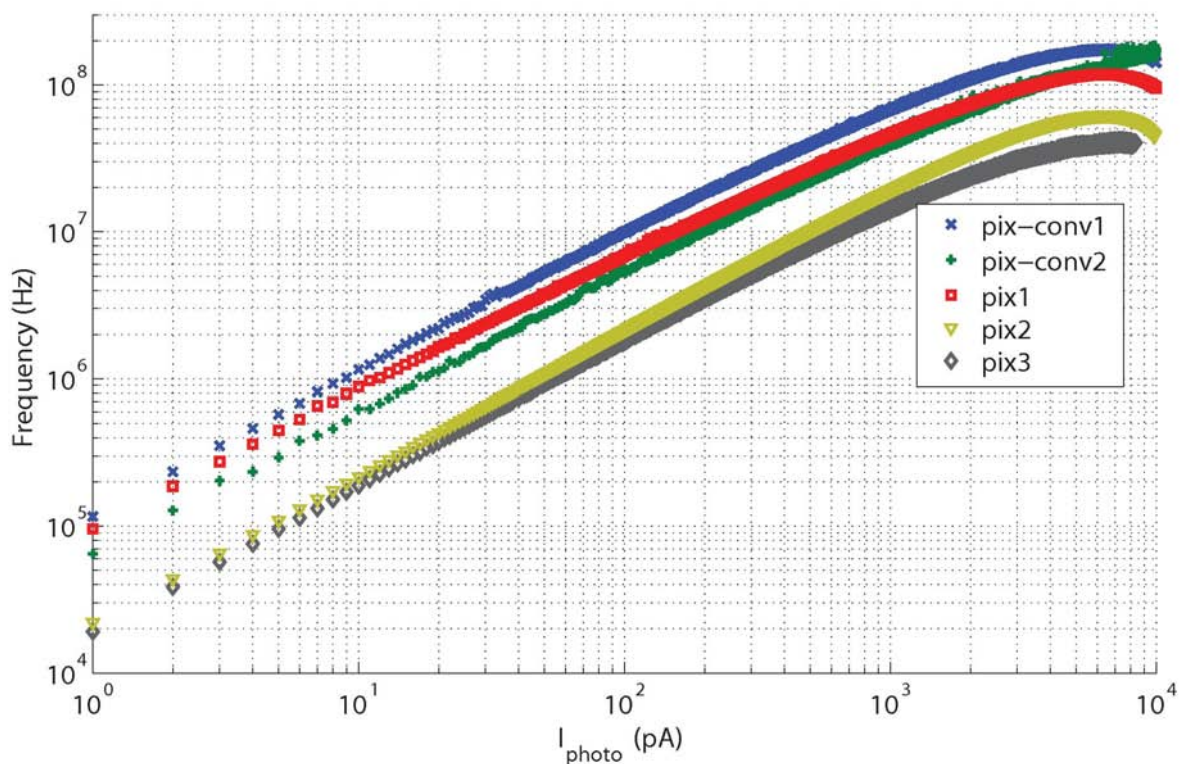
Figure 6.6. Frequency response of the PFM pixels. Dynamic range of the PFM pixels within the range of 1 pA to 10 nA photocurrent (plus dark current). Clearly, the ratio of the low and high frequencies for all the circuits indicate very close results in terms of dynamic range. Therefore, the pix2 can be considered as a design that provides comparable dynamic range with lower power consumption.

---

[16]This design implementation will not be possible in a single well structure.

6.3   Pattern matching system

Some of the more recent research on human-like vision is derived from the work of Hubel and Wiesel (1959) based on directional edge detection that forms the basic part of early information processing in the visual system. Most of the recognition algorithms like Gabor filters (Porat and Zeevi 1988), fractal-based texture extraction (Potlapalli and Luo 1998), and spatial spectroscopy-based approaches (Rudolph *et al.* 1998) are application oriented. A recent overview of a wide range of neuromorphic implementations can be also found in Indiveri *et al.* (2011). A more general purpose "human-like" image recognition approach proposed by Yagi and Shibata (2003) is based on the projected principal-edge distribution (PPED) algorithm. The algorithm consists of two steps: feature map generation followed by a vector formation. The result of the former step is used by an associative processor which can be a "neural-like" implementation. In the case of this research the matching processor, shown in Figure 6.7, is a memristor-based content addressable memory (CAM). The CAM implementation is discussed in Chapter 8.

The PPED architecture together with the proposed 3D hardware implementation strategy is conceptualised in Figure 6.7. Directional edge-based processing can be carried out using a directional convolution kernel. Experimental results for medical images and face detection and identification have highlighted that identification of four directional edges (horizontal, vertical, and +45 degree, and -45 degree) provide an acceptable method for creating feature vectors utilised for image matching, recognition, and classification (Shibata 2009).

Image data of 5×5 pixels obtained from an image sensor together with convolution kernels act as inputs. The image data flow for PPED algorithm (Yagi and Shibata 2003) and implementation approach are illustrated in Figure 6.8. For each of the directions, the convolution given by Eq. (6.3) is performed in parallel for both the positive and negative kernel weights, where $I_p(i,j)$ represents input data for pixel (i,j), the subscript dr refer to the direction (horizontal, vertical, -45 degree, and +45 degree), $\mathcal{K}_{\mathrm{dr}}(x,y)$ is the kernel data for pixel (x,y) and the specified direction, and $I^*_{\mathrm{dr}}(i,j)$ indicates output pixel data for the specified direction.

$$I^*_{\mathrm{dr}}(i,j) = \sum_{x=-2}^{2} \sum_{y=-2}^{2} \mathcal{K}_{\mathrm{dr}}(x,y) \times I_p(i+x,j+y) \, , \qquad (6.3)$$

Image Capture

PPED Vector Processor

Recognition

Back-illuminated CIS (BiCIS)

Edge Detection Filter

H +45° V -45°

Threshold Detector

Feature Map Memory

Feature Map Generator

Vector Construction Processor

Vector Storage

Matching Processor

Through-Silicon-Via (TSV)
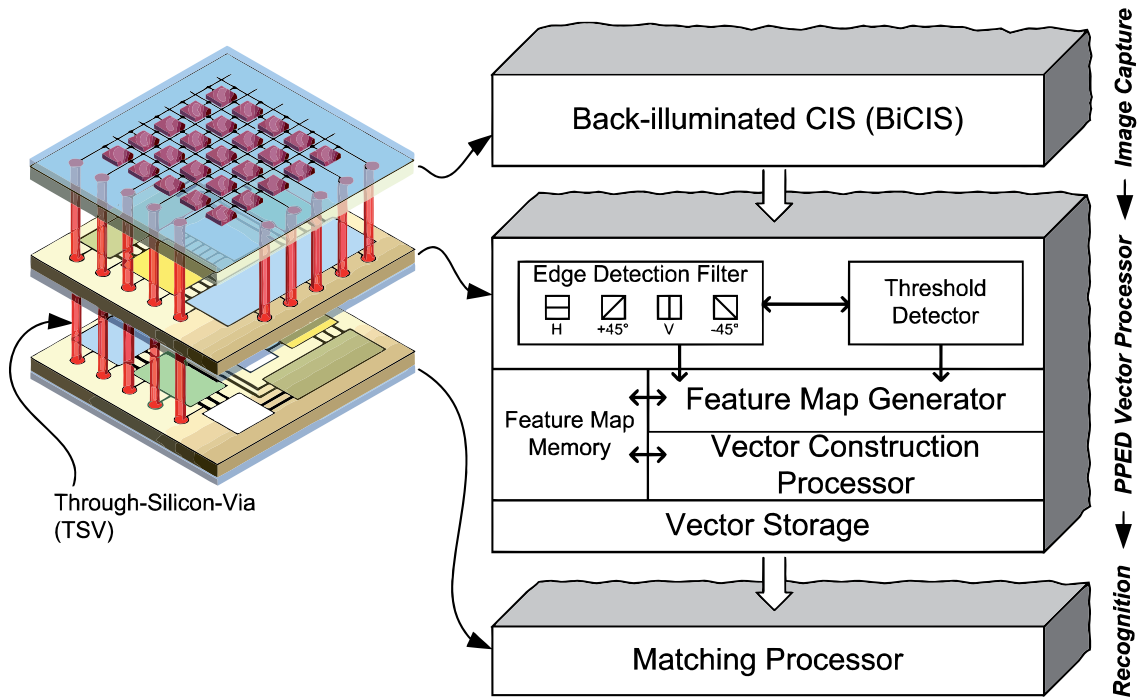
Figure 6.7. A system overview of the feature generation algorithm. 3D multilayered recognition system based on projected principal-edge distribution (PPED) algorithm as part of the system integration. The CMOS image sensor is a back-illuminated sensor which helps in increasing sensitivity and fill-factor (Hinckley *et al.* 2002). The matching processor is a memristor-based content addressable memory that is discussed in Chapter 8.

Each input pixel has 8-bit depth corresponding to a grayscale image. At each clock input, one "column" of the 5×5 input images, namely, 8-bit$\times$5 pixels is read and subsequently is applied to the image buffer. The reading procedure is repeated 4 times for the input image. For a seamless operation, the threshold $T_{th}(i,j)$ is available prior to presenting the image data $I_p(i,j)$ to the edge filter. Threshold values are determined from the differences in the absolute-value between neighbouring pixels. The median is used as the threshold value $T_{th}(i,j)$. For a 5×5 input pixels using the first horizontal and vertical nearest neighbours there is a total of 40 absolute-value differences. The median value of $T_{th}(\cdot)$ is derived from mixed-signal majority voting circuit defined by Eq.(6.4).

$$F_{dr}(i,j) = \begin{cases} 0 & : \quad \text{If} \quad \max_{dr}(I_{dr}^*(i,j)) < T_{th}(i,j) \\ 1 & : \quad \text{If} \quad \max_{dr}(I_{dr}^*(i,j)) \geq T_{th}(i,j) \, , \end{cases} \qquad (6.4)$$

where $F_{dr}(i,j)$ constitute the feature map for the edge flag buffer and forms the input to the vector formation processor. To generate a 1D projection, then the number of ones for each of the horizontal and vertical directions is counted. This results in 64-1D projections for the horizontal and vertical directions. The objective here is to map 64-1D vector projections for a 64×64 input feature map. In the next step the horizontal/vertical vectors are added in groups of 4 which imply that the output is 16 vectors for each of the horizontal and the vertical directions. Computation of ± 45 degree directions is more complex. Initially there are 128 vectors for the two diagonal directions. By taking an average, these vectors are reduced to 16, which subsequently result in 64 vector projections. The process is repeated in groups of four. At the completion of the step, smoothing operation takes place by averaging the results. The output of this step results in a series of 13-bit PPED vectors that present the edge-features of an input image by means of 1D vector projections. The same procedure using PPED algorithm is implemented to create the image templates. The matching and recognition is performed by the proposed bottom layer of matching processor shown in Figure 6.7. Therefore, the output is a (binary) vector that can be compared to the stored template data in the memory for pattern recognition and classification, for example. Note that the PPED is a rotation-invariant scheme that makes it suitable for any image recognition purposes.

6.4   Conclusion and extensions

A system overview of the proposed CMOS based imager with a layer of memristor was discussed in this chapter and the focus of this work within this system has been highlighted. The targeted system consists of a three dimensional multi-layer integrated circuit dice that are stacked on top of each other. As part of the targeted system, two CMOS image sensor structures, pulse-width and pulse-frequency modulations, are also discussed. The CMOS image sensors will be connected to a content addressable memory (CAM) structure which is introduced in Chapter 8. Besides the detail analysis of CMOS image sensors, a low-voltage operation, interface hardware layer between the image sensor and memristive layer were added for image feature generation. This algorithm generates a robust and one dimensional digital output vector that can then be sent to an associative memory for further processing.
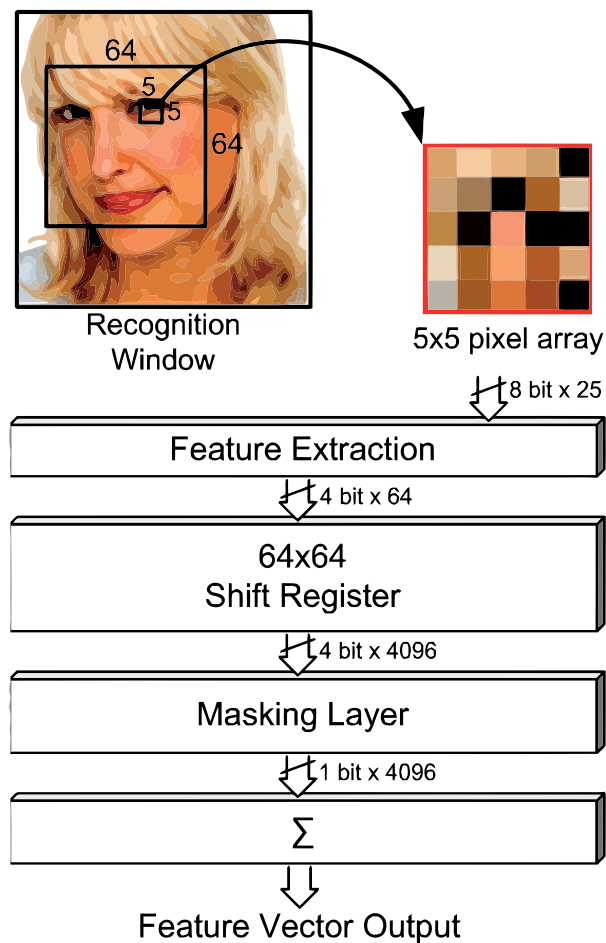
Figure 6.8. Projected principal-edge distribution (PPED) algorithm. Data flow model for feature vector generation using PPED algorithm (Yagi and Shibata 2003).

The next chapter provides a systematic approach for modelling large scale memristor and CRS arrays. This is important form this perspective that the targeted system, explained in this chapter, utilises an array of memristive devices for processing information and storage.

Chapter 7

Memristive Crossbar Architecture and Challenges

CONVENTIONAL memory technologies are challenged by their technological physical limits, as a result emerging nanometer scale technologies, driven by novel materials, are becoming an attractive option for future memory architectures. Among these technologies, RRAMs have created new possibilities because of their nano-features and unique *I-V* characteristics. One particular problem that dominates the maximum array size in this technology is interaction between neighbouring cells due to "sneak-path" currents during the READ and WRITE operations. Although the storage mechanism for Complementary Resistive Switch (CRS) based memory is fundamentally different from what has been reported for memristors, the device basics are similar. This chapter provides an analytical approach to the design of memristor and CRS-based memory array. The presented design methodology will assist designers in implementing CRS and/or memristive based devices for future memory systems.

[This page has been left blank intentionally.]

7.1   Introduction

Emerging memory technologies based on new materials have been widely accepted as alternatives to the current CMOS technology. These technologies are mainly classified into three subclasses: Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM), Phase Change Memories (PCM), and Resistive RAM (RRAM), that are shown in Table 4.1. Memory applications motivate the need for an evaluation of these technologies in terms of READ and WRITE bandwidth, latency, and energy dissipation. The International Technology Roadmap for Semiconductors (*ITRS 2009*), highlights that the performance characteristics of these emerging technologies are rather promising when compared with the current large memory arrays based on Static RAM (SRAM) constructs, particularly for large memory capacities. This suggests that emerging technologies, except PCRAM, will overtake advanced conventional Complementary Metal Oxide Semiconductor (CMOS) technology. We define a figure of merit as $E_R E_W \tau_R \tau_W N_{W,ref}$ for comparing these technologies—with greater emphasis on the access time—the parameters represent READ and WRITE energy (E_R, E_W), READ and WRITE latencies (τ_R, τ_W), and the number of refresh cycles ($N_{W,ref}$). This figure of merit indicates a significant improvement of RRAMs, MRAMs, and PCRAMs, over SRAMs for large memory capacities (> 1 GB) (*ITRS 2009*). The READ and WRITE access times of MRAMs show around 41% more and 48% less processing time than RRAMs. RRAMs introduce smaller cell size, $4F^2$/bit, where F is the lithographic feature size, see Figure 5.10 (c), with comparable endurance in comparison with the other memory technologies. Although a number of strategies that utilize diode and/or transistor cross-point devices are proposed, their fabrication is relatively more complex than a RRAM-based crossbar (Flocke and Noll 2007).

Although the memristor has introduced new possibilities for memory applications within the simple and relatively low cost crossbar array architectures, the inherent interfering current paths with neighbouring cells impose limitations on the array scalability, a necessary condition for large memory arrays (Linn *et al.* 2010). The imposed limitation was addressed by Linn *et al.* (2010) through the adaptation of two series memristive elements connected with opposing polarities, and discussed in Chapter 5. This structure is referred to as Complementary Resistive Switch (CRS) as shown in Figure 5.11. The unique aspect of this device is in using a series of high resistance states

(HRS) and low resistance states (LRS) to introduce logic "0" and logic "1". For example, a LRS/HRS combination represents "1" while a HRS/LRS state represents "0". Using this approach, the net resistance of the device is always around HRS, which helps in reducing sneak-path currents, which is the currents passing through neighbouring devices during the addressing process, and at the same time main path currents that passes through the addressed device. The advantage of using CRS as a fundamental element originates from its excellent READ voltage margin, even at small HRS to LRS ratios.

Along with addressing the parasitic current path issue, the importance of parasitic resistors also increases as F reduces. In a practical memory design, the line resistance of a nanowire can be calculated as $R_{\text{line}} = \rho_{\text{metal}}(0.2n/F)$, where n is the number of cells in the line and ρ_{metal} is the resistivity of metal, which is a function of F (Zhirnov *et al.* 2010). Therefore, a mathematical model is developed to consider the nanowire parasitic resistances in a matrix based analysis of cross-point arrays.

In this chapter Section 7.2 describes crossbar memory array and its nano and CMOS components. Also introduces a comprehensive approach for memristive-based crossbar array modelling. Two memristive-based arrays, memristor-based and CRS-based, are discussed in this section. Simulation results and also statistical analysis of these two memristive arrays are provided in Section 7.3. Section 7.4 discusses the simulation results.

7.2   Crossbar memory array

The crossbar structure shown in Figure 7.1 (a) is used to construct the memory array. The cross-point element could be either a CRS device or a memristor. In order to read any stored bit in $R_{i,j}$, similar to many other reported schemes (Amsinck *et al.* 2005, Flocke and Noll 2007, Flocke *et al.* 2008, Shin *et al.* 2011a), here we apply $V_{\text{pu}} = V_{\text{READ}}$ to the ith bit-line, j^{th} word-line is grounded, and all other word and bit lines are floating. A direct benefit of this approach is the pull-up resistor (R_{pu}) can be implemented in nano domain Flocke and Noll (2007), and Flocke *et al.* (2008). Then, the stored state of the device then can be read by sensing V_{oi} using CMOS sense amplifiers (SAs). Reading "1" creates a current pulse, and as a consequence, a voltage pulse appears on the middle electrode. Note that the CRS read-out mechanism does not rely on sensing the

Table 7.1. CRS and memristor device parameters. Parameters of the memristive and CRS cross-point junctions and array structure. * Array type: (M) Memristor-based, (C) CRS-based, (B) Applicable for both. † Assumed that bit-lines are directly connected to sense amplifiers (SAs) and there is no R_{sel} in between. ‡ Assumed that these resistors are implemented in nano domain. Transistors in Figure 7.1 are used to express a more general form of a hybrid nano/CMOS memory. $^{\triangleright}$ Lumped parasitic resistance of an activated pull-down.

Parameter	Value	Array*	Description
R_{LRS}	100 kΩ	(M)	low resistance state
R_{LRS}	200 kΩ	(C)	low resistance state
R_{HRS}	100 MΩ	(B)	high resistance state
r	10^3	(M)	resistance ratio
R_{b}	100 Ω	(B)	input resistance of SA†
R_{w}	100 Ω	(B)	pull-down resistance$^{\triangleright}$
R_{pu}	R_{LRS}	(B)	pull-up resistor‡
r_{W}	1.25 $\Omega/\square$	(B)	parasitic resistor
$V_{\text{th,SET}}$	2.2 V	(M)	SET threshold
$|V_{\text{th,RESET}}|$	1.8 V	(M)	RESET threshold
V_{READ}	1 V	(M)	READ voltage
V_{WRITE}	2 V	(M)	WRITE voltage
$|V_{\text{th,SET}}|$	2.4 V	(C)	SET threshold
$|V_{\text{th,RESET}}|$	3.6 V	(C)	RESET threshold
V_{READ}	2.8 V	(C)	read voltage
V_{WRITE}	3.8 V	(C)	write voltage

middle electrode (ME) and this electrode is floating. The read-out mechanism detects the affect of this current pulse on the bit-line's nanowire capacitor and sense then using an array of SAs.

Although for memristors the WRITE operation dominates because of its relatively high voltage/current, for CRS device the READ current dominates the current level. Therefore, in our case, the READ operation analysis for energy consumption and performance characteristics is more critical than WRITE operation. Consequently, the READ and WRITE simulation results are discussed here. Table 7.1 highlights the cross-point junction and array parameters.
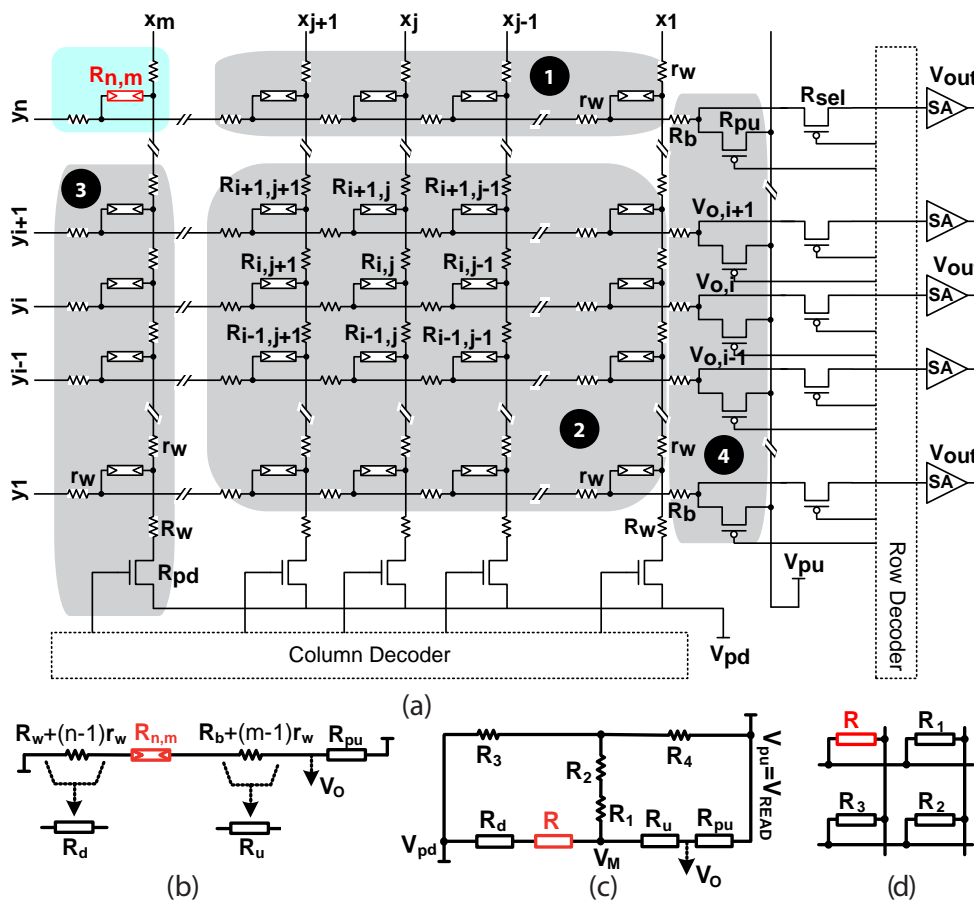
Figure 7.1. Crossbar array and its simplified models. Typical $n \times m$ crossbar array. (a) A hybrid nano/CMOS circuit. Columns show word-lines and rows identify bit-lines. Each $R_{i,j}$ show resistive elements that can be a memristor or a CRS device. Nanowire segment resistance is shown by $r_{\mathrm{w}} = R_{\mathrm{line}}/n$ (if $n = m$) and the connection between the nanowire and word-line is shown using R_{w}. Similarly the bit-line resistance indicated by R_{b}. According to the model discussed in Section 7.1, unit resistance of a bit/word line (nanowire) for $F = 100$ nm and $n = 64$ is around 1 Ω while it is increased to 32 Ω if F reduces to 5 nm, which is in consistency with the unit resistance that is reported in *ITRS (2009)* (1.25 Ω). The segment resistance of $r_{\mathrm{w}} = 1.25$ Ω is taken in our simulations. The pull-up resistors, R_{pu}, can be implemented in nano domain. The triangular shape at the output shows a CMOS amplifier that is assumed to have an acceptable sensitivity (ΔV or ΔI) range of > 100 mV. While READ process is in progress appropriate signals provided by decoders directs $V_{\mathrm{o},i}$ to $V_{\mathrm{out},i}$. Stored pattern in groups (1), (2), and (3) can be identifed by R_{X1}, R_{X2}, and R_{X3}, respectively. (b) The (n^{th},m^{th}) cell that can be identified in red color is the worst case possible cell for any READ and WRITE schemes. This circuit does not consider sneak-path current. (c) Equivalent circuit for the READ scheme with sneak-path and parasitic nanowire resistors considerations. (d) Schematic of a 2×2 array that is a good approximation to the array according to the grouping.

The WRITE scheme that is used is the common accessing method in which the ith bit-line is pulled up, the jth word-line is grounded, and the other lines are all connected to $V_{\text{w}}/2$, where V_{w} is the WRITE voltage. This voltage should be high enough to create sufficient voltage difference across the target cell and at the same time having no unwanted affect on the other cells that mainly see a $V_{\text{w}}/2$ voltage difference. A control mechanism for the WRITE process is introduced by Ebong and Mazumder (2011a).

To analyse the structure, we need to provide a simplified equivalent circuit for the crossbar structure, as can be seen in Figure 7.1 (b) and (c). Note that $V_{\text{MEM,READ}} < V_{\text{CRS,READ}}$ and $V_{\text{th,SET}} < V_{\text{CRS,READ}} < V_{\text{th,RESET}}$. Figure 7.1 (c) illustrates the equivalent circuit considering sneak-path currents for the both memristive and CRS-based array. For the sake of simplicity, two series resistors, R_1 and R_2, are evaluated separately.

The resistor value for the memristive-based and CRS-based circuit can be written as,

$$R_1 = \frac{R_{\text{X1}}}{(m-1)} + r_{\text{w}} , \tag{7.1}$$

$$R_2 = \frac{R_{\text{X2}}}{(m-1)(n-1)} + r_{\text{w}} , \tag{7.2}$$

$$R_3 = \frac{R_{\text{X3}} + R_{\text{d}}}{(n-1)} , \tag{7.3}$$

$$R_4 = \frac{R_{\text{pu}} + R_{\text{u}}}{(n-1)} , \tag{7.4}$$

where R_{X} represents the array's stored pattern in three different groups as seen in Figure 7.1 (a). For the worst case READ or WRITE in a memristive array $R_{\text{X1}} = R_{\text{X2}} = R_{\text{X3}} = R_{\text{LRS}}$ and for a CRS array $R_{\text{X1}} = R_{\text{X2}} \equiv$ logic "1" or logic "0", whereas $R_{\text{X3}} \equiv$ logic "1". Although a worst case cell selection is considered here, due to the harmonic series behavior of the overall parallel parasitic resistance, increasing R_{LRS} and/or decreasing the array size, $n = m$, results in better agreement with the analytical approximation for R_1 and R_2. These equations then can be used for evaluating the impact of parasitic current paths and parasitic nanowire resistors on the array performance.

The worst case pattern is assumed to be applied when $R_{\text{LRS}} \equiv$ logic "1" for either memristive or CRS arrays. In this case, we have the most significant voltage drop because of the both parasitic paths and elements. Therefore, a pattern of either logic "0" or "1" for all the elements except those on j^{th} word-line (x_j) is assumed, which is roughly equivalent to a HRS resistance for a CRS device, $R_{\text{CRS,HRS}} = R_{\text{HRS}} + R_{\text{LRS}}$. A close look at Figure 5.13 (a) and (c) shows if the stored logic in all the CRS devices along x_j, which may or may may not include $R_{i,j}$, is "1" (LRS/HRS), so applying a V_{READ} can

change their states to an ON condition (LRS/LRS). Therefore, during the READ time, $n - 1$ devices along x_j comprise the ON resistance, $R_{ON} = 2R_{LRS}$, in our simulations. Therefore, for a CRS array, $R_{X1} = R_{X2} = R_{HRS} + R_{LRS}$ and $R_{X3} = 2R_{LRS}$.

Sizing of the pull-up resistor, R_{pu}, as part of the nano domain implementation is a very important factor. For instance, low R_{LRS} devices, e.g. magnetic tunneling junctions (MTJs), interconnection impedance should be also taken into account, whereas in RRAMs, the LRS resistance is normally $\gtrsim 100$ kΩ (Yi *et al.* 2011). Therefore, this equivalent circuit provides a generalised form for a nano-crossbar array. In other words, if $R_{LRS} \gg (n + m)r_W$, the nanowire overall resistance will be negligible. These considerations along with taking low output potential, V_{OL}, and high output potential, V_{OH}, lead to an optimal value for R_{pu}. We first follow the conventional approach without considering parasitic currents and the nanowire resistors. Note that in a more precise analysis, the sense amplifier's sensitivity is also important to be considered (Zhirnov *et al.* 2010). In this situation have,

$$V_{OL} = \frac{R_L}{R_L + R_{pu}} V_{pu} , \tag{7.5}$$

$$V_{OH} = \frac{R_H}{R_H + R_{pu}} V_{pu} , \tag{7.6}$$

where for a memristive array $R_L = R_{LRS}$ and $R_H = R_{HRS}$, whereas for a CRS array $R_L = 2R_{LRS}$ and $R_H = R_{HRS} + R_{LRS}$. These equations are applicable for both of the arrays (memristive and CRS array). Read margin (RM) is defined as $\Delta V = V_{OH} - V_{OL}$. An optimal value of R_{pu} can be extracted from $\partial \Delta V / \partial R_{pu} = 0$. For a memristive array, $R_{pu,MEM} = R_{LRS}\sqrt{r}$, where $r = R_{HRS}/R_{LRS}$. Taking parasitic resistors into account (e.g. MJTs), and neglecting sneak-paths, results in $R_{pu,MEM} = \sqrt{rR_{LRS}(R_{LRS} + (n + m)r_W)}$ as an optimal value for the load resistor. For a CRS array,

$$R_{pu,CRS} = R_{LRS}\sqrt{2(1 + r)} . \tag{7.7}$$

A generalised form can be achieved by solving two Kirchhoff's current laws (KCLs) for the equivalent circuit (Figure 7.1 (c)). Therefore, if $R_{12} = R_1 + R_2$ and

$$x = \frac{R_{12}}{R_4} + \frac{R_{12}}{R_3} - 1 , \tag{7.8}$$

$$y = \frac{1}{R + R_d} + \frac{1}{R_{pu} + R_u} - \frac{1}{R_{12}} , \tag{7.9}$$

$$V_M = \frac{R_{12}(xR_4 - (R_{pu} + R_u))}{R_4(1 + xyR_{12})(R_{pu} + R_u)} V_{pu} , \tag{7.10}$$

$$V_O = \frac{R_u}{R_{pu} + R_u}(V_{pu} - V_M) , \tag{7.11}$$

where R is a memristor or CRS device to be read. This is similar to the ideal condition, $R_{LRS} \Rightarrow V_{OL,MEM}$, $2R_{LRS} \Rightarrow V_{OL,CRS}$, $R_{HRS} \Rightarrow V_{OH,MEM}$, and $R_{HRS} + R_{LRS} \Rightarrow V_{OH,CRS}$. A numerical approach helps designers to identify an optimal value for R_{pu}. The significance of this analytical model can be highlighted using a comparison between the optimal values for R_{pu} calculated through Eqs. (7.5) and (7.6) and the optimal value calculated via Eq. (7.11) and if parasitic resistors are negligible then Eq. (7.10). The optimal value for a memristive array, neglecting sneak currents and parasitic resistors, is around 3.16 MΩ using data from Table 7.1. These parameters are strong function of array size (n and m) and R_{LRS}. In practical designs, R_{pu} optimal increases as $n\ (= m)$ increases. This rate of change can be significantly reduced by a high R_{LRS}. This study shows $R_{LRS} > 3$ MΩ results in a significant reduction in dependency of the optimum value to the array size. This analytical approach also indicates that in our case $R_{pu} \approx R_{LRS}$ for CRS and memristive arrays.

This chapter calculates the voltage pattern using $2mn$ linear equations from a $n \times m$ array. This mathematical framework can be easily implemented using KCL equations in a matrix form. Figure 7.2 demonstrates the schematic of how KCL equations work in the two plates. Basically, it shows that for $1 < (i$ and $j) < n\ (n = m)$,

$$g_w V_{B1,i} + g_w V_{B2,i} = G_{i,j} V_{i,j} , \tag{7.12}$$

$$g_w V_{W1,j} + g_w V_{W2,j} = -G_{i,j} V_{i,j} , \tag{7.13}$$

where $g_w = 1/r_W$, $G_{i,j} = 1/R_{i,j}$, $V_{B1,i} = V_{B,i,j+1} - V_{B,i,j}$, $V_{B2,i} = V_{B,i,j-1} - V_{B,i,j}$, $V_{W1,j} = V_{W,i+1,j} - V_{W,i,j}$, $V_{W2,j} = V_{W,i-1,j} - V_{W,i,j}$, and $V_{i,j} = V_{B,i,j} - V_{W,i,j}$. Therefore, there are $2mn$ unknowns and $2mn$ equations. Depending on the READ scheme, the first and last rows (word-line) and columns (bit-line) should be treated differently.

Figure 7.2. Crosspoint memory element between two plates of bit and word lines. A schematic of an interconnection network in a crossbar array to illustrate the two KCL equations that can be achieved from both bit-line and word-line plates. Generally, current flow through a cross-point device from the ith bit-line is $I_{\text{B},i} = I_{\text{B1},i} + I_{\text{B2},i}$, similarly for the jth word-line is $I_{\text{W},j} = I_{\text{W1},j} + I_{\text{W2},j}$.

Although, the impact of multiple parasitic currents and nanowire resistors are studied in the literature (Liang and Wong 2010, Flocke and Noll 2007), a comprehensive analytical approach to address these issues, for the both memristive and CRS arrays, is lacking and it is this issue that is addressed in this section.

7.3 Simulations of the crossbar array

Extensive analytical studies have been carried out in the area of nano crossbar memory design (Flocke and Noll 2007, Flocke *et al.* 2008, Liang and Wong 2010, Shin *et al.* 2011a, Amsinck *et al.* 2005). These studies are extended here and also the comprehensive analytical framework, introduced early in this section, to the simulation of the memristive and CRS-based memory arrays.

For simulations in this chapter, a range of rectangular array sizes from $n = 4, 16$, and 64 ($n = m$) and three input patterns, the best case, the worst case, and a random pattern are considered. Parameter values can be found in Table 7.1 and the simulations results are as reported in Table 7.2. If $\Delta V \geq 100$ mV is used for the CMOS amplifiers, $\Delta V / V_{\text{pu}} \geq$

Table 7.2. Crossbar simulation results. Memristor and CRS crossbar array simulation results for the best, worst, and random patterns in Figure 7.5.

Array	$\frac{\Delta V}{V_{\text{READ}}}$ (%)		Energy (pJ)	V_{READ}
	MEM ($> 10\%$)			
16×16	Worst	2.3	32.1	1 V
16×16	Best	52.6	4.0	1 V
16×16	Random	5.5	26.9	1 V
64×64	Worst	0.45	127.0	1 V
	CRS ($\geq 3.6\%$)			
16×16	Worst	19.8	119.9	2.8 V
16×16	Best	24.3	20.8	2.8 V
16×16	Random	21.2	89.0	2.8 V
64×64	Worst	9.5	483	2.8 V

10% for memristors and $\Delta V / V_{\text{pu}} \geq 3.6\%$ for CRS are chosen. The only valid case for store pattern using memristor array is (16×16), while all the results for a CRS array are valid. This study shows that a memristive array needs substantial reduction in the amount of sneak leakage currents to be an appropriate candidate for the future memory applications if R_{LRS} values are in the order of kΩ.

For a worst case pattern in a CRS-based array, the $(16 \times 16) - 1$ bits are initially programmed at their LRS/HRS state (R_{X1}, R_{X2}, and R_{X3}), which is effectively equivalent to a HRS state. There is only 1 bit in the target word-line that programmed with different logic value and this is just to be able to read V_{OH} and V_{OL} at the same time. Figure 7.3 illustrates the condition for a worst case occurs when applying an appropriate READ voltage (here 2.8V) and 15 CRS devices switch to their R_{ON} state, which makes a significant difference in terms of the maximum amount of current that can pass through the device. Consequently, this is the main source of power dissipation for a CRS array. Similar scenario were observed for a 64×64 array.

Figure 7.4 illustrates voltage pattern for a 64×64 CRS array for reading 32th word-line. The magnitude of voltage peak above the settled voltage surface for unselected cells shows a successful READ process. Similar approach can be taken for WRITE process to show that the minimum requirement (at least the programming threshold voltage) is met on the selected cell(s).
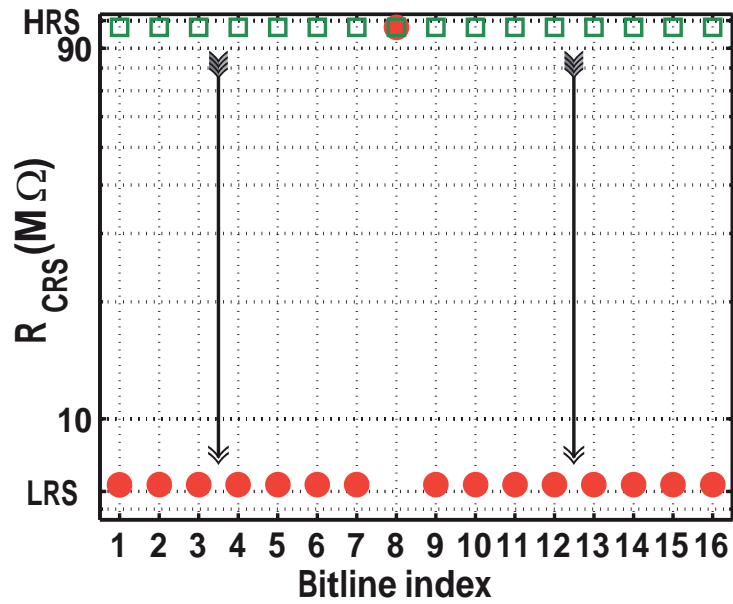
Figure 7.3. CRS resistance switch from a logic state to ON. Resistance switch in a column of CRS devices, green rectangular and red circles are the resistance states before and after READ operation, respectively.
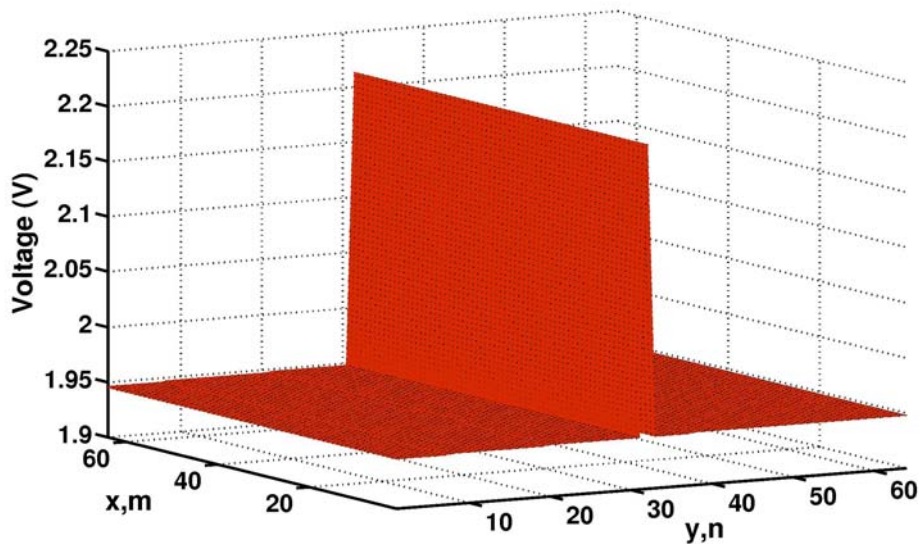
Figure 7.4. Voltage pattern across a CRS array. Voltage pattern across a 64×64 CRS crosspoint array after addressing.

By analysing the results for a range of array sizes from 4×4 to 64×64, it is observed that to gain an appropriate and nondestructive READ V_{READ} for memristors should be set to 1 V. This is an intermediate voltage and is low enough to avoid significant change in the device internal state and is high enough to drive a (64×64) array for the last or worst case selected cells. Our simulations indicate that a relatively high LRS (> 3 MΩ, as reported in Liang and Wong (2010)) guarantee enough read margin as well as sufficient potential across a selective cell for a successful WRITE operation when $r > 2$. Therefore, the negative contributions of nanowire parasitic resistors and parasitic (sneak) path currents that are responsible for voltage drop on the selected lines can be both significantly mitigated to a negligible level by increasing R_{LRS} and maintaining r at a level to guarantee a distinguishable high and low state outputs, whether in terms of ΔV or ΔI.

Endurance requirement[17] in the CRS will be relaxed by utilising a nondestructive and scalable read-out techniques, which significantly reduce the total number of refreshing cycles. A nondestructive readout approach for CRS-based arrays can be found in Tappertzhofen *et al.* (2011).

7.3.1   Statistical analysis

Recent study on memristive switching behaviour indicates that there is also a lognormal (long tail) distribution associated with LRS switching (SET) (Yi *et al.* 2011). This certainly reduces the impact of interconnection resistors due to the fact that a significant portion of low resistor states have higher values than the nominal R_{LRS}, however, the impact of such distribution on the device switching speed is significant. The lognormal distribution has been also seen in the switching time RRAMs (Medeiros-Ribeiro *et al.* 2011). However, despite extensive research about the mechanism that causes the lognormal distribution, this area is still under intensive discussion (Medeiros-Ribeiro *et al.* 2011).

---

[17]An endurance of 10^{15} cycles is required to either replace SRAM or DRAM (*ITRS 2009*). There is also an inverse relationship between endurance and data retention. To support reliable large array products, memory technologies must be able to retain data over a long lifetime (> 10 years at 85 centigrade) with a low defect rates.
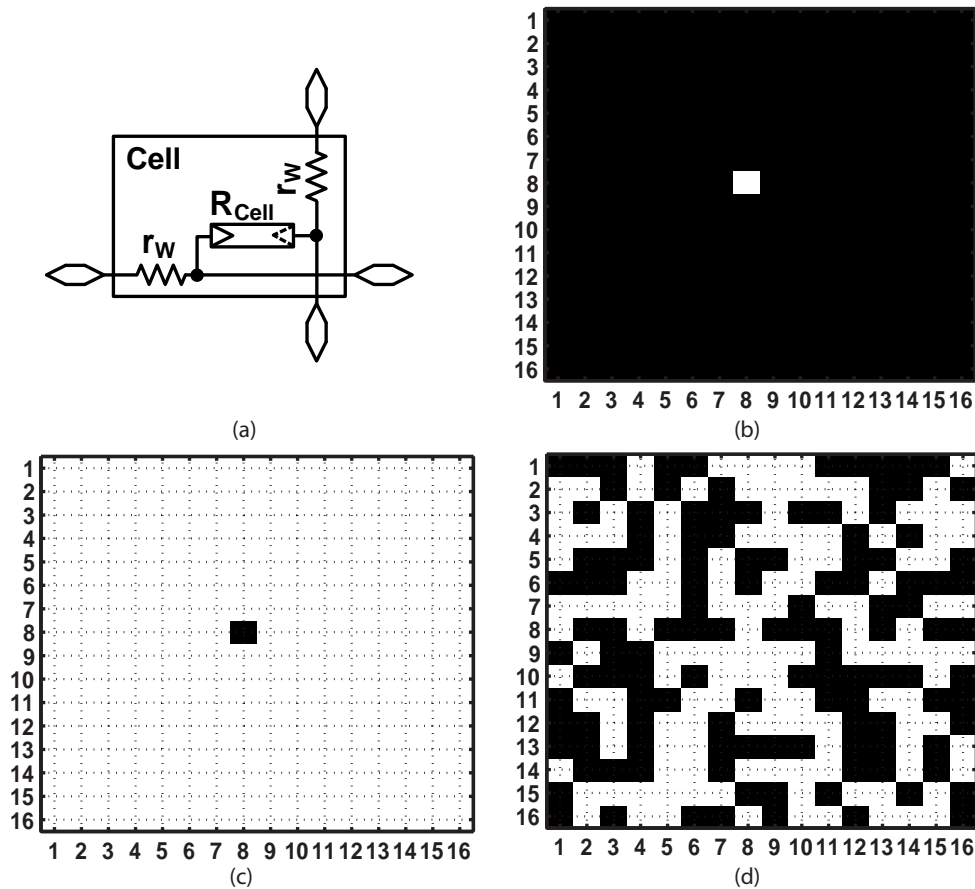
Figure 7.5. Crosspoint cell and patterns for simulations. A cross-point cell for simulation and input patterns. (a) Cross-point cell. Horizontal line shows bit-line and vertical wire illustrates word-line. (b) A possible best case in terms sneak-paths for reading 8th word-line. A pattern that all the 16 bits in this word are programmed at their OFF state and there is only one bit with ON state resistance (LRS) is assumed. The worst case possible is to read from or write in the last word-line. (c) A possible worst case. (d) A random pattern. In all cases, reading the 8th column is the target. One bit is initially programmed with different logic to be able to analyse read margin efficiently. It is worth mentioning that these cases are all relative worst and best cases for comparing the two technologies. A worst case for reading "1" occurs if selected word line contains only cells with R_{HRS} and the rest of the array are at R_{LRS}. Worst case for reading "0" and writing happen when all the resistive elements are at their R_{LRS} state. For a CRS array, if the array under test is initially programmed to store "0" for all the cells on selected word line and "1" for the rest of the array, worst case for reading "1" occurs, otherwise if the array stores only "1" logic then the worst case for WRITE operation and reading "0" occurs.

An analysis has been carried out on a 4×4 memristive and a 16×16 CRS array sizes through 1000 Monte Carlo simulations to observe the impact of the uncertainty associated with R_{LRS}, device process variation, spatial randomness of the initial state programming, and unfixed applied voltages. The ON state lognormal distribution data is extracted from Yi *et al.* (2011) while a Gaussian distribution is assumed for the the line edge roughness (LER) for devices, nanowires, and variation on the applied voltages. According to Hu *et al.* (2011), $(-3\sigma, +3\sigma) = (-5.4\%, 4.1\%)$ LER and $(-5.5\%, 4.8\%)$ thickness fluctuations is assumed for the both R_{LRS} and R_{HRS}. It is assumed that the normal distribution for initial state programming with 6σ variation is 5% is also assumed. Figure 7.6 demonstrates that the CRS array's output is less sensitive to the overall uncertainty, whereas the memristive array is widely spread out. Minimum value for CRS and memristor arrays are 15% and 1%, respectively. As discussed earlier, $\Delta V / V_{pu} \geq 3.6\%$ for the CRS cross-point and $\geq 10\%$ for the memristor array are acceptable. Table 7.2 has already shown that CRS array stored data pattern sensitivity is much less (11 times) than the memristive array. Similarly here, while a memristive array read margin is far less than 10%, a CRS array guarantee 12% margin.

In Hu *et al.* (2011) the impact of such variations is defined as $R_{XRS} \cdot \theta_{Th} / \theta_{LER}$, where R_{XRS} is either LRS or HRS resistance and the $\theta_{Th} / \theta_{LER}$ defines the thickness fluctuations over LER variation. The HRS resistance in a TiO_2-based memristor is less affected by the overall variation, whereas LRS variation shows a significant deviation from its nominal value. Likewise, since CRS overall resistance of the ON state is $2R_{LRS}$, so it is less affected by such variation.

7.4   Discussion

Results of simulations indicate that the most important parameter that should be increased to achieve higher array sizes for a memristive array is R_{LRS}. This research verify that a high r ($= R_{HRS} / R_{LRS}$) does not necessarily improve the substantial amount of parasitic path currents, while a higher R_{LRS} value guarantees a successful READ and WRITE operations. This improvement can be achieved at the cost of increasing the access time.

In a CRS-based cross-point, the results is more significant since for a high R_{LRS} the effective resistances of HRS and LRS are significantly increased. Assuming a high
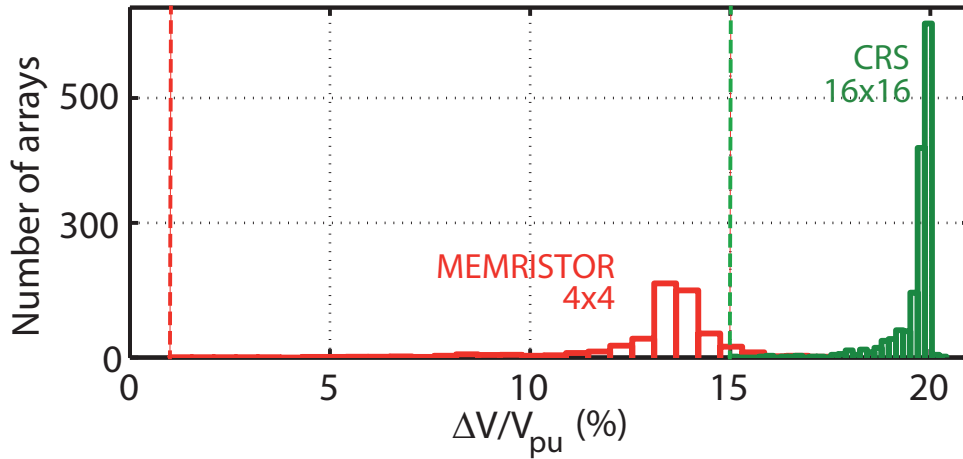
Figure 7.6. Variation analysis of memristor and CRS arrays. The uncertainty associated with LRS, nanowires process variation, and nonideal initial state programming impact on memristor and CRS array by 1000 simulation runs, so 1000 arrays. The red and green lines illustrate minimum read margin for the memristive cross-point and CRS array, respectively. The y-axis shows the number of arrays out of the total 1000 arrays.

$R_{\text{LRS}} = 3$ MΩ, $R_{\text{HRS}} = 12$ MΩ ($r = 4$), and $V_{\text{READ}} = 1$ V, READ operation results in a $\Delta V > 300$ mV. Analytically, the read margin (RM) does not depend on the absolute values of LRS or HRS resistances rather on their ratio, and RM can be calculated using,

$$\text{RM}_{\text{MEM}} = \frac{1 + r - 2\sqrt{r}}{r - 1} \, , \tag{7.14}$$

which means for a 100 mV limitation $R_{\text{HRS}}/R_{\text{LRS}}$ ratio should be ≥ 1.3. Similarly the simulations results show that such high value assumption for R_{LRS}, RM for CRS-based devices can be written as

$$\text{RM}_{\text{CRS}} = \frac{(r - 1)\sqrt{2(1 + r)}}{4(1 + r) + (3 + r)\sqrt{2(1 + r)}} \, , \tag{7.15}$$

which results $r \geq 1.15$ ($> 3.6\%$) minimum requirement for a successful READ.

Our study also shows that for similar WRITE and READ access time and high R_{LRS} values, energy dissipation ratio of a CRS array over a memristive array constantly increases. The total power dissipation for an operation can be calculated using

$$P_{\text{total}} = P_{\text{nano}} + P_{\text{CMOS}} \, , \tag{7.16}$$

$$P_{\text{nano}} = P_{\text{sel}} + P_{\text{unsel}} + P_{\text{pars}} \, , \tag{7.17}$$

where $P_{\text{nano}}, P_{\text{CMOS}}, P_{\text{sel}}, P_{\text{unsel}}$, and P_{pars} are the nano domain, CMOS domain, selected cells, unselected cells, and parasitic elements (nanowires) power dissipations, respectively. It is assumed that P_{CMOS} for memristive and CRS arrays are comparable and

P_{pars} is negligible. The unselected cells power dissipation can be identified by READ and WRITE schemes and can be divided into two (or more) subclasses of half-selected or unselected cells. Here the target is to identify the memory pattern dependency on the total power dissipation assuming a high R_{LRS}.

The READ scheme that is discussed earlier, is used as the first READ scheme. Considering such a scheme and high R_{LRS} the total power dissipated by unselected cells (groups (1) and (2) in Figure 7.1 (a), through sneak currents) is negligible. Therefore, the worst case (reading "1") power consumption for $n \times m$ cells nano in the domain can be calculated through the following equation

$$P_{\text{nano,MEM}} = \frac{n V_{\text{pu,MEM}}^2}{R_{\text{LRS}}(1 + \sqrt{r})} \, , \tag{7.18}$$

while similar approach for an $n' \times m'$ CRS array results

$$P_{\text{nano,CRS}} = \frac{n' V_{\text{pu,CRS}}^2}{R_{\text{LRS}}(2 + \sqrt{2(1+r)})} \, , \tag{7.19}$$

where in this work $V_{\text{pu,MEM}} = 1$ V and $V_{\text{pu,CRS}} = 2.8$ V. To fill the gap between the power consumption in memristor and CRS arrays and having similar array size ($n \times m$), $n' = n/c$ and $m' = mc$, where c is a constant that is adjusted to achieve approximately similar power consumption for the two arrays. Here $c = 4$, so for example 1 K bits of data can be stored either in a 32×32 memristive array or 8×128 CRS array and have roughly similar power dissipation.

In the programming (WRITE) procedure, if $V_{\text{w,MEM}} = 2$ V and $V_{\text{w,CRS}} = 3.8$ V, there are $n + m - 2$ cells in the both arrays that are half-selected, groups (1) and (3) in Figure 7.1 (a), and $(n - 1)(m - 1)$ cells that are not selected, ideally 0 V voltage difference, group (2) in Figure 7.1 (a). The worst case condition is to have all of them at LRS for memristive array and LRS/HRS (logic "1") for CRS-based crossbar. Therefore, one potential problem with the WRITE scheme is to reset one or more half-selected cross-points. These cells are categorised under unselected cells for the power calculation. Here, there are 1 V and 1.9 V potential differences across the half-selected cells in memristor and CRS arrays, respectively, that is sufficiently low to avoid misprogramming. A power consumption analysis for this scheme shows that if $n > 16$ and $r > 3.5$, the total power dissipated in the CRS nano domain is much lower than the memristive array. The main reason is the all of the half-selected cells have an effective resistance equivalent to $(1 + r)R_{\text{LRS}}$ in a CRS array, whereas the same cells have R_{LRS}

in memristor array, which is significantly lower in size. For example, for $n = 100$ and $r = 4$ overall improvement in power dissipation is around 38% while for $r = 10$ results 70% reduction. This improvement rapidly increases if the number of half-selected cells increases. For instance, a WRITE scheme that activates all bit-lines (pull-up) and j^{th} word-line (grounded) and applying $V_{\text{w}}/2$ on the rest of the word lines, can write n bits each time and contains $n(m-1)$ half-selected cells.

This study indicates that if $R_{\text{LRS}} \ll 3\,\text{M}\Omega$, more than 65% and 50% of the total power (and consequently the total energy) is dissipated in half-selected cells during a WRITE operation for the 1-bit WRITE and multi-bit WRITE schemes, respectively. The contribution of half-selected cells is further increased if $R_{\text{LRS}} \geq 3\,\text{M}\Omega$. The total power consumption is also rapidly increased as the array size increases. The results also indicate that writing a word (multi-bit) is much more energy efficient than a bit, particularly for CRS-based array. Note that for the multi-bit WRITE scheme we applied a two-step WRITE operation (SET-before-RESET) introduced in Xu *et al.* (2011). The trade-off between using several WRITE schemes is still an open question.

Due to the fact that a high R_{LRS} would decrease the energy dissipation and the operation speed at the same time it is very important to note that the nonlinearity of the memristor characteristics plays an important role in identifying the maximum size constraint of a memristive array by identifying the effect of half-selected memory cells.

Xu *et al.* (2011) proposed a nonlinearity coefficient to analyse the nonlinearity effect using static resistance values of memristor biased at V_{w}/p and V_{w} as $K_{\text{c}}(p, V_{\text{w}}) = pR(V_{\text{w}}/p)/R(V_{\text{w}})$. This factor identifies the upper limit for n and m in a memristive array. If parameter α in $I \propto \sinh(\alpha V)$ represents memristor nonlinearity, the factor emphasizes that either higher α or higher p result in a larger $K_{\text{c}}(p, V_{\text{w}})$. Clearly, the later option is under the designer's control. In fact, this technique effectively creates an intermediate R_{LRS}, which is larger than its actual value. Note that the resistance does not necessarily increases if p increases. There is some examples that are not following similar characteristics, for instance $\sinh^{-1}(\cdot)$ behaviour in Inoue *et al.* (2005). In this case, larger resistances are achievable by decreasing p. So $K_{\text{c}}(p, V_{\text{w}})$ is used for bit- and word-lines. Considering the $V_{\text{w}}/2$ scheme, this approach is appropriate when $p = 2$, $K_{\text{c}}(2, V_{\text{w}})$. For $p > 2$, however, selected word-lines current cannot be calculated with $I(V_{\text{w}}/p)$ since the current that passes through an unselected cells on a selected word-line is a function of $V_{\text{w}}(1 - 1/p)$. Hence, calculating an upper limit for n is a function

of $K_r(p, V_w)$ that can be defined as,

$$K_r(p, V_w) = \frac{p}{p-1} \frac{R(V_w(1 - \frac{1}{p}))}{R(V_w)} \,, \tag{7.20}$$

therefore, a higher nonlinearity coefficient would not necessarily result larger upper limit for memristive array. Furthermore, controlling RESET parameters, such as filament formation process, electrode material, Joule heating process, and TiO$_2$ composition, play an important role here.

7.5   Conclusion and potential extensions

Simulation results indicate that due to sneak-paths, a memristive array is faced with misprogramming and misreading that aggressively limit the maximum nano-crossbar array size. However, the read margin in a CRS array is reliable with technology variations such as uncertainty in initial state programming, nanowire process variation, and the associated uncertainty on low resistance state programming. Therefore the presented work in this chapter provides a foundation and a generic analytical approach in the design of future CRS based circuits and systems.

The next chapter presents the first memristor-based and CRS-based content addressable memory implementations as one of the application of crossbar arrays using memristive devices.

Chapter 8

Associative Memory

CIRCUIT implementation based on memristive devices has attracted much of attention during the past few years. The aim in this chapter is to present the first memristor-based content addressable memory (MCAM) structure and also the first CRS-based CAM. The CRS-based CAM can implement binary and/or ternary CAMs, for use is as a part of a pattern matching system. The memristor-based designs are compared with the conventional implementations and their advantages are reported in this chapter.

[This page has been left blank intentionally.]

8.1   Introduction

Large-capacity Content Addressable Memory (CAM) is a key element in a wide variety of applications, e.g. pattern matching and recognition in particular. The inevitable complexities of scaling of MOS transistors introduce a major challenge in the realisation of such systems. Convergence of disparate and significantly different technologies that are compatible with CMOS processing may allow extension of Moore's Law for a few more years. This chapter provides a new approach towards the design and modelling of Memristor-based Content Addressable Memory (MCAM) using a combination of memristor and MOS devices to form the core of a memory (or compare logic) cell that forms the building block of CAM architecture. The non-volatile characteristic and the nanoscale geometry together with compatibility of the memristor with CMOS processing technology increases the packing density, providing new approaches toward power management through disabling CAM blocks without loss of stored data resulting in reduced power dissipation. This approach also has the scope for speed improvement as the technology matures.

In this chapter, Section 8.2 introduces a memristor-based content addressable memory with different configurations and their simulations and analysis. Section 8.3 also introduces a content addressable memory based on the complementary resistive switch.

8.2   Conventional CAM and MCAM structures

A content addressable memory illustrated in Figure 8.1 takes a search word and returns the matching memory location. Such an approach can be considered as a mapping of the large space of the input search word to that of the smaller space of output match location in a single clock cycle (Tyshchenko and Sheikholeslami 2008). There are numerous applications including Translation Lookaside Buffers (TLB), image coding (Kumaki *et al.* 2007), classifiers to forward Internet Protocol (IP) packets in network routers (Kim *et al.* 2009c), etc. Inclusion of memristors in the architecture ensures that data is retained if the power source is interrupted enabling new possibilities in system design in terms of power failure recovery.

Figure 8.1. Architecture for content addressable memories. Generic content addressable memory architecture for $n \times n$ NAND-type CAM cells. In this structure each data (D) and search (S) bits share one common bus line (D/S) to reduce the interconnection complexity. The architecture is based on the MCAM cell of Figure 8.4 (d) and the match-lines (MLs) composed of nMOS pass transistors.

8.2.1 Conventional content addressable memory

To better appreciate some of the benefits of our proposed structure, a brief overview of the conventional CAM cell using static random access memory (SRAM) is provided, as shown in Figure 8.2 (a). The two inverters that form the latch use four transistors including two p-type transistors that normally require more silicon area. Problems such as relatively high leakage current particularly for nanoscale CMOS technology (Verma and Chandrakasan 2008) and the need for inclusion of both V_{DD} and ground lines in each cell bring further challenges for CAM designers in order to increase the packing density and still maintain sensible power dissipation. Thus, to satisfy the combination of ultra dense designs, low-power (low-leakage), and high-performance, the SRAM cell is the focus of architectural design considerations.

For instance, one of the known problems of the conventional 6-T SRAM for ultra low-power applications is its static noise margin (SNM) (Verma and Chandrakasan 2008).

Fundamentally, the main technique used to design an ultra low-power memory is voltage scaling that brings CMOS operation down to the subthreshold regime. Verma and Chandrakasan (2008) demonstrated that at very low supply voltages the static noise margin for SRAM disappears due to process variation. To address the low SNM for subthreshold supply voltage Verma and Chandrakasan (2008) proposed 8-T SRAM cell shown in Figure 8.2 (b). This means, there is a need for a significant increase in silicon area to reduce possible failure when the supply voltage is scaled down.

Failure is a major issue in designing ultra dense (high capacity) memories. Therefore, a range of fault tolerance techniques are usually applied (Lu and Hsu 2006). As long as the defect or failure is within the SRAM structure, a traditional approach such as replication of memory cells can be implemented. Obviously it results in a large silicon overhead area, which exacerbates the issue of power consumption.

Some of the specific CAM cells, for example, ternary content addressable memory (TCAM) are normally used for the design of high-speed lookup-intensive applications in network routers, such as packet forwarding and classification two SRAM cells, are required. Thus, the dissipation brought about as the result of leakage becomes a major design challenge in TCAMs (Mohan and Sachdev 2009). It should be noted that the focus in this paper is to address the design of the store/compare core cell only, leaving out details of CAM's peripherals such as read/write drivers, encoder, Match-Line (ML) sensing selective precharge, pipelining, ML segmentation, current saving technique etc. (Pagiamtzis and Sheikholeslami 2006).

8.2.2   Generic memristor-nMOS circuit

Figure 8.3 shows the basic structure for a memristor-nMOS storage cell. For writing a logic "1", the memristor receives a positive bias to maintain an "ON" state. This corresponds to the memristor being programmed as a logic "1". To program a "0" a reverse bias is applied to the memristor, which makes the memristor resistance high. This corresponds to logic "0" being programmed.
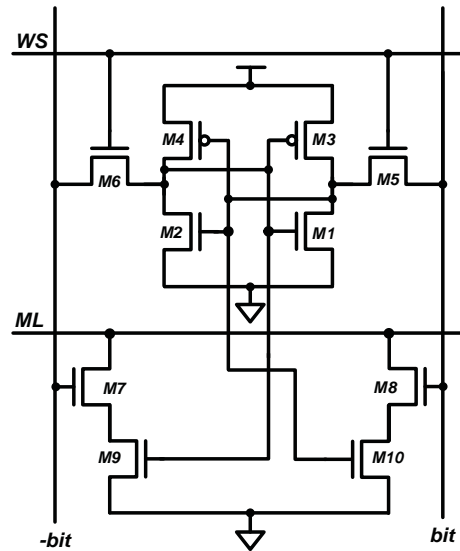
(a) Conventional 10-T NOR-type CAM Cell.
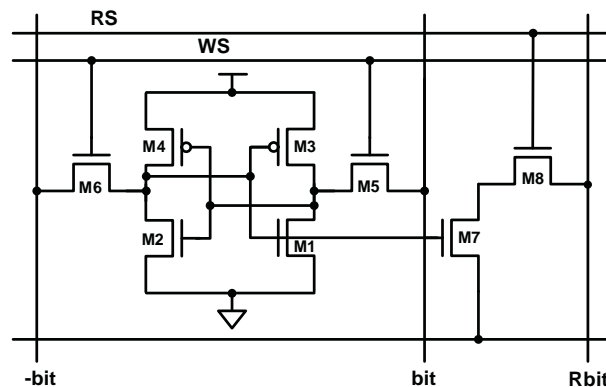
(b) Subthreshold 8-T SRAM Cell.

Figure 8.2. Conventional CAM cell structure and SRAM cell. Conventional CAM cell structure and the design of a SRAM cell for ultra low-power applications. In (a) a conventional 10-T NOR-type CAM circuit is demonstrated. Usually, conventional NOR- or NAND-type CAM cells have more than 9 transistors (Pagiamtzis and Sheikholeslami 2006). In (a) and (b), RS, Rbit, WS, ML, bit, and -bit lines are read select, read bit-line, word select, match-line, data, and complementary data signals.

(a) Structure of write mode.   (b) Basic cell.

(c) Program "Low" resistance "1".   (d) Program "High" resistance "0".
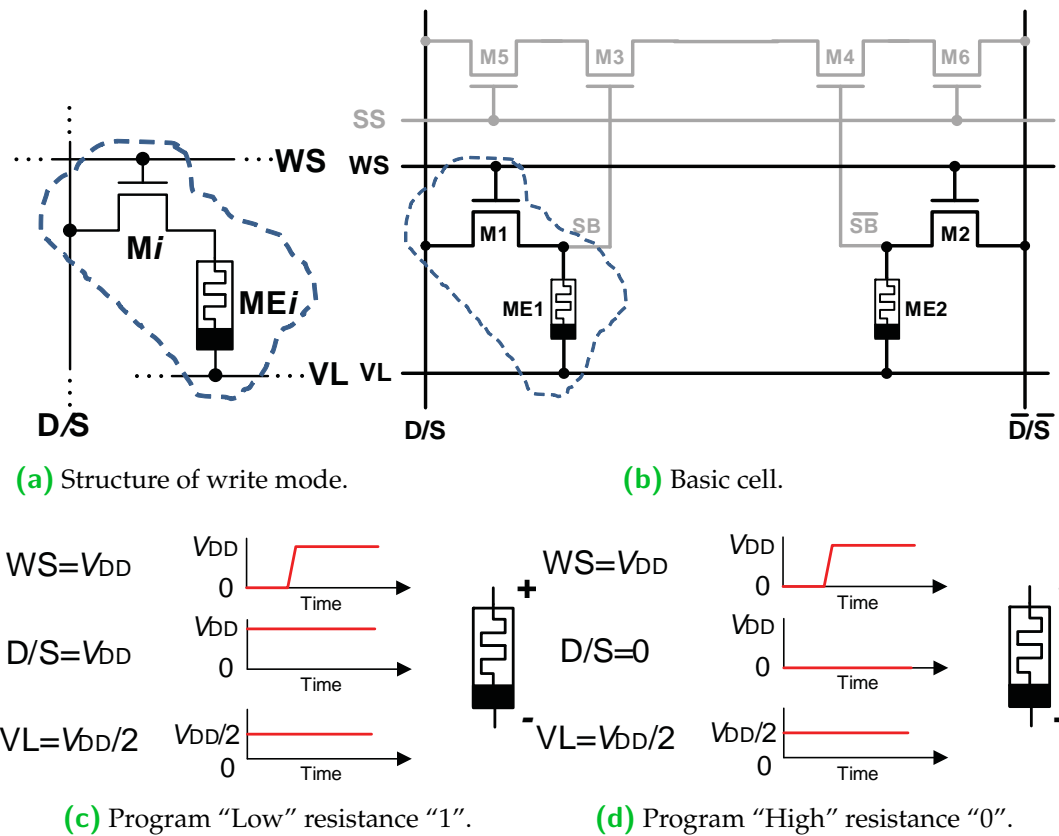
Figure 8.3. Memristor-nMOS cell and characteristics. Basic memristor-nMOS storage cell and the timing diagram. (a) shows write mode part of the i-th cell in a row. (b) Basic cell circuit without the match-line transistor. (c) "Low" resistance, R_{ON}, programming. Equivalent to logic "1". (d) "High" resistance, R_{OFF}, programming. Equivalent to logic "0".

8.2.3   MCAM Cell

In this subsection, variations of MCAM cells as well as a brief architectural perspective are introduced. The details of read/write operations and their timing issues are also discussed in the next section. A CAM cell serves two basic functions: "bit storage" and "bit comparison". There are a variety of approaches in the design of basic cell such as NOR based match-line, NAND based match-line, etc. This part of the thesis reviews the properties of conventional SRAM-based CAM and provides a possible approach for the design of content addressable memory based on the memristor.

MCAM cell properties

Figure 8.4 illustrates several variations of the MCAM core whereby bit-storage is implemented by memristors ME1 and ME2. Bit comparison is performed by either NOR or alternatively NAND based logic as part of the match-line ML_i circuitry. The matching operation is equivalent to logical XORing of the search bit (SB) and stored bit (D). The match-line (ML) transistors in the NOR-type cells can be considered as part of a pull-down path of a pre-charged NOR gate connected at the end of each individual ML_i row. The NAND-type CAM functions in a similar manner forming the pull-down of a pre-charged NAND gate. Although each of the selected cells in Figure 8.4 have their relative merits, the approach in Figure 8.4 (c), where Data bits and Search bits share a common bus is selected for detailed analysis. The structure of the 7-T NAND-type, shown in Figure 8.4 (d), and the NOR-type are identical except for the position of the ML transistor. In the NOR-type, ML makes a connection between shared ML and ground while in the NAND-type, the ML transistors act as a series of switches between the ML_i and ML_{i+1}.

8.2.4 Simulation results analysis and comparison

Generally, special algorithm is needed depending on the type of operation to be performed, namely "WRITE" and "READ" operations. In this section, the "WRITE" and "READ" operations of the basic MCAM cell for 7-T NOR-type are reported. In the following simulations $R_{LRS} = 100\ \Omega$ and $R_{HRS} = 100\ k\Omega$. Both the conventional CAM and MCAM circuits have been implemented using Dongbu HiTech 0.18 μm technology which needs 1.8 V nominal operating voltage for the CAM. The MCAM cell is implemented using nMOS devices and memristors without the need for V_{DD} voltage source. Using the above memristor parameters, satisfactory operation of the MCAM cell is achieved at 3.0 V. We have referred to this voltage as the nominal voltage for the MCAM cell. Furthermore, the initial state of the memristors ("ON", "OFF", or in between) is determined by initial resistance, R_{INIT}.

Write operation

At the write phase, the memristor ME1 is programmed based on the data bit on the D line. The complementary data is also stored in ME2. During the write operation,

(a) 5-T NOR-type.

(b) 6-T NOR-type.

(c) 7-T NOR-type.

(d) 7-T NAND-type.
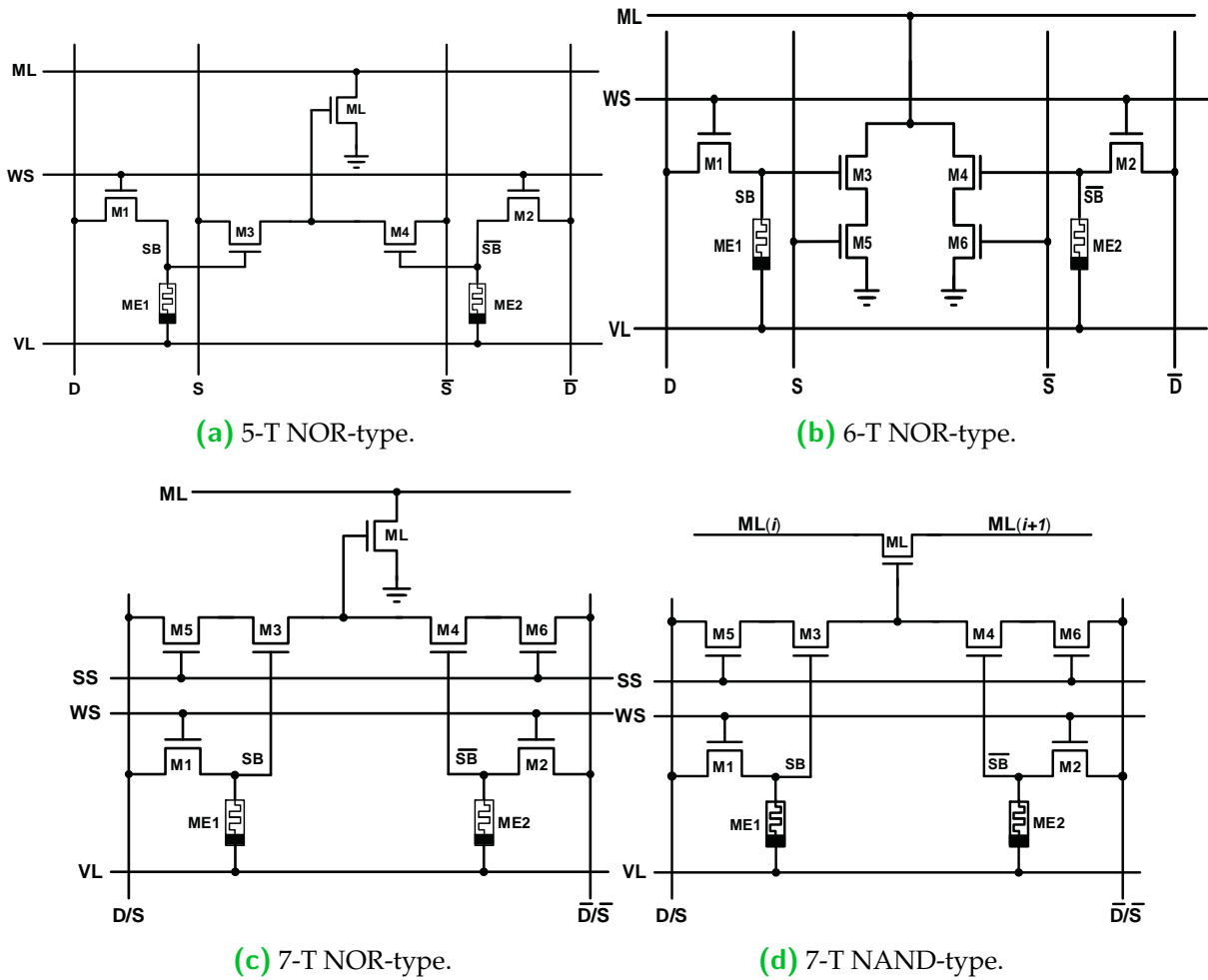
Figure 8.4. MCAM circuits. Cell configurations of possible MCAM structures.

the select line is zero and an appropriate write voltage is applied on VL. The magnitude of this voltage is half of supply voltage. The pulse width is determined by the time required for the memristor to change its state from logic "1" (R_{LRS}) to logic "0" (R_{HRS}) or vice versa. Waveforms in Figure 8.5 illustrate the write operation. In this case $R_{\mathrm{INIT}} = 40$ kΩ and the initial state is around $x = 0.6$, where $x = w/L$ from Chapter 3. The diagrams show two write operations, for both when D is "1" and when it is "0". By applying $V_{\mathrm{DD}}/2$ to VL line, there will be a $-V_{\mathrm{DD}}/2$ potential voltage across the memristor ME2 and $V_{\mathrm{DD}} - V_{\mathrm{th,M1}}$ across the memristor ME1.

The highlighted area in Figure 8.5 (b) shows the difference in the write operation between ME1 and ME2. When D $= 0$ and $\overline{\mathrm{D}} = V_{\mathrm{DD}}$, there is a threshold voltage (V_{th}) drop at the $\overline{\mathrm{SB}}$ node. Thus, the potential voltage across the memristor will be $V_{\mathrm{DD}}/2 - V_{\mathrm{th,M2}}$. At the same time, $-V_{\mathrm{DD}}/2$ is the voltage across the ME1, so the change in state in ME1 occurs faster than memristor ME2. The time for a state change is approximately 75 ns

for ME1 and 220 ns for ME2. Therefore, 145 ns delay is imposed because of the voltage drop across ME2. Figure 8.5 (b) present simulation results carried out using a behavioural SPICE macro-model.
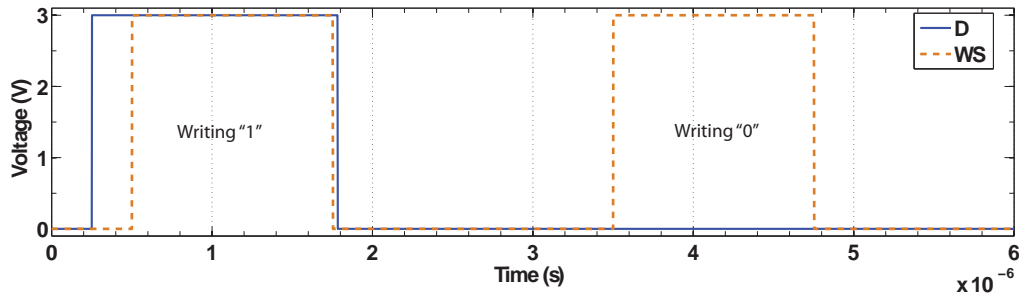
(a) Data (D) and Word Select (WS) signals. WS pulse width is 1.2 μs.
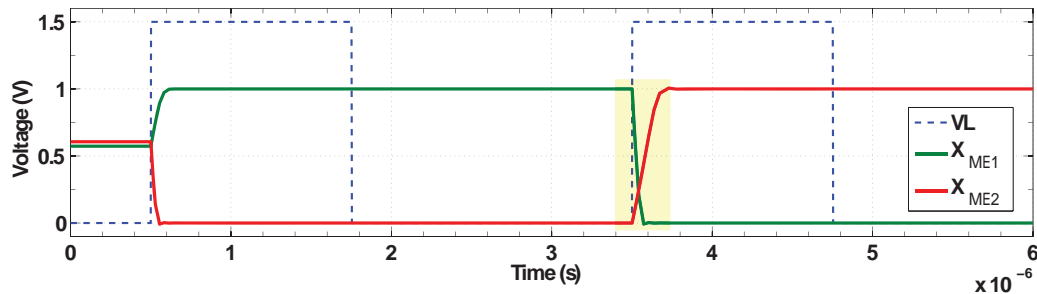
(b) Write enable, VL, and memristors state, x_{ME1} and x_{ME2}, signals.

Figure 8.5. MCAM write simulation. Write operation timing diagram. The highlighted area in (b) shows the minimum time for writing, which is the maximum for both memristors, around 220 ns. In (b) x_{ME1} and x_{ME2} are dimensionless parameters and both are varying between 0 and 1. The rational for showing VL and x_{ME1} and x_{ME2} together is that VL acts as a trigger for the state variables. $VL_{active} = 1.5$ V ($V_{DD}/2$) for write operation.

Read operation

Let us assume that ME1 and ME2 were programmed as a logic "1" and logic "0", respectively. Therefore, ME1 and ME2 are in the "ON" and "OFF" states and $R_{INIT,ME1} = 200$ Ω and $R_{INIT,ME2} = 99$ kΩ. In this case, the search line, S, is activated first. At the same time search select signal, SS, is activated to turn on the two select transistors, M5 and M6. The word select (WS) is disabled during the read operation. Figure 8.6 shows the waveforms for a complete read cycle. Read operation requires higher voltage for a short period of time. The VL pulse width (PW) for read operation is 12 ns as illustrated in Figure 8.6 (b) which is the "minimum" pulse width necessary to retain the memristor's state.

For matching "1" (when S=V_{DD}), the sequence of operations are as follows: (i) match-line, ML, is pre-charged, (ii) SS is activated, and (iii) VL is enabled as is shown in Figure 8.6 (a)-(c). A logic "1" is transferred to the bit-match node, which discharges the match-line, ML$_i$, through transistor ML. At this point x_{ME1} commences to decrease its state from 1 to 0.84, and x_{ME2} increases its state from 0 to 0.05. Thus, there is a match between stored data and search data. The following read operation for S="0" follows a similar pattern as shown in Figure 8.6 (c). The simulation results confirm the functionality of proposed MCAM circuitry.

(a)

(b)

(c)

(d)
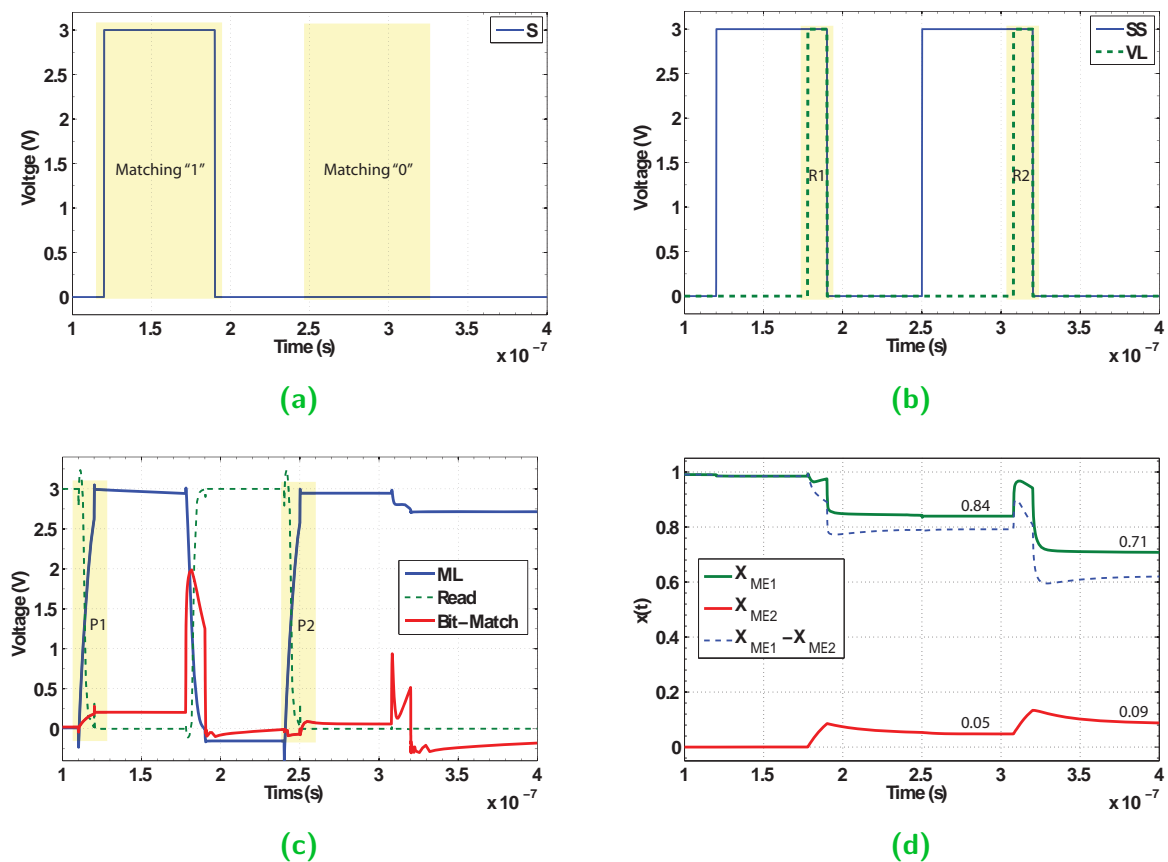
Figure 8.6. MCAM read simulation. Read operation timing diagram: (a) Search signal (S). For matching "1" S=V_{DD} and for matching "0" S=0, (b) Search select (SS) and read enable (VL) signals. VL$_{active}$ = 3.0 V (V_{DD}), (c) Bit-match, read, and match-line (ML) signals. Read=$\overline{ML}$, (d) ME1 and ME2 state variable signals. In (b) and (c), R1, R2, P1, and P2 represent two read and match-line pre-charge phases, respectively. The final (stable) values for x_{ME1} and x_{ME2} after two read operations are around 0.7 and 0.09. The difference between x_{ME1} and x_{ME2}, in terms of time is also shown in (d).

8.2.5 Simulation results analysis

Table 8.1 provides a comparison between the various MCAM cells that are proposed in Figure 8.4. It is worth noting that these simulations are based on a single cell. Therefore there are no differences in characteristics between 7-T NAND and 7-T NOR cells. The difference in minimum VL pulse width for read operation ($\text{VL}_{\text{min.PW,R}}$), between different MCAM cells, is relatively significant and is brought about as the result of pass-transistors in the path from search line to the bit-match node. One important issue in the design of MCAM cells is endurance. For instance, DRAM cells must be refreshed at least every 16 ms, which corresponds to at least 10^{10} write cycles in their life cycle (Lewis and Lee 2009). Analysing a WRITE operation followed by two serial read operations shows that 5-T, 6-T, and 7-T NOR/NAND cells deliver a promising result. After two serial read operations the memristor state values for x_{ME1} and x_{ME2} are, 0.74 and 0.06, and 0.71 and 0.09, for 5-T, 6-T, and 7-T NOR/NAND cell, respectively. The overall conclusion from the simulation results shows that in terms of speed, the 6-T NOR-type MCAM cell has improved in performance, but it uses separate Data and Search lines. The 7-T NOR/NAND cell shares the same line for Data and Search inputs. However, it is slightly slower $\text{VL}_{\text{min.PW,R}} = 12$ ns, while the voltage swing on the match-line is reduced by a threshold voltage (V_{th}) drop. In Table 8.1, PW,W and PW,R stand for Pulse Width for WRITE and READ operations, respectively.

Power analysis

A behavioural model was used to estimate the peak, average, and RMS power dissipation of an MCAM cell compared to the conventional SRAM-based cell showing in Figure 8.2. The power consumption is the sum of the static and dynamic power dissipations. A reduction of around 96% in average power consumption of the MCAM cell was archived. This is also practically feasible with a very low RESET switching current (10-100 nA) devices, as reported in Raghavan *et al.* (2011), and Ahn *et al.* (2008). The maximum power dissipation reduction is also better than 74% for the memristor-based structure. The Root Mean Square (RMS) value of current, which is sunk from the supply rail for the MCAM, is around 47 μA less than the conventional SRAM-based circuitry, which also shows more than 95% reduction in sink current.

Table 8.1. MCAM cells performance. Comparison between the proposed CAM cells in Figure 8.4.

Cell name	VL$_{\text{min.PW,W}}$ (ns) VL$_{\text{W}}=\frac{V_{\text{DD}}}{2}$	VL$_{\text{min.PW,R}}$ (ns) VL$_{\text{R}}=V_{\text{DD}}$	V$_{\text{drop}}$(bit-match) Voltage (V)	Data & Search Buses
6-T NOR, Figure 8.4 (b)	223	5	0	Separate
5-T NOR, Figure 8.4 (a)	219	9	V_{th}	Separate
7-T NOR/NAND, Figure 8.4 (c) or (d)	220	12	V_{th}	Shared

8.2.6 A 2×2 MCAM structure verification

Figure 8.7 presents an implementation of a 2×2 structure whereby the 7-T NAND-type (Figure 8.4 (d)) was used. As stated before, for the NOR-type, ML makes a connection between shared ML and ground while in the NAND-type, the ML transistors act as a series of switches between the ML_{out} and ground. The ML_1 and ML_2 match signals, illustrated in Figure 8.7 (a), are these ML_{out} signals. The cells are initially programmed to be "0" or "1" and the search bit vector is "10". The first row cells are programmed "10". As a consequence, ML_1 is discharged since there is a match between the stored and search bit vectors. Figure 8.7 (c) and (d) demonstrate the ML_1 and ML_2 outputs, respectively. Basically, using the ML transistors as an array of pass-transistors in a NAND-type structure imposes a significant delay, but using the proposed MCAM cells, the timing information shows a small delay of matching process is around 12 ns.

8.2.7 Physical layout

Layout of conventional 10-T NOR-type CAM and 7-T NOR-type MCAM cells are shown in Figure 8.8. The MCAM cell dimension are of $4.8 \times 4.36 \ \mu m^2$, while the dimensions for the conventional SRAM-based cell is $6.0 \times 6.5 \ \mu m^2$. Thus, the reduction in silicon area is in the order of 46%. The 2×2 structure also shows over a 46% area reduction. The two memristors, shown in highlighted regions of Figure 8.8 (b), were implemented between metal-3 and metal-4 layers as part of CMOS post processing.

8.3 CRS-based B/TCAM

This section presents a novel resistive-only Binary and Ternary Content Addressable Memory (B/TCAM) cell that consists of two Complementary Resistive Switches (CRSs), based on CRS model, presented in Section 5.6. The current section introduces two read-out method, namely logic→logic and logic→ON state transitions. The operation of such a CRS-based B/TCAM cell relies on a logic→ON state transition that enables this novel CRS application for future pattern matching and recognition systems. The nanometer scale, high scalability (along the third dimension), and relatively more robust functionality of the CRS cell compare to classic RRAM devices, pave the
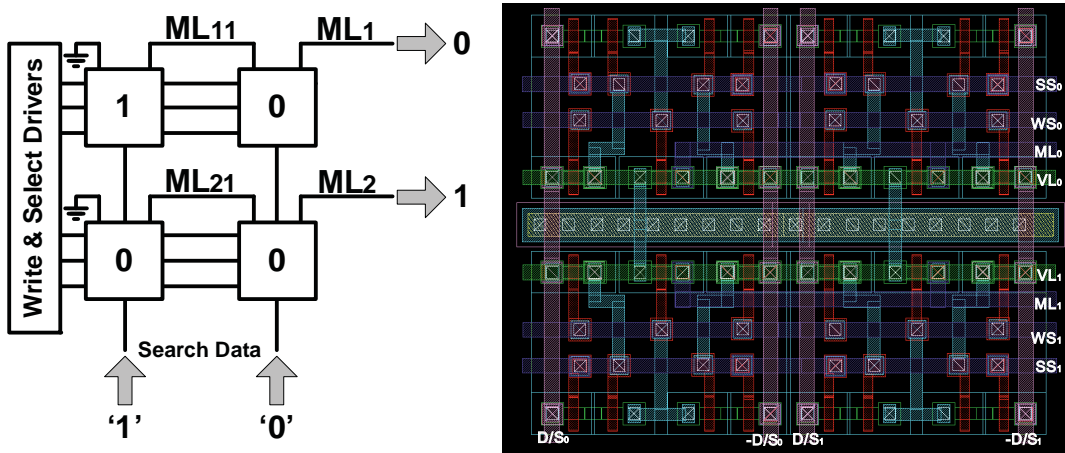
(a) 2×2 architecture, search data ("10"), and matching information.

(b) Layout implementation.
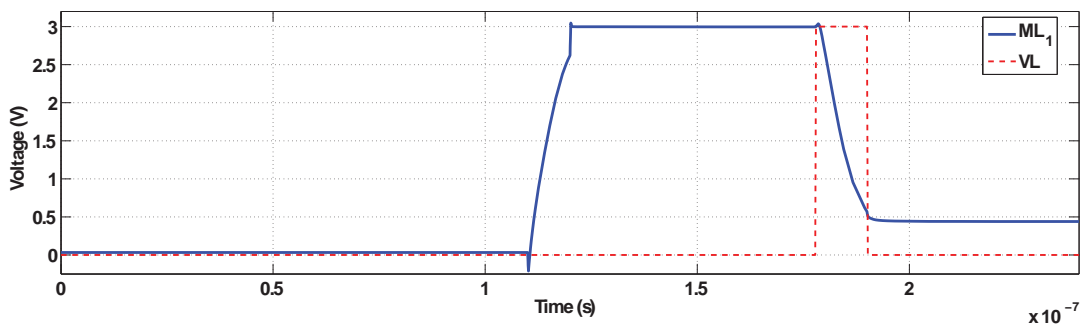
(c) ML_1 signal behaviour once VL triggers matching operation.
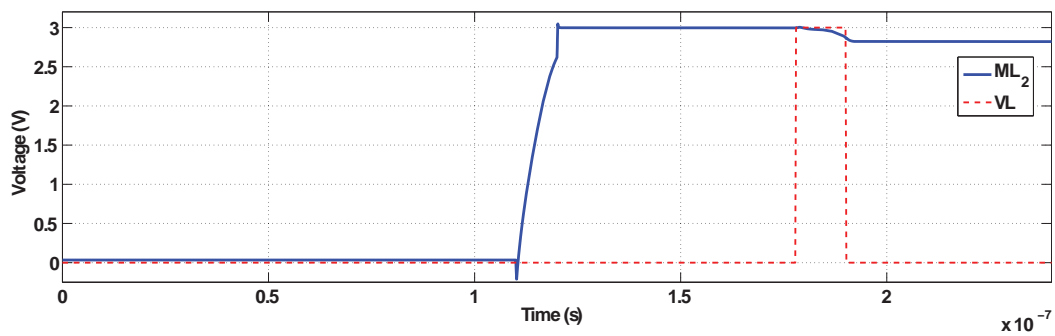
(d) ML_2 signal behaviour once VL triggers matching operation.

Figure 8.7. Small array of MCAM cells. A 2×2 MCAM structure: (a) 2×2 architecture and its layout implementation in (b) that shows over a 46% area reduction compare to a conventional implementation. (c) Illustrates ML_1 signal and (d) shows ML_2 signal. The search data ("10") is matched with the first row stored information so the $ML_1 = 0$ shows the search data is matched with row_1 and $ML_2 = 1$ shows the data is not matched with the stored information in the second row.
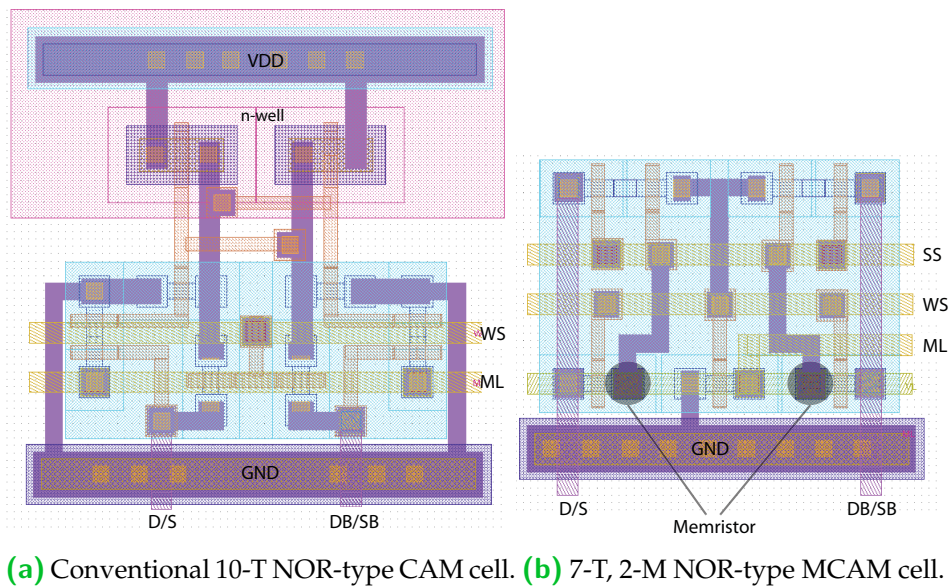
(a) Conventional 10-T NOR-type CAM cell. **(b)** 7-T, 2-M NOR-type MCAM cell.

Figure 8.8. Layout implementations of memristor-based and SRAM-based CAM cells. Layout implementation (a) conventional SRAM-based and (b) proposed MCAM cells. In (a) V_{DD} line is required. In (b), highlighted regions show the two memristors in the upper layer.

way for high-density RRAM structures. Due to the fact that the ON and OFF resistances of a device can be identified through material engineering, the leakage problem (voltage drop along an addressed line) can be significantly mitigated by increasing LRS resistance, R_{LRS} as was addressed analytically in Chapter 7. According to the analytical analysis in Chapter 7, implementing such array is practically feasible if memristor devices provide sufficiently large R_{LRS}. The content here is an application of 'material implication' logic which is explained in Section 8.3.2. The application of 'material implication' for Boolean logic implementation is discussed in Chapter 9.

8.3.1 Memristive arrays and scalability

Scalability (2D and 3D) of CRS-based crossbar memory array can be significantly increased by having a forming free device. Such devices quite popular for digital type RRAMs (Linn *et al.* 2010). A $R_{HRS}/R_{LRS} = 10^3$ results in 5000×5000 CRS array which is quite promising outlook for realising a Tera-bit memory (Kavehei *et al.* 2011a). A study by Strukov and Likharev (2007) shows that even if 3% of devices in a crossbar memory array are faulty a 2 Tbit·cm^{-2} density at 10 ns access time can be achieved. Defect tolerant mechanism is out of the scope of this research, but it can be addressed

using conventional codes, e.g. Error Correcting Code (ECC), Reed-Solomon, and Bose-Chaudhuri-Hocquenghem (BCH) codes (Roberts 2011). That analytical analysis also shows if 3% of the total devices are faulty, the density of crossbar memory, can be 6 times more than the density of ideal CMOS array, for $F_{\text{CMOS}}/F_{\text{nano}} = 3.3$ even when considering CMOS feature size, F_{CMOS}, as advance as 32 nm and access time of 10 ns. The study shows that the crossbar superiority will be significantly increased as $F_{\text{CMOS}}/F_{\text{nano}}$ increases. Therefore, introducing a memory cell using a crosspoint structure is an important contribution particularly when it uses a device which creates a new viewpoint for digital storage.

8.3.2   CRS read-out methods and material implication

Following the discussions in Section 5.6, CRS's structure is similar to a *memistor* (note the missing "r") (Widrow 1960, Thakoor *et al.* 1990, Xia *et al.* 2011a). A (digital) CRS uses a combination of a High Resistance State (HRS) and a Low Resistance State (LRS) to encode logic "0" and logic "1". Consequently, the overall resistance of such device is always around HRS, resulting in a significant reduction in the parasitic current paths through neighbouring devices. Figure 8.9 summaries the CRS states. If p and q indicate resistances of the memristors M1 and M2, respectively, four different states can be observed. For example, $p/q \leftarrow$ L/H indicates that LRS is written in p (memristor M1) and HRS in q (memristor M2). Two transitions are possible: logic→logic and logic→ON. The first transition indicates a change from L/H ("1") to H/L ("0") or vice versa, where L and H represent LRS and HRS states for memristors. Combinations L/H and H/L for p and q represent logic "1" and logic "0", respectively. Note that the H/H state only occurs once in a "fresh" device. According to Figure 5.11 (c) any transition between the states occurs if the applied voltage exceed, the SET thresholds, $V_{\text{th,S1}}$ or $V_{\text{th,S2}}$ and the device's initial state supports the transition. Possible state transitions are shown in Table 8.2, where p'/q' shows the next state, p/q illustrates the initial state, and output is a current pulse or spike. These outputs enable us to have two different read-out mechanisms, logic→ON or logic→logic. Considering the input-output relation, it is clear that CRS acts as a (Mealy) Finite State Machine (FSM) as has been experimentally demonstrated by Rosezin *et al.* (2011).

Conditional transitions between logical or non-logical states, as shown in Table 8.2 for the CRS, can be defined through *material implication* logic, IMP. It has been proven
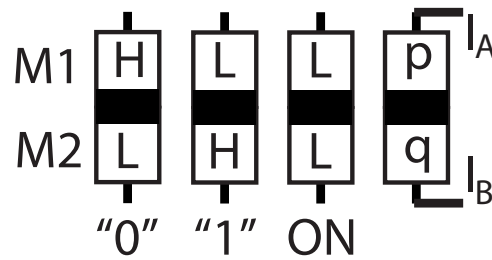
Figure 8.9. CRS device possible state configuration. CRS device structure and logical definition of each combination. A demonstration of all the operational states. Figure 5.11 (c) illustrates the crossbar view, and CRS functionality.

that the implication and FALSE operation are a complete set for logical operations (Borghetti *et al.* 2010, Rosezin *et al.* 2011). This logical operation results in a change of q depending on the state of p (or vise versa), known as p IMP q, 'p implies q' or 'if p then q'. Therefore, p NIMP q represent 'p not imply q', Table 8.2 (i), for example, represents $q \leftarrow$ H and we say the conditions (initial p/q and ΔV) not implies q. A full description of material implication logic is given in Borghetti *et al.* (2010), Bickerstaff and Swartzlander (2011), Kim *et al.* (2011c), Lehtonen *et al.* (2010), Xia *et al.* (2011a), and Kvatinsky *et al.* (2011), and from a new perspective for Ovonic devices in Ovshinsky (2011), however, this is the first application of NIMP operation that is shown here for a CRS device (Kavehei *et al.* 2011b, Kavehei *et al.* 2011c). There is some criticism around the CRS device operation which is mainly about the destructive read-out property and mimicking the behaviour of *Goto pairs*[18] (Rose and Manem 2010, Strukov and Likharev 2011). Although, the CRS structure might look like the Goto pairs, the middle electrode (shown in Figure 5.11 (a) with ME) must not be connected to any other crosspoint, which a big advantage for this device as having the middle electrode connected result in new parasitic current paths as it is the case with the structures proposed by Chen *et al.* (2011) and Shin *et al.* (2011b). Therefore, there is no meaningful difference between a memristive array and a complementary array in the available (CRS) form. For example, if a memristor array creates odd number (≥ 3) of elements in each sneak path, using the middle electrode results in an even number of elements (≥ 2) in each

---

[18]Goto pairs are known as a replacement for transistors (Kuekes *et al.* 2005). A two-terminal latching switch which is ran into several problems, e.g. retention time and switching speed. Relatively high switching speed in order to compete with the advanced MOS devices and relatively long retention in order to complete computing, e.g. ideally years or in some cases a few hours (Likharev and Strukov 2005).

Table 8.2. CRS states. State transitions in a CRS.

	p/q	$\Delta V = V_{I_A} - V_{I_B}$	p'/q'	Output
i)	"1"	$V_{\text{th,S1}} < \Delta V < V_{\text{th,R1}}$	ON	pulse
ii)	"1"	$V_{\text{th,R1}} < \Delta V$	"0"	spike
iii)	"0"	$V_{\text{th,R2}} < \Delta V < V_{\text{th,S2}}$	ON	pulse
iv)	"0"	$\Delta V < V_{\text{th,R2}}$	"1"	spike
v)	ON	$V_{\text{th,R1}} < \Delta V$	"0"	–
vi)	ON	$\Delta V < V_{\text{th,R2}}$	"1"	–

sneak path, hence reduced memory performance in terms of power consumption and functionality.

The transition from L/H ("1") to H/L ("0") or vice versa needs a high applied voltage ($> V_{\text{th,RESET}}$) that result in a current spike. While a logic→ON transition requires a voltage that lies between the SET and the RESET thresholds. These transitions conditionally occur depending on the device initial state and the polarity of applied voltage.

8.3.3 Proposed CRS-based CAM cell

The proposed structure functionality is similar to the other CAM cells. Here, however, it is compatible with the (four-dimensional) CMOL (CMOS MOLecular scale devices) architecture that is described in Strukov and Williams (2009b) and as its unique feature, it contains CRS devices that are stacked on top of the silicon substrate. Figure 8.10 summarises the idea. The grey and white modules in Figure 8.10 (a) represent the CMOS domain and the nano domain implementations, respectively. The red (rectangular) and blue (circle) dots correspond to via connections from the CMOS domain to the nano domain. The implementation is compatible with the CMOL architecture using a Field Programmable Gate Array (FPGA) type structure (Strukov and Williams 2009b, Strukov and Likharev 2007). The trade-off analysis between system performance and system partitioning using CMOS and the nano domain is beyond the scope of this research. Nonetheless, each cell represents a CAM cell that is entirely implemented in the nano domain. This is one of the differences between the proposed structure and other non-volatile CAM structures that basically rely on floating-gate transistors. Figure 8.10 (b) illustrates the CAM cell structure that works for binary CAM and a more flexible type, ternary CAM, applications. For simplicity, the dot

colours are chosen to be identical with the via colours in Strukov and Likharev (2007). It has to be stated that connecting the middle electrode (the black line in the CRS symbol) is not allowed because it, firstly, creates new sneak-path currents and, secondly, affects the expected functionality of the proposed CRS devices. Although the CAM functionality is observed, the readout mechanism is destructive.

Figure 8.10 (c) demonstrates the cell functionality. Possible combinations are shown in Figure 8.10 (c) (i) to (v). If the stored data (D) in the complementary cell (consisting of D and $\overline{D}$) is "1" and it is matched with the complementary select lines (SL and $\overline{SL}$) during the evaluation phase (active En), no path is between the pre-charged ML and SLs. Likewise, if D = SL ="0", ML remains charged (for D and SL vectors all the elements must be matched). The only possibility to discharge ML is the in situation that has been defined as logic$\rightarrow$ON implication. This situation can only happen either when D ="1" and SL ="0" or D ="0" and SL ="1". This path is shown with the dashed red arrows and the corresponding ON state device is also highlighted. Either of the combinations indicates a mismatched situation a voltage drop occurs on the corresponding ML. Details of the crossbar design and applied voltages are described in Kavehei *et al.* (2011a).

The proposed cell can handle TCAM operation, if a protocol for storing "don't care" (X) bits can be approved. The total CAM capacity can be calculated through

$$MC_{CAM} = (m \times n) \cdot h/2 \,, \tag{8.1}$$

where m and n identify the array size, h indicates the number of layers and the appearance of 2 is due to the fact that we need complementary cells. Apart from the very high density capability of the proposed CAM cell, A 64×8 CAM is simulated and its function is confirmed. In this implementation 16 select lines and 64 match-lines are required. Figure 8.11 illustrates simulation inputs and results. The stored memory pattern and the search stream are randomly generated and shown in Figure 8.11 (a) and (b). For simplicity, in the presentation, we intentionally addressed only one (the 1st) match-line, therefore, the expectation is to see ML_1 remains unchanged while all other match-lines are dropped. The voltage drop must be detectable by the sense amplifier (SA) chain (Kavehei *et al.* 2011a). Nano-wire parasitic resistors are also taken into account as reported in Chapter 7.
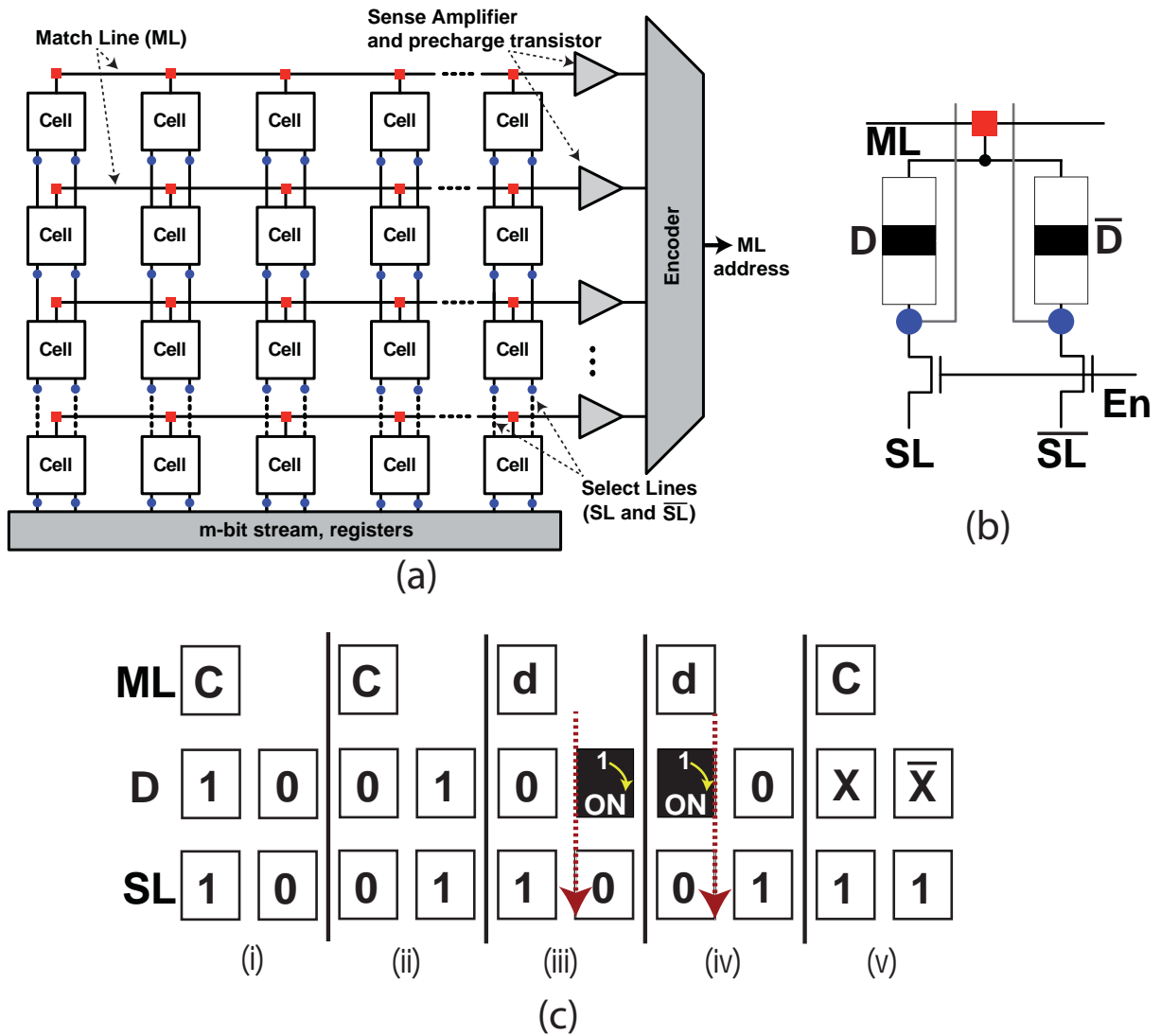
Figure 8.10. CRS-based B/TCAM. The CAM system, (a), and proposed cell (b). Design is compatible with CMOL architecture. The blue and red via contacts between the CMOL type array and CRS-based array highlights this compatibility. The logical operation of the B/TCAM cell is shown in (c). ML $=$C and d demonstrate charged and discharged ML, respectively.

Figures 8.11 (c) and (e) illustrate matched (solid line) and mismatched (dashed lines) MLs and the evaluation signals, En (dashed line with circle symbols). The only match-line that remains unchanged after activating the enable is the red one. The voltage drop right after activating En occurs due to the fact that each ML acts as the middle node of a voltage divider with an effective pull-up and pull-down resistors. Therefore, another advantage of CRS-based CAM is that the pull-down resistors are initially R_{HRS}, whereas a memristor-based array is highly pattern dependent. One issue with the design of a CRS-based CAM is the reverse leakage. In this case, leaked currents through matched MLs and mismatched MLs pull-up the voltage on mismatched MLs. This problem can be addressed using a feedback mechanism from MLs to SLs.

Figure 8.11 (d) demonstrates resistances of two CRS devices, with stored logic "0" or "1" (dashed line) and ON states (solid line). In the mismatched cells a logic$\rightarrow$ON transition is observed. The ON resistance of a CRS device is equivalent to $2R_{LRS}$. The outputs then feed into an array of SAs through the red via connections. The design of these Sense Amplifiers (SAs) requires a detail analysis of the array output for finding optimum values for crossbar memory parameters (Kavehei *et al.* 2011a).

Increasing access time and decreasing energy dissipation of B/TCAMs are two trends that have been aggressively pursued. Although, comparing today's mature or advanced technologies with the emerging technologies is not quite fair, a switching speed and energy analysis of fabricated devices in Kavehei *et al.* (2011a), and Borghetti *et al.* (2010) illustrates that applying higher voltage pulses exponentially increases the switching speed and it reduces overall energy dissipation. It is also observed that more than 80% of the total power is consumed by the nanowires, while the device itself consumes 10-100 pJ dynamic energy (30 ns switching time) (Borghetti *et al.* 2010), which is not an outstanding result compared to low-power B/TCAMs. Resistive memories and in particular, CRS devices, present a relatively robust operation, non-volatile memory, high scalability, and small switching time, while maintaining a relatively low switching energy, which make such device a serious alternative to the conventional CMOS technology (Linn *et al.* 2010, Kavehei *et al.* 2011a, Rosezin *et al.* 2011). In addition, as the CRS technology matures and the advanced transistor technologies continue to face more challenges, the combination of these two technologies will result in significantly more efficient and denser designs (Strukov and Likharev 2007).
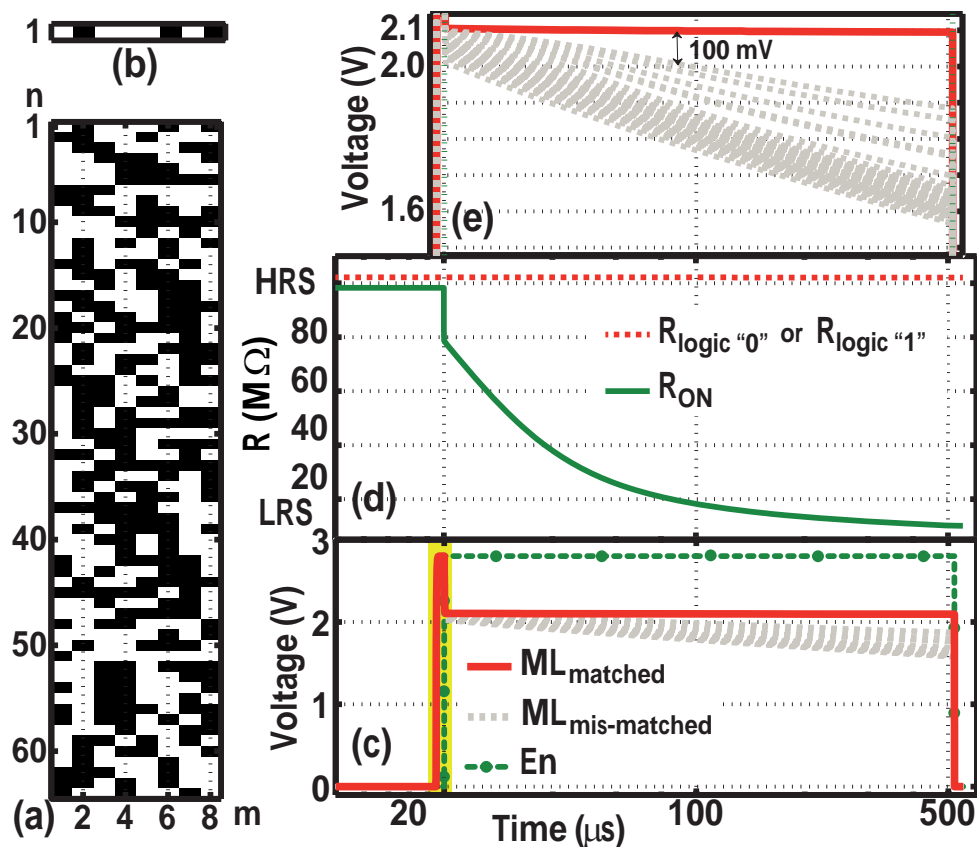
Figure 8.11. Simulation of a 64×8 **CRS-based B/TCAM .** CRS-based CAM simulation results (using Cadence Spectre). The stored and input patterns are shown in (a) and (b), respectively. (c) demonstrates matched and mismatched MLs and the evaluation, En, signal. The yellow region highlights a pre-charge step. (e) demonstrates a more clear picture of (c). Approximately, 80 μs for the worst-case ML to reaches the minimum detectable ΔV. (d) Illustrates two resistor samples (logic -either "0" or "1"- and ON states).

8.4   Conclusions and future work

The idea of a circuit element, which relates the charge q and the magnetic flux Φ realisable only at the nanoscale with the ability to remember the past history of charge flow, creates interesting approaches in future CAM-based architectures as we approach the domain of multi-technology hyperintegration where optimization of disparate technologies becomes the new challenge. The scaling of CMOS technology is challenging below 10 nm and thus nanoscale features of the memristor can be significantly exploited. The memristor is thus a strong candidate for tera-bit memory/compare logic.

The non-volatile characteristic and nanoscale geometry of the memristor together with its compatibility with CMOS process technology increases the memory cell packing density, reduces power dissipation and provides for new approaches towards power reduction and management through disabling blocks of MCAM cells without loss of stored data. The simulation results show that the MCAM approach provides a 45% reduction in silicon area when compared with the SRAM equivalent cell. The Read operation of the MCAM ranges between 5 ns to 12 ns, for various implementations, and is comparable with current SRAM and DRAM approaches.

Simulation results indicate a reduction of some 96% in average power dissipation with the MCAM cell. The maximum power reduction is over 74% for the memristor-based structure. The RMS value of current sunk from the supply rail for the MCAM is also approximately 47 μA, which correspond to over a 95% reduction when compared to SRAM-based circuitry. To the best of our knowledge this is the first power consumption analysis of a memristor-based structure that has been presented using a behavioural modelling approach. As the technology is better understood and matures further improvements in performance can be expected.

Besides memory applications, memristors have shown a promising outlook for analogue and digital computing. This topic is discussed in the next chapter where this application is explored in forms of 'analogue memristor' and 'digital memristor' as well as limitations of the fabricated memristor device in addressing a reliable analogue computing. The next chapter also discusses application of memristive devices in neuromorphic computing and its extension to a basic simulation of learning process in memristor networks.

Chapter 9

Computing with Memristive Devices

THE classical von Neumann machine suffers from a large sequential (fetch-execute-store cycle) processing overload due to the existence of the data bus between memory and logic. Neuromorphic engineering introduces a more efficient (event driven) implementation but not necessarily low-power. Software techniques are power hungry and traditionally there is no low-power hardware device (switch) to provide tighter coupling between memory and logic. The memristor is an emerging technology that combines non-volatile memory and in-situ computational characteristics in one device promising an entirely new computer architecture.

[This page has been left blank intentionally.]

9.1 Introduction

This chapter presents new computational building blocks based on memristive devices. These blocks, can be used to implement either supervised or unsupervised learning modules. This is achieved using a crosspoint architecture, which is an efficient array implementation for nanoscale two-terminal memristive devices. Based on these blocks and an experimentally verified SPICE macromodel for the memristor, it is demonstrated that firstly, a Spike-Timing-Dependent Plasticity (STDP)-like circuits can be implemented by a single memristor device and secondly, a memristor-based competitive Hebbian learning through STDP using a 1×1000 synaptic network. This is achieved by adjusting the memristor's conductance values (weights) as a function of the timing difference between presynaptic and postsynaptic spikes. These implementations have a number of shortcomings due to the memristor's characteristics such as memory decay, highly nonlinear switching behaviour as a function of applied voltage/current, and functional uniformity. These shortcomings of the analogue approach can be addressed by utilising a digital approach that can be used for biomimetic computation approach. The digital implementations in this chapter use in-situ computational capability of the memristor that is used in a similar way to CAM cells implementation in Chapter 8.

In this chapter, Section 9.2 describes in-situ computing capability of the memristive devices. This section proposes a novel way of carrying out logical operations using CRS devices and simulation results. The method that is applied to a simple structure in order to express its flexibility in implementing different logic gates. Section 9.3 presents a memristor-based building block for analogue computing, which is a multiply-accumulation circuit (MAC), and its simulation results. This section also presents experimental results to highlights multiple stable state programming, sharp switching characteristics, memristor-based STDP (mSTDP) implementation, and learning capability of a memristor network using 1000 pre-synaptic neurons and 1 post-synaptic neuron.

9.2 Digital in-situ computing

9.2.1 CRS-based logical operations

Here, CRS-based logical operation and a logic→ON transition dependent PLA (programmable logic array), which is explained in Chapter 8, are introduced. The presented approach relies on crossbar memory array structure discussed in Chapter 7. This is achieved by charging the bit-line in a crossbar, then applying inputs to its word lines. The inherent implication property of the device causes a change under certain conditions that has been already discussed in Subsection 8.3.2. Rosezin *et al.* (2011) proposed AND and NOR operations using the logic→logic transition and current spike read-out process. This method is very dependent on the current spike as a result of the transient ON state between two logic states. In their implementation, two combinations have been evaluated out of two possible combinations for two CRS devices. Assume voltage, ΔV, is applied across a CRS device that is exceeded its RESET threshold, in this situation this device changes its stored logic, D, if D is a certain logic depends on the signature of ΔV. Furthermore, if two CRS devices are connected together, that intermediate point can be connected to either ground or power supply to generate NOR/AND gate. That is the reason that no more possible state can be assumed using such approach.

Here two comprehensive forms of building logical gates are introduced. The first form, allows storing one or more inputs as device state and the second method does not. Figure 9.1 illustrates how CRS works as an implementation of a not implication, NIMP, operation and how NAND and OR operations can be implemented using a single CRS device. A better description of NIMP operation can be found in Section 8.3.2. Figure 9.1 (a)-(d) are well explained in the figure's caption and their operations are also described. Figure 9.1 (e) and (f) follow similar phenomenon but in a form of a PLA. The proposed approach relies having a logic→ON transition in the OR-plane whenever an output product term is addressed. From the NIMP operation, it is clear that if the applied inputs are part of the output product terms, that bit-line does not discharge so there will be enough voltage across the output CRS device with stored logic "1" (green) to turn to ON and conduct significantly more current to charge the output load.

Here we applied $V_{\mathrm{pu}} = 2.8$ V and $V_{\mathrm{pd}} = 0$ V, so we used 0.25 μm CMOS transistors in our CMOS domain. Therefore, equivalent input voltage for logics "1" is 2.8 V and for
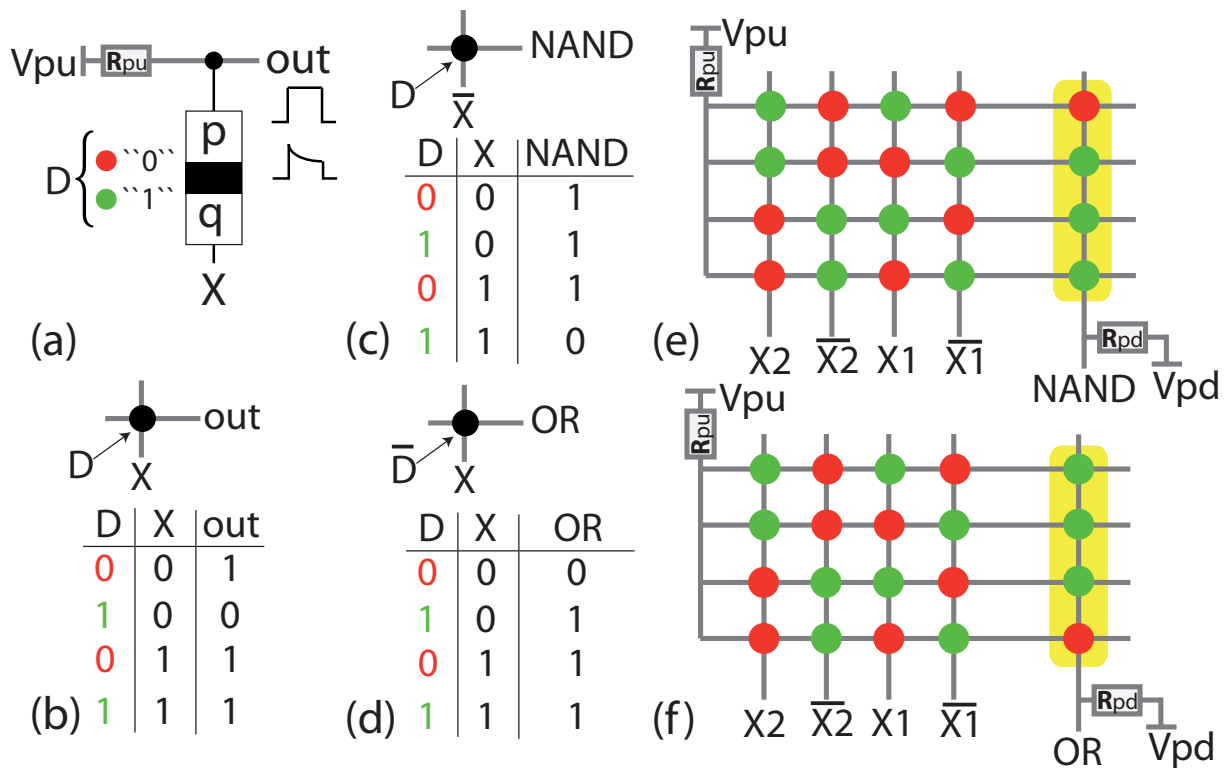
Figure 9.1. CRS-based logic gates and PLA structures. CRS-based logic gate structures. (a) D represents stored data, X is an input, and R_{pu} is pull-up resistor. The output is initially charged and it is discharged depends on D and X. (b) Shows how a "not implication", NIMP, can be implemented. Here $q' \leftarrow D$ NIMP X. (c) Two inputs NAND gate is implemented by storing one input as device state and another one as an actual input. Here, complementary signal of X is applied to the device. (d) Similar to NAND but complementary of D stored in the CRS and X is applied as an input. Therefore, an OR operation is implemented, simply by a single CRS device. It is clear that the presented operations are sequential and they requires one (or several) initialisation, which is an inherent limitation of Boolean logic operations reported in Rosezin *et al.* (2011), and Borghetti *et al.* (2010). Pull-up (charge) voltage is enough to push a device to its ON state and not writing a logic, $V_{\text{th,S}} < V_{\text{pu}} < V_{\text{th,R}}$. NOT function can also be implemented using a single CRS if D stores (the data) A and $X = 0$, $F = \overline{A}$. (e) and (d) are PLA implementations of the two logic gates. Here, the complementary output signals, AND and NOR are removed. The yellow colour highlights the OR-plane and the rest of the crossbar represents the AND-plane.

logics "0" is 0 V. Both, the pull-up and pull-down resistors, R_{pu} and R_{pd}, are both equal to $R_{\mathrm{LRS}}\sqrt{2(r+1)}$, where $r = R_{\mathrm{HRS}}/R_{LRS}$ (Kavehei *et al.* 2011a). The used peripheral CMOS circuitries can be found in Qureshi *et al.* (2011), and it is briefly highlighted in Fig. 9.2. The sense amplifier was designed for voltage sensitivity of more than 100 mV.

NOTE:
This figure is included on page 170 of the print copy of
the thesis held in the University of Adelaide Library.

Figure 9.2. Peripheral CMOS circuitries for multiplexing. CMOS switches and multiplexers to control and apply READ and WRITE modes. Adapted from Qureshi *et al.* (2011).

Assuming we have two inputs, X_1 and X_2, and two CRS devices, D_1 and D_2, connected to these inputs and a charged bit-line. A number of functions can be implemented by writing $\overline{F} = D_1 \cdot \overline{X_1} + D_2 \cdot \overline{X_2}$, hence, $F = \overline{D_1} \cdot \overline{D_2} + \overline{D_1} \cdot X_2 + \overline{D_2} \cdot X_1 + X_1 \cdot X_2$. The first term, $\overline{D_1} \cdot \overline{D_2}$, indicates that if both CRSs store "0" TRUE ($F = 1$) is implemented. Some other functions that are implemented using this configuration are shown in Table 9.1. In Section 8.3.3, a demonstration of a CRS-based content addressable memory based on the XOR/XNOR function was shown, which is basically an XNOR (XOR) implementation in Table 9.1. Figure 9.3 (a) illustrates simulation of a two input NAND function.

Table 9.1. CRS-based logic gates. CRS-based logic implementation with two inputs and two CRS devices, $F = \overline{D_1} \cdot \overline{D_2} + \overline{D_1} \cdot X_2 + \overline{D_2} \cdot X_1 + X_1 \cdot X_2$.

D_1	D_2	X_1	X_2	Function
$\overline{A}$	A	0	B	$A \cdot B$ (AND)
A	$\overline{A}$	0	$\overline{B}$	$\overline{A + B}$ (NOR)
A	$\overline{A}$	$\overline{B}$	B	$A \oplus B$ (XOR)
$\overline{A}$	A	$\overline{B}$	B	$A \odot B$ (XNOR)

The most significant advantage of this method is that the initialisation step (step 1) is that the data is written into CRS arrays and not represented by a simple refresh cycle, as it is shown in Figure 9.3 (b).

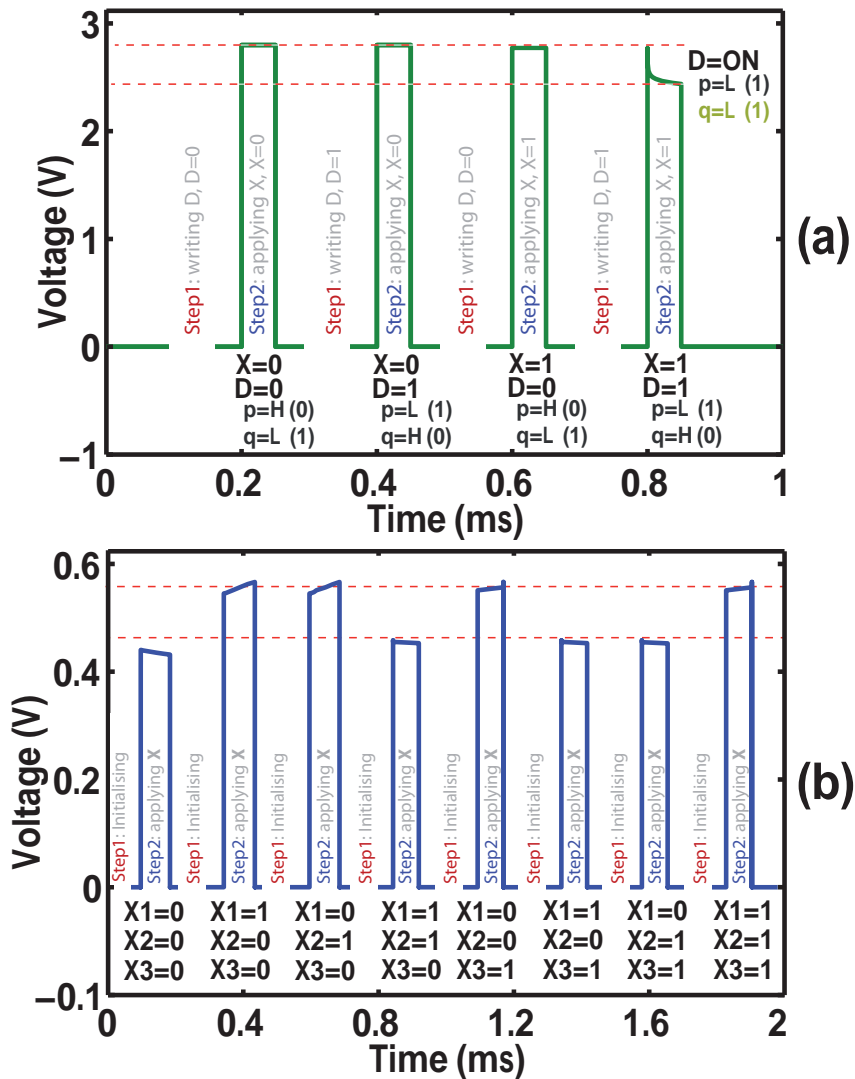## 9.3 Analogue memory and computing

9.3.1 Memristor device characteristics for analogue computing

According to Eq. (5.1) in Chapter 5, memristor device characteristics can be defined using a system of two equations,

$$\begin{cases} I = g(w, V) \cdot V \\ \frac{\mathrm{d}w}{\mathrm{d}t} = f(w, V) \,, \end{cases} \tag{9.1}$$

where w is a physical variable indicating the internal memristor state that in theory can have a value between 0 and L ($0 < w < L$), where L is the thickness of a thin-film metal-oxide (memristive) material sandwiched between two metallic electrodes, and I and V represent current and voltage, respectively. The $g(\cdot)$ function represents the memristor's conductance. The state variable can be expressed using a normalised form $x = 1 - w/L$. In this case, $w \to 0$ or moving towards higher conductances can be expressed as $x \to 1$ and $w \to L$ or moving towards lower conductances can be shown as $x \to 0$. Eq. (9.1) shows that the output of the system (here I), at a given time, depends on w and V. State transition conditions are also explained by the function $f(\cdot)$. To measure this function, several time-domain experiments for I and V are required. According to our measurements, a $\sinh(\cdot)$ like behaviour plus an additional term can be used to explain the dynamics of the device.

Figure 9.3. Two sample gate simulations for CRS-based logic. CRS-based logic gate simulations. (a) A 2-input NAND gate (Figure 9.1 (c)) simulation. In this style, we are allowed to store one input as the CRS state. (b) A 3-input XOR (SUM) function, implemented in a PLA structure. In both cases, (a) and (b), dashed red line show worst-case low and high output voltages that are sent to the sense amplifiers. Due to limited space, complementary output signals of the XNOR are not shown. Initialisation in (b) means, the array should be initialised before the next logical operation and this is the main reason that the first approach (in (a)) is by far more efficient implementation in terms of both hardware and number of steps. No initialisation is required in (a), because 'writing D' effectively means writing one of the inputs into the device.

The sinh($\cdot$) term defines the dependency of velocity, dw/dt, to the effective applied electric field that has been described as an ionic crystal behaviour in an external electric field (Mott and Gurney 1964), as discussed in Section 5.6. The additional term highlights the dependency of conductance, G_t, on previous conductance, G_{t-1}. Intuitively, an exponential form function $h(w)$ is used to define dw/dt as a function of w based on Figure 3 in Pickett *et al.* (2009). The $h(w)$ function then should be multiplied by the sinh($\cdot$). The conductance behaviour as a function of w is also shown in Figure 2 of Kavehei *et al.* (2011d). Due to the asymmetric behaviour of $w \to 0$ and $w \to L$ (Pickett *et al.* 2009), we have used two different $h(w)$ definition to have a more accurate switching properties (Pickett *et al.* 2009, Kavehei *et al.* 2011d).

The state variable equation then can be defined as

$$\frac{dw}{dt} = h(w)f(V) + d(w) \ . \tag{9.2}$$

This demonstration is similar to Eq. (5.13) and helps to easily extract the linear approximation of the memristor model presented in Strukov *et al.* (2008). The function $d(w)$ represents the decay term which can be weeks, months, or more. The decay term appears to be very similar to synaptic weight update (learning) rule (Snider 2011, Snider 2008b, Snider 2008a, Strukov 2011). The first term of Eq. (9.2), represents a voltage dependent, highly nonlinear characteristics that makes high-speed digital computing possible (Rosezin *et al.* 2011). This property originated from the fact that resistance modulation inside the metal-oxide occurs via electron-ion interactions. This term creates a significant problem for learning applications in the current form and also limits new opportunities for the future of biomimetic circuits and systems as these two recent studies on the short-term and long-term memory transitions in a nanodevices (Ohno *et al.* 2011, Chang *et al.* 2011).

This problem can be addressed by taking advantage of the high nonlinearity of the memristor devices. As the nonlinear behaviour in the device produces a threshold-like region that voltages below that threshold do not change the conductance. Considering the fact that, memristor's conductance, G, can be tuned by a series of pulses in voltage form with appropriate pulse widths and a voltage around the threshold, obviously. Applying a voltage around the threshold slightly changes x (or w) if it is maintained for a few μs. It is observed that such voltage cannot change the device state if the duration is around a few tens of nanoseconds. However, a slight increase in the applied voltage increases the switching speed by several orders of magnitude, which makes

nanosecond (digital) switching possible. Therefore, a series of few μs pulses with an appropriate pulse shape can be used to implement Hebbian learning rule (Zamarreño-Ramos *et al.* 2011).

9.3.2 Muti-stable state memory

Here we demonstrate such behaviour in $Ag/TiO_2/ITO$ experiment, which is an identification for existence of an ionic drift. Figure 9.4 illustrates the existence of the multi-stable memory levels. The experiments carried out using a Keithley 4200-SCS. Triangular input voltage was swept from 0 V to -0.9 V and vice versa. Current compliance of 500 μA was applied to avoid any damage to the device. At the end of each cycle device was disconnected from inputs.

The most critical limitation of analogue memristor is its state decay. The problem is once the analogue state is vanished, it is extremely hard, if not possible, to refresh it to its previous state. Although many stable state can be observed, our measurements for five conductance levels showed decay distribution ranging from a few hours up to a few days. More measurements were not possible with our limited time.
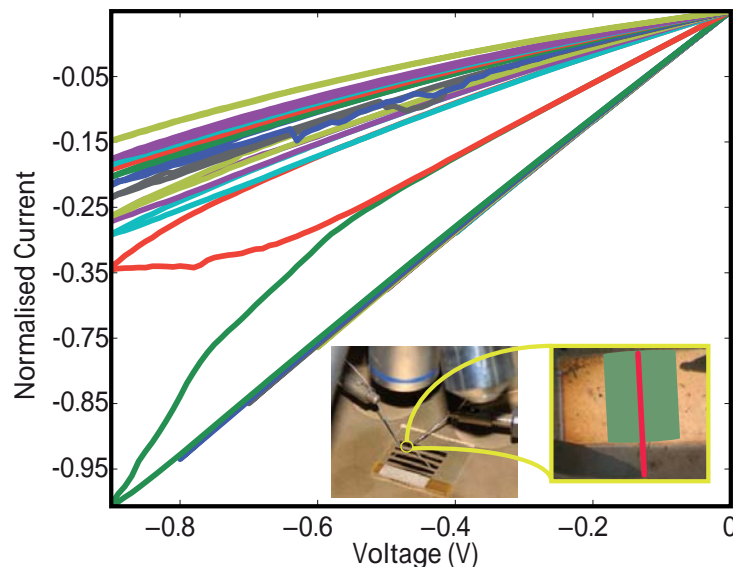

Figure 9.4. Multi-stable state memory existence in the memristor device. Memristor analogue behaviour. Experimental result from $Ag/TiO_2/ITO$ memristor. Current values are normalised to their maximum value (35 μA). Inset shows a device under test (DUT). The red and the green areas highlight a memristor device.

9.3.3   Existence of a threshold-like switching

The existence of a switching threshold in a TiO_2-based memristor is demonstrated. According to Chua's definition (Chua 1971), memristor links electrical charge to flux, φ, and $\varphi = \int V dt$. Therefore, the amount of flux passing through the device can be controlled by V and/or time. So, low pulse widths should not change the conductance if the voltage is lower than a certain value and small voltages similarly do not change the conductance if the applied pulse width is not sufficient. The analysis started from the amorphous (RESET) state and a crystallisation window created above 0.8 V and 100 μs. Figure 9.5 illustrates the results from a Pt/TiO_2/Pt memristor. It is observed that the area of crystallisation window decreases as R_{HRS} increases in different devices (Kavehei *et al.* 2011d).
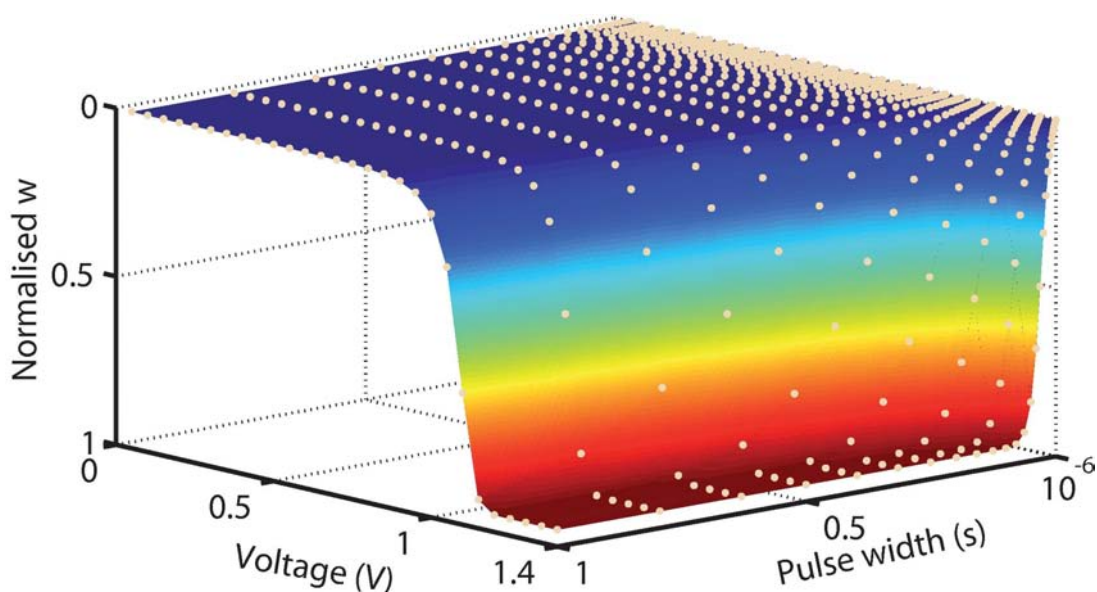
Figure 9.5. Sharp switching behaviour of the memristor. Existance of a switching threshold in the memristor material. The pulse widths are from 10 μs to 1 s.

9.3.4   Memristive, plasticity, and learning

The connection can be drawn between memristive devices and biological synaptic update rule, known as STDP, that has been observed in the brain Jo *et al.* (2010). This can be achieved by collecting data from a memristive device based on the time difference, Δt, between two signals, so called pre- and post-synaptic signals. The results are shown in Figure 9.6 (a), which shows how the device under test (DUT) weight (resistance) changes as a function of Δt. The intermediate states vanish after a certain decay

duration whereas a significantly higher potentiation ($x \rightarrow 1$) will be kept as a long term memory. So, the existence of intermediate states decay helps in mimicking the long-term potentiation and short-term plasticity (LTP and LTP) behaviour (Ohno *et al.* 2011).

The collected information is then used as stimuli for a network of 1×1000 memristors are connected to one neuron being implemented and pre- and post-synaptic spikes shape is the same as Zamarreño-Ramos *et al.* (2011), implementing the competitive Hebbian learning rule (Song *et al.* 2000). Initial states have been shown in Figure 9.6 (c) are shown in red. Intentionally, a Gaussian distribution has been employed for the memristors' initial state values. After running the simulation for 35 minutes, the network results in a population distribution of weights similar to a previously published competitive Hebbian learning rules (Song *et al.* 2000). The additive and multiplicative features of a memristive network strictly depends on the device and its nonlinearity parameters. Figure 9.6 (b) demonstrates a Poissonian ISI distribution which is applied to the array. To the best of the author knowledge, this is the first circuit demonstration a memristor-based array that shows an implementation of competitive Hebbian learning rules (Kavehei *et al.* 2011b).

9.3.5 Programmable analogue circuits

Although neural plasticity plays an important role for adaptation and development, networks with fixed synaptic weight pattern should be also studied. Therefore, one of the challenges for this emerging technology is to integrate learning and unlearning hardware as part of a neural computational platform. Since memristors possess a threshold-like behaviour, usually low- or very low-voltage operations do not change the memristor's initial state. This fact helps developing programmable analogue computing circuits (Pershin and Di Ventra 2010). There is also a similar design in Mouttet (2009), however the design presents neither simulation nor experimental results.

This section introduces the use of a memristive array for implementing a multiplication of inputs and the memristor's internal state, w, which represents the memristor's conductance. Figure 9.7 (a) illustrates a single row of the array and Figure 9.7 (b) shows its simulation results for two elements, M1 and M2, connected to two inputs, In_1 and In_2. In this case, first a voltage pulse to M1 was applied to read its conductance, then a
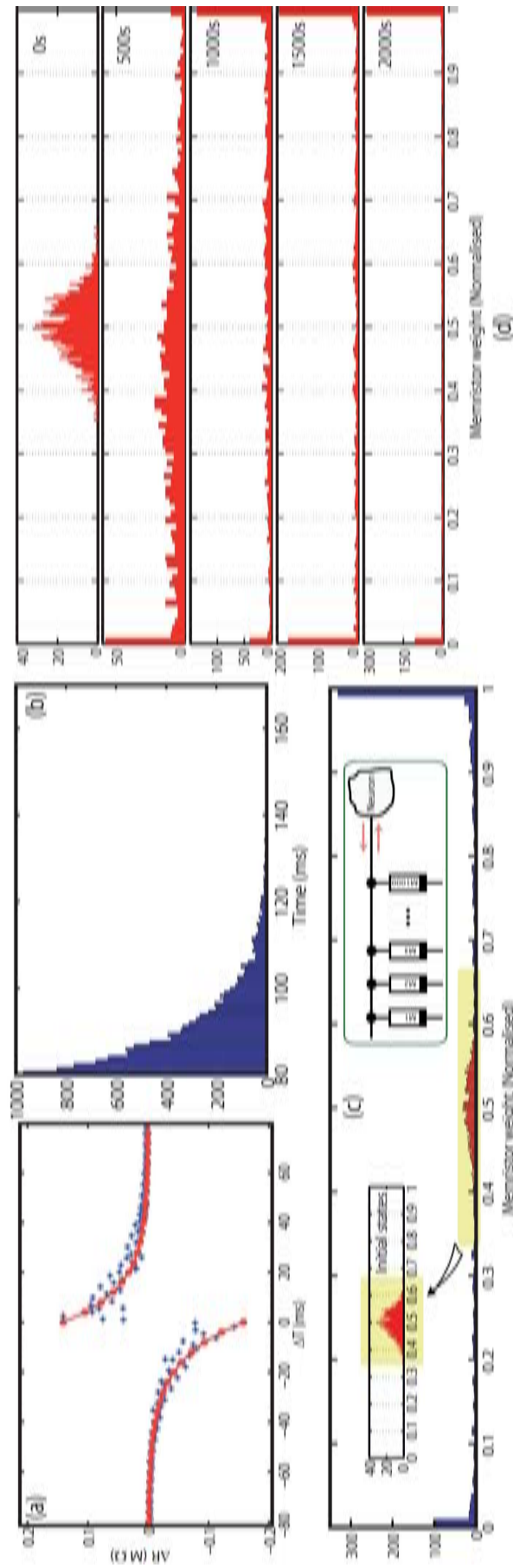
Figure 9.6. Synaptic weight evolution in an array of memristors. Memristor neural plasticity and competitive learning. (a) Dots illustrate experimental data and the solid (red) line shows the fitting STDP rule. We exclude devices that reach lowest and highest conductances in depression and potentiation processes, respectively, because they add no extra information to our analysis. (b) A Poisson inter-spike interval (ISI) distribution for 1×1000 memristors (synapse) connected to one neuron, inset in (c). (c) Illustrates simulation results of such network. It is clear that it follow the competitive learning behaviour reported in Song *et al.* (2000). (d) Evolution of synaptic strength from 0 s to 2000 s.

pulse to M2 for the same reason. When two voltage pulses are simultaneously applied to M1 and M2, accumulation operation can be clearly observed.
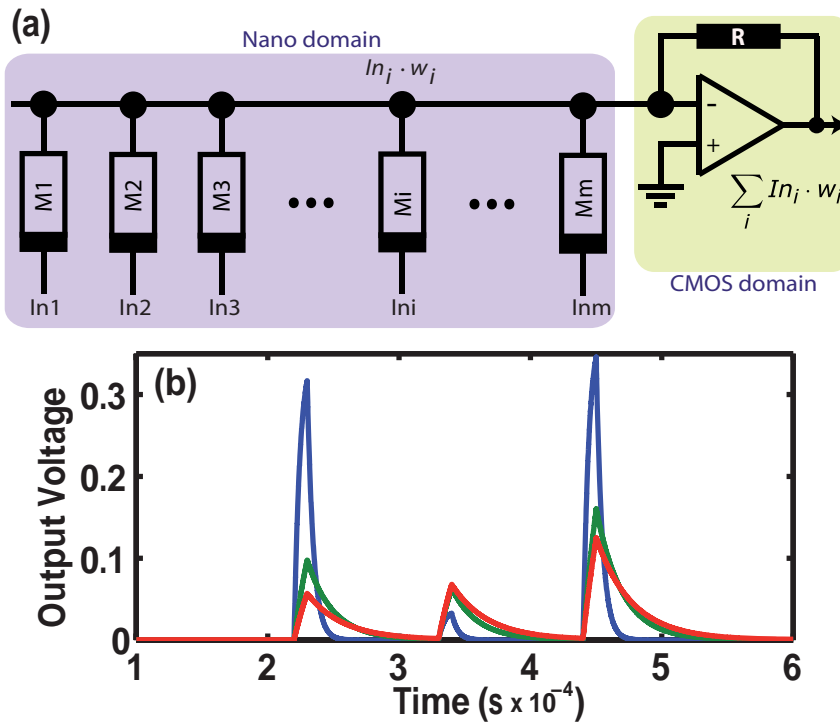
Figure 9.7. A memristor-based multiply-accumulate module for biomimetic applications. Multiply-accumulate module. (a) Shows a single row of multiply elements (memristors), $In_i \cdot w_i$. (b) Demonstrates simulation results for two memristors, M1 and M2. In this simulation, memristor M2 programmed at $x = 0.5$, which is equivalent to $(R_{\mathrm{HRS}} + R_{\mathrm{LRS}})/2$. Then memristor M1 changes its resistance from R_{LRS} to R_{HRS} in three steps. Each step is a simulation that is shown with different colours. Blue for $R_{\mathrm{M1}} = R_{\mathrm{LRS}}$, green for R_{M1} close to $(R_{\mathrm{HRS}} + R_{\mathrm{LRS}})/2$, and red for R_{M1} close to R_{HRS}. The summing amplifier can be replaced by any threshold module for different applications.

9.4 Conclusion and future work

This chapter introduced basic functional blocks for analogue and digital computation based on memristive devices. It is difficult to have a fair comparison between emerging and the conventional devices as the emerging technologies are at their early stages. Moreover, architectural aspects for future computers seems to be dependent on the concept of universal memory and computational capability of one individual device or nano-system that is entirely different with the classical von Neumann computational

framework. Therefore, introducing more compatible circuits and algorithms with these futuristic technologies could play an important role. This work presented the existence of ionic drift in the fabricated memristors. This chapter was also illustrated how the memristor can be used to implement competitive Hebbian learning (additive STDP). An analogue multiplication-accumulation circuit (MAC) was introduced that is able to implement a low precision multiplication and addition. This circuit combines inherent non-volatile memory and dynamics of a memristor as a synapse. The problem of state decay can be addressed by using a digital version of such learning system. A complete implementation of such algorithm in digital domain is out of the scope for this thesis. However, the concept of digital computing using a more robust memristive device, CRS, was explained and two methods for implementing logical blocks were introduced. The next chapter concludes the thesis and summarises the original contributions.

Chapter 10

Summary and Future Work

CONCLUSION and outlook of the integration of resistance switching materials into a hybrid CMOS/Nano structure and ultimately in entirely passive nanocrossbar arrays are summarised in this chapter. A common conclusion that can be found in all publications on emerging and advanced device technologies is that RRAM, CRS, Programmable Metallization Cell (PMC) or Conductive Bridging RAM (CBRAM), PCM, STT-MRAM, Ferromagnetic RAM (FeRAM), graphene, Carbon Nano Tube (CNT), Single Electron Transistor (SET), molecular two- or three-terminal device, organic switch, Resonant Tunnelling Devices (RTD), spin transistor, or any other emerging technology will be limited as scaling rate cannot continue for ever. This fact and the inherent properties of memristors motivated the author to carry out research on this emerging topic. According to the presented measurement and simulation results, this thesis has presented a comprehensive analysis of fundamental circuit and system blocks based on memristive devices that pave the way for the future research in this area toward numerous new applications. This study mainly focused on the modelling and circuit applications of crosspoint junctions as single memory elements and crossbar arrays as the most promising architecture of the future memories.

[This page has been left blank intentionally.]

10.1   Part I—modelling and fabrication

Introducing the concept of resistance modulation index and an early SPICE macro-model of memristive device: Chapters 2 and 3

Background: Among various memristor features, two key properties have attracted significant attention. First, its non-volatile memory characteristic and, second, its nanometer scale dimensions. In the case of resistor and memristor the equations are similar apart from the inclusion of an integral sign on both side of the equation for memristor. For simplicity, this constant can be viewed as the parameter that permits the memristor to remember its "last resistance" it had, or in other words, the device's new state is strongly depend on the history of device states. In analogy to the early days of silicon CMOS technology, modelling methodologies are evolutionary as the memristive technology matures. Accordingly a deeper insight is gained by understanding of the device operation, leading to the development of practical models that can be implemented in current CAD tools.

Methodology: The modelling approach is based on the constitutive relationship between the charge and the flux. A direct consequence of the HP's first model can be the resistance modulation index which simply defines the changes of resistance as a function of history of applied voltage at a given time. The early SPICE model implements the relationship between the history of current (q) and the history of voltage (Φ) through a macro-model. In this model switching is modelled by switching between two different resistances.

Result: The method has a moderate success. It has shown that the model meets the requirements from Chua and Kang (1976) to be named a memristor model. It was also tested in circuits with different passive circuit elements and has confirmed expectations. It has also simulated with an operational amplifier to implement a multi-time constant integrator circuit.

Future work: Although, the model is working properly for digital applications, an improvement to the proposed method is required to deal with the memristor's non-linearity that cannot be modelled accurately using such basic structure. The concept of resistor-memristor (RM), capacitor-memristor (CM), inductor-memristor (LM), and

resistor-inductor-capacitor-memristor (RLCM) circuits have been presented and well defined mathematically by Lam (1972), however, there has been very little effort toward releasing nanometer scale nonlinear networks containing memristors to experimentally confirm those theoretical information. The sensitivity and stability of this new class of networks cannot be directly gained from the conventional nonlinear network analysis without memristor (Lam 1972). Therefore, the future work here can be define as a comprehensive sensitivity and stability analysis of nonlinear networks containing memristor, e.g. resistive (memristive) networks for early vision processing.

Original contribution: For the first time, the concept of resistance modulation index is introduced and SPICE simulation of CM and LM networks are carried out (Kavehei *et al.* 2010). Fundamental switching characteristics of memristor is explained and modelled using SPICE.

Observation of memristive behaviour in the fabricated Ag/TiO$_2$/ITO memristor: Chapter 4

Background: Different materials can be used and hence different properties can be achieved. This chapter introduces memristive materials and reviews the recent progress in the Resistive Random Access Memory (RRAM) technology. The traditional scaling scheme cannot maintain the progression of flash memories. It is observed that for generations beyond 20 nm, flash's endurance is significantly decreased due to the phenomenal increase in leakage currents. Therefore, a technological shift is almost inevitable and it is believed that RRAMs is one of the most promising emerging non-volatile technologies.

Methodology: Due to the fact that it is assumed that the conduction mechanism of Metal-Insulator-Metal (MIM) structure is based on the change in the distribution of oxygen vacancies within the nano-layer memristive material and a coupled ionic and electronic transport, the top electrode's properties, e.g. electrode potential and work function, play an important role during the switching process. The decision to use Ag was made on the grounds of using another top electrode with a lower work function (than Pt), which is more fabrication-friendly. As a result, it can be understood that any material or combination of materials that has impact on the barrier height at the top electrode-TiO$_2$ interface plays a key role in the shape and uniformity of switching.

Result: The fabricated devices have exhibited bipolar ON and OFF switching as well as multi-stable state behaviour. It is observed that decay does not seem to be a big problem for digital application of such memory devices, whereas functional uniformity does create the main source of issue. According to the bipolar behaviour of the device and also memristive fundamentals, intuitively (see Figure 4 (b) in Kim *et al.* (2011d)), asymmetric applied voltages in this case (or asymmetric applied pulse width) should improve the switching uniformity for digital applications. It has been observed that such understanding from memristor's fundamentals helps in improving switching behaviour of the devices under test.

Future work: The selection of a new material set and using their different properties have strong impact on the functionality of nanometer scale devices. A fairly straight-forward future direction is device optimisation based on the previous understanding

and the available knowledge about materials. fabrication-friendly, high oxidation resistance, and high work function are only three properties that a top electrode is expected to have. These properties is very much like gate metal's properties of the advanced MOS transistors, e.g. titanium aluminium nitride (TiAlN) and titanium nitride (TiN) coatings. Application of these materials as electrodes is not well explored (Akinaga and Shima 2010). On the other hand, the barrier height at the top electrode and resistance (memristive) material interface depends oxygen vacancy concentration in the memristive material. At the same time, the metal oxide material should provide a simple and fabrication-friendly process, high ionic conductivity, high Schottky barrier height, and reliable operation at high temperature. This list would lead to the use of hafnium oxide (HfO_2) and zirconium oxide (ZrO_2), for example. Another research path can be considered according to the possibilities introduced by Gao *et al.* (2009). They claimed that more oxygen vacancies would supposedly lead to more uniform conductive filaments in terms of LRS and HRS resistances, forming voltages, and threshold voltages. They used a doped metal oxide, in this case Al-doped HfO_2. The mechanism is to have a more systematic filament path rather than the random filaments in an undoped HfO_2. This approach can be combined with the explained research path to improve robustness, endurance, retention, and energy efficiency of the future memory devices. In addition, control mechanisms on the SET current is necessary due to the fact that normally higher SET currents needs higher RESET currents to break filaments. These control mechanisms can be used as an additional circuitry in the programming phase.

Original contribution: The structure is unique among many implemented memristive devices. The measured switching behaviour has shown a good functional uniformity as well as the existence of a non-volatile bistable and multi-stable memory that is remarkably important for the rest of the contributions of this thesis (Kavehei *et al.* 2011d).

SPICE macromodel for memristor based on its underlying switching behaviour: Chapter 5

Background: Memristor modelling is the key point for assisting circuit designers to work on memristive-based circuits. The significance of this modelling comes from the fact that this nanoscale device enables us to introduce new on-chip computation, which is promising for the future of artificial intelligence and radically different computer architectures. One of the very first steps toward this vision is in providing a device model that is compatible with commonly accepted design modelling packages such as SPICE. The fact that some of the memristive elements, e.g. Complementary Resistive Switch (CRS), do not have available a SPICE model motivated the author to extend the use of memristor model for CRS modelling.

Methodology: This part of the thesis is primarily concerned with the development of simple models that will assist us in the understanding of circuits and system behaviour providing the basis whereby system performance, in terms of signal delays and power dissipation can be estimated. The model is an analytical and empirical model that describes the switching characteristics of a memristor. The model is tested against measured data and has shown a good agreement with experimental results. According to the available information in Chapter 5, back-to-back connection of two bipolar memristors in series should results in a CRS device. This fact is tested for the first time on a Ag/TiO$_2$/ITO memristor and results were demonstrated.

Result: The introduced model is in a good agreement with the measured data. Experimental results from connecting two bipolar memristors is also resulted in a CRS-like function. It has been stated here that CRS device can be treated like a memistor with a floating control node. A CRS model is also presented according to the fundamental switching characteristics of the memristor.

Future work: Improving the presented model to be more coupled with the device geometry is the next step. In addition, switching asymmetry and dependency of the conductance change to the initial conductance can be considered for future work. Using a series of applied pulses it has been primarily observed that this relationship is in fact a high nonlinear (exponential) relationship. It is also observed that at low-voltages, memristor's conductance depends on $\sinh(\sqrt{V})$, therefore, it will create issues for some of the applications, such as the linearised differential pair (Varghese

and Gandhi 2009). These properties emphasis the need for more detailed models. Furthermore, despite several applications for the inherent decay of the device state (Ohno *et al.* 2011, Chang *et al.* 2011), the source of such mechanism is neither well studied nor well characterised.

Original contribution: A new memristor model was introduced and its functionality was confirmed with the experimental data (Kavehei *et al.* 2011d). For the first time, a CRS model was developed and its functionality was achieved using a back-to-back connection between two different bipolar memristive elements (Kavehei *et al.* 2011a).

10.2   System overview

Introducing overall perspective of the targeted system and implementation of CMOS image sensor: Chapters 6

Methodology: System overview of the targeted structure for the contributions of this thesis was given. The system consists of several layers of integrated circuits stacked on top of each other. The first and the second layers, CMOS image sensor and memristive memory and logic, are included in the context of this thesis. The image sensor array produces digital outputs corresponding to the incident light. The imager functionality is carried out through two different concepts, pulse-width and pulse-frequency modulation. Both of the designs were fabricated and tested and related reports are verified. The memristive based array consists of an associative memory as well as memristive-based computational modules. These two layers will be connected using a hardware interface for image feature generation. The image feature generation algorithm is adopted from the literature. It is a rotation-invariant scheme that makes it suitable for any image recognition purposes and in particular the targeted system's application.

Result: A system overview was reviewed and the unique properties of such system were discussed. Two separated layers of image sensors and memristors are introduced and the link between the two was also identified. The results in this part are mainly around the functionality and performance of the two type of CMOS image sensors. The pulse-width modulation (PWM) has shown an acceptable dynamic range at a very low operation, which shows an improvement in comparison with other available designs. In the design of pulse-frequency modulation (PFM) cells a new type of Schmitt trigger circuit is used to reduce power consumption while maintaining the low-voltage operation. The result successfully shows a relatively low power consumption compare to other implementations and a very robust performance under a wide range of light intensities.

Ongoing work: A joint implementation of such structure is an ongoing project which is underpins of further research. The expected full system will be used to carry out early vision processing tasks such as edge detection and smoothing as well as feature generation for pattern matching applications.

Original contribution: The system structure and the type of application are new (Lee *et al.* 2010). The need for a massive memory-logic implementation required a radically different memory array with high density and low-power properties. The single inverter PWM structure and the application of new type of Schmitt trigger circuits in the PFM pixel are also two further contributions.

10.3 Part II—nanocrossbar array properties and memristive-based memory and computing

Nanocrossbar array and a comprehensive modelling approach: Chapter 7

Background: One particular problem that dominates the maximum crossbar array size is interaction between selected cell with neighbouring cells due to sneak-path currents. A possible device level solution to compensate this issue is to implement memory array using CRS. Therefore, it is very important to verify, through simulations, fabrication, and analytical approach, that how significant are these improvements.

Methodology: Two types of memristive arrays were implemented: (i) memristor-based without a diode or any selective device in series, and (ii) CRS based. For each one, a comprehensive approach for modelling a crossbar array including all parasitic resistors for bit- and word-lines was presented. This approach can be combined with a system of linear equations that enable designers to determine voltage value at each particular node. This combination has led to a comprehensive analytical approach that allows designers to find optimum values for particular design parameters.

Result: Simulation results indicated that due to sneak-paths, a memristive array is faced with an inaccurate write or reading, which aggressively limit the maximum nanocrossbar array size. However, the read margin in a CRS array is robust against process and programming variations such as uncertainty in the initial state programming, nanowire process variation, and the associated uncertainty on the low resistance state programming. Results of simulations also indicated that the most important parameter that should be increased to achieve higher array sizes for a memristive array is R_{LRS}. This research verified that a high r ($= R_{\text{HRS}}/R_{\text{LRS}}$) does not substantially reduce the amount of parasitic path currents, while a high R_{LRS} value ($> 3\,\text{M}\Omega$) guarantees a successful READ and WRITE operations.

Future work: Perhaps the most important problem with the CRS based memory array is the destructive read-out. This would lead to a high number of refresh cycles (WRITE) for each READ (1.5 programming and refreshing cycles for each read access cycle). This shortcoming can be improved using a new read-out technique from Tappertzhofen *et al.* (2011).

Original contribution: Introducing a comprehensive analytical method which included: (i) parasitic element in the crossbar array, (ii) system of linear equations for finding voltage pattern in the array, (iii) SPICE implementation of a memristor and CRS based arrays, (iv) a detail comparison based on the SPICE simulations between CRS based and memristor based arrays (Kavehei *et al.* 2011a).

Memristor-MOS content addressable memory (MCAM) and CRS-CAM: Chapter 8

Background: Large-capacity Content Addressable Memory (CAM) is a key element in a wide variety of applications, e.g. pattern matching and recognition in particular. The inevitable complexities of scaling of MOS transistors introduce a major challenge in the realisation of such systems. Convergence of disparate and significantly different technologies and that are compatible with CMOS processing would allow extension of Moore's Law for a few more years.

Methodology: We consider a memristor as a resistor with two different resistances combined with MOS transistor parasitic capacitors. Different resistance results in different time constants, which can be used to implement a memristor-MOS type structure. In such implementation, transistors are part of the CAM cells and acting as switches, while memristors are responsible for keeping data. In this approach, a non-volatile CAM implementation can be achieved. Although, the design is very promising, the combination of transistors in the nano domain to act as the selective device limits scaling of this design. An ultimate goal is to eliminate transistors and diodes from the nano domain and include only resistive elements, such as two back-to-back memristors (CRS). The first step toward such structure is done by introducing the CRS-CAM. This cell works based on the material implication logic implementation of XOR and XNOR gates.

Result: The simulation results show that the MCAM approach provides a 45% reduction in silicon area when compared with the SRAM equivalent cell. The Read operation of the MCAM ranges between 5 ns to 12 ns, for various implementations, and is comparable with current SRAM and DRAM approaches. However, the Write operation is significantly longer, which can be improved by applying higher voltage potentials. This approach would result in using larger transistors which also can be solved by a differential applied voltage approach. The CRS-CAM also showed the functionality of both binary and ternary CAM which is quite useful for the targeted application. The inclusion of only two resistors (2R) in the nano domain together with the promising results on the CRS-based array size and the non-destructive read-out method in Tappertzhofen *et al.* (2011) results in a clear picture toward the future of CRS-CAM.

Future work: Addressing the non-destructive read-out technique (Tappertzhofen *et al.* 2011) of the CRS-CAM will be of prime interest and will allow for a much faster memory operation.

Original contribution: The memristor-based CAM and CRS-CAM designs are introduced for the first time. The concept of logic→ON state transitions together with the implementation of 'material implication' for such transitions are also introduced for the first time (Eshraghian *et al.* 2011b, Kavehei *et al.* 2011c).

Memristive based in-situ computing properties: Chapter 9

Background: The classical von Neumann machine suffers from large sequential (fetch-execute-store cycle) processing overload due to the existence of the data bus between memory and logic. On the other hand, a biologically-inspired computing system needs extraordinary number of elements (neurons and synapses). Therefore, the classical methods do not certainly lead to an answer for future of computing and neuromorphic engineering.

Methodology: This part has introduced a method, which is based on the inherent computing capability of memristors that can be shown experimentally in the context of material implication logic. The concept of 'material implication' together with the non-volatile memory capability and multi-stable state characteristics of memristors has led to a radically different technique in computing in the both forms of analogue and digital. The analogue and biomimetic circuits implementations are also implemented by adjusting the memristor's conductance values (weights) as a function of the timing difference between presynaptic and postsynaptic spikes.

Result: This part presented new computational building blocks based on memristive devices. Based on these blocks and an experimentally verified SPICE macromodel for the memristor, the implementation of the spike timing-dependent plasticity (STDP) was demonstrated using a single memristor device and the competitive Hebbian learning through STDP using a 1×1000 synaptic network. These implementations had a number of shortcomings due to the memristor's characteristics such as memory decay, highly nonlinear switching behaviour as a function of applied voltage, and functional uniformity. These shortcomings can be addressed by utilising a digital approach that can be used in conjunction with the analogue behaviour for biomimetic computation. The digital implementations also used the in-situ computational capability of the memristor that is used in similar way to implement CRS-CAM cells in Chapter 8.

Future work: This is just the starting point for the CRS-based logic. This technology enables energy efficient and ultra-high density nonvolatile memory and digital computing.

Original contribution: CRS-based logical operations were introduced. This thesis introduced a flexible technique in implementing logical gates using CRS devices, which bypassed the shortcomings of the recent technique introduced by Rosezin *et al.* (2011). Their technique is fairly limited and it is very difficult to extend such method to build logic gates other than a NOR and an AND. The non-destructive read-out is also not an issue here due to the fact that the device must be initially programmed by the logic value of one of the inputs. For the first time, a memristor-based multiplication-accumulation (MAC) operator module is simulated. The demonstration of STDP learning rule by a single memristor is also shown and for the first time a large array of memristors showed the implementation of an (additive) competitive Hebbian learning rule through SPICE simulation.

Appendix A

Electromagnetic Theory of Memristors

ELECTROMAGNETIC theory of memristors provides an understanding how the 4th fundamental element can be seen from the quasistatic expansion of Maxwell's equations. For the first time, we show how this insight can be gained in a clearer way by exploiting a unified form of Maxwell's equations based on Geometric Algebra (GA).

[This page has been left blank intentionally.]

A.1   The link to Maxwell's equations

Regarding the very first memristor argument (Chua 1971), using the quasistatic expansion of Maxwell's equations, proposing a link between the first order terms in the expansion $\mathbf{D_1}$ and $\mathbf{B_1}$, which are the first order electric and magnetic flux densities, respectively, we can now identify these elements as connecting $\frac{dV}{dt}$ and $\frac{di}{dt}$, as shown in Figure 2.1. For linear systems, the memristor becomes equivalent to a resistor, and hence the memristor can be seen as a special case that relates $\mathbf{D_1}$ to $\mathbf{B_1}$.

Beginning from the electrostatic field in conjunction with the relativity principle and Maxwell's equations, we show how the fundamental circuit elements can be derived. Table A.1 in fact, can be seen as an underlying motivation to Figure 2.1. It was first shown by Einstein, that an electrostatic field will register magnetic fields, when viewed by an observer from a relatively moving frame. Hence, the most fundamental aspect of Maxwell's equations is the electrostatic field, defined by the single parameter charge q, creating an electrostatic potential V. However this is sufficient to define capacitance with the relation $q = CV$. The field can then be found from $\mathbf{E} = -\nabla V$, or we can calculate the field directly from the charge distribution ρ, according to Maxwell's first equation $\nabla \cdot \mathbf{E} = \frac{\rho}{\epsilon}$. We can thus view capacitance as the first fundamental circuit element, shown in Table A.1.

For the non-electrostatic case, we have the magnetic field, which is described by the flux calculated from the inductance L, given by $\Phi = Li$ (Ampère's law, Maxwell's third equation). We have $\Phi = \int V dt = Li = L\frac{dq}{dt}$ and hence, differentiating with respect to time, $V = L\frac{d^2q}{dt^2}$. Thus, α_e and β_e in Figure 2.1 increase one unit by the differentiation and this relation therefore presents inductance as the second generation of fundamental circuit element, as shown in Table A.1. During steady currents, inductors have no reactance, but AC currents produce a fluctuating magnetic field in the inductor that according to Faraday's law (Maxwell's second equation) will produce a back emf proportional to $\partial_t B$, as given by $\nabla \times \mathbf{E} = -\partial_t B$, which is shown in the third line of Table A.1.

A.1.1 Resistance in the Maxwell picture

Based on Maxwell's equations, the first two fundamental circuit components are loss-less. In order to identify the third fundamental element we need to allow energy dissipation. We might expect from the Lorentz force law that charges will accelerate in an electric field because of the relation $\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B})$. In a dielectric the electrons soon hit terminal velocity, and will drift at a constant velocity v_d. Here, due to the relatively low velocities, we can neglect the magnetic force in circuits. The new law is simply Ohm's law, $V = Ri$, where the steady current $i = A_x \sigma \mathbf{E}$, σ is the conductance of the material and A_x is the cross-sectional area of the element. Hence we have $V = R\frac{dq}{dt}$, linking potential with the first time derivative of charge. Hence we can consider R as the third fundamental element. Even though resistance depends on Ohm's law and not Maxwell's electromagnetic equations, a steady current can be simulated with a moving reference frame past a static charge and hence from this perspective resistance can be considered fundamental.

A.1.2 Questions surrounding the 4th element

From Figure 2.1, it can be seen that the memristor completes the square of circuit variables Φ, V, i, q, with a link between Φ and q. Moreover, it may be argued that the concept of memristive systems developed later, which include meminductors and memcapacitors, leads us to classify the memristor as the first new element in a second generation of circuit elements based on the integrals of the circuit variables q, V, i, and Φ.

It appears that there are two threads to Chua's original argument for a memristor: a) memristor as a basic two-terminal circuit element that establishes a link between charge q and magnetic flux Φ, b) a circuit theory perspective, along the line that a memristor in fact links the quantities $\mathbf{D_1}$ and $\mathbf{B_1}$ in the quasistatic expansion of Maxwell's equations. A natural question would be then how these two seemingly distinct approaches to the basic physical principles of a memristor are related with each other? In particular, how the link between q and Φ can be re-expressed in terms of $\mathbf{D_1}$ and $\mathbf{B_1}$ and vice versa? Fano *et al.* (1968) stated 'Quasi-static fields involving both first-order fields fall outside the scope of circuit theory'. However, Chua was expecting an element linking the first order electric and magnetic fields. A possible answer to this conflict, is the

Table A.1. Fundamental circuit elements. Electromagnetic interpretation of the fundamental passive circuit elements.

Physical level	Variables	Element	Field	Property	Relation
1. Electrostatic	q, V	$q = CV$	$\mathbf{E} = -\nabla V$	Capacitance	$V = \frac{1}{C}q$
2. Accel. charge	$\frac{d^2 q}{dt^2} = \frac{di}{dt}$	$\Phi = Li$	$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$	Inductance	$V = L\frac{d^2 q}{dt^2}$
3. Diffusion	$\frac{dq}{dt}$	$V = Ri$	$\mathbf{J} = \frac{i}{A_x} = \sigma \mathbf{E}$	Resistance	$V = R\frac{dq}{dt}$

$\mathbf{D_1}$ and $\mathbf{B_1}$ relation points to a resistive type component, but lying between the variable pairs $\frac{dV}{dt}, \frac{di}{dt}$ as opposed to the variable pairs Φ, q for HP's memristor. Alternatively, there is also perhaps scope for a new circuit element using Ampère's law (Maxwell's third equation) using the property of a changing electric field related to changing the magnetic field given by $\nabla \times \mathbf{H} - \frac{\partial \mathbf{D}}{\partial t} = \mathbf{J}$.

A.2   Quasi-static expansion of Maxwell's equations

Circuit theory can be treated as a special case of electromagnetic field theory, using the quasi-static expansion of Maxwell's equations (Chua 1971, Kavehei *et al.* 2010). Although, in order for the expansion to converge we require the dimensions of the circuit elements to be smaller than the wavelength of the highest frequency being applied (Fano *et al.* 1968). In the presence of dielectrics, Maxwell's equations are typically written, in S.I. units, as

$$
\begin{aligned}
\nabla \cdot \mathbf{D} &= \rho \quad (\text{Gauss's law}), \\
\nabla \times \mathbf{E} + \frac{\partial \mathbf{B}}{\partial t} &= 0 \quad (\text{Faraday's law}), \\
\nabla \times \mathbf{H} - \frac{\partial \mathbf{D}}{\partial t} &= \mathbf{J} \quad (\text{Ampère's law}), \\
\nabla \cdot \mathbf{B} &= 0 \quad (\text{Gauss's law of magnetism}),
\end{aligned}
$$

where we use the constitutive relations to allow for the polarization $\mathbf{P}$ and magnetization $\mathbf{M}$ of dielectrics

$$
\begin{aligned}
\mathbf{D} &= \epsilon_0 \mathbf{E} + \mathbf{P} = \mathcal{D}(\mathbf{E}), \\
\mathbf{B} &= \mu_0(\mathbf{H} + \mathbf{M}) = \mathcal{B}(\mathbf{H}),
\end{aligned}
$$

so that ρ and $\mathbf{J}$ refer to free charges and currents respectively and $\mathbf{E}, \mathbf{B}$ are the vector fields with ∇ the vector gradient.

Maxwell's four equations along with the Lorentz force law

$$\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B}),$$

completely summarize classical electrodynamics (Griffiths and Inglefield 1999). The charge continuity equation $\nabla \cdot \mathbf{J} = -\frac{\partial \rho}{\partial t}$ is contained within Ampère's law. If we assume the behaviour of charges in a dielectric is governed by Ohm's law, then we also have $\mathbf{J} = \sigma \mathbf{E}$, where we have ignored the magnetic component of the Lorentz force.

If we include a time rate parameter α, then we define the family time $\tau = \alpha t$, then Maxwell's equations, which include a time derivative, become (Fano *et al.* 1968, Kavehei *et al.* 2010)

$$\nabla \times \mathbf{E} + \alpha \partial_\tau \mathbf{B} = 0,$$
$$\nabla \times \mathbf{H} - \alpha \partial_\tau \mathbf{D} = \mathbf{J}.$$

We can define the vector fields, as a power series in α, for example using the electric field we have

$$
\begin{aligned}
\mathbf{E} &= \mathbf{E}_{\alpha=0} + \alpha \left.\frac{\partial \mathbf{E}}{\partial \alpha}\right|_{\alpha=0} + \frac{\alpha^2}{2} \left.\frac{\partial^2 \mathbf{E}}{\partial \alpha^2}\right|_{\alpha=0} + \dots \\
&\quad + \frac{\alpha^k}{k!} \left.\frac{\partial^k \mathbf{E}}{\partial \alpha^k}\right|_{\alpha=0} + \dots \\
&= \mathbf{E}_0 + \alpha \mathbf{E}_1 + \alpha^2 \mathbf{E}_2 + \dots + \alpha^k \mathbf{E}_k + \dots
\end{aligned}
\tag{A.1}
$$

where

$$\mathbf{E}_k = \frac{1}{k!} \left.\frac{\partial^k \mathbf{E}}{\partial \alpha^k}\right|_{\alpha=0}.$$

Therefore the relevant Maxwell's equations become

$$
\begin{aligned}
&\nabla \times \mathbf{E_0} + \alpha(\nabla \times \mathbf{E_1} + \partial_\tau \mathbf{B}_0) + \alpha^2(\nabla \times \mathbf{E_2} + \partial_\tau \mathbf{B}_1) \\
&+ \dots = 0 \\
&\nabla \times \mathbf{H_0} + \alpha(\nabla \times \mathbf{H_1} - \partial_\tau \mathbf{D}_0) + \alpha^2(\nabla \times \mathbf{H_2} - \partial_\tau \mathbf{D}_1) \\
&= \mathbf{J_0} + \alpha \mathbf{J}_1 + \alpha^2 \mathbf{J}_2 + \dots \\
&\mathbf{J}_0 + \alpha \mathbf{J}_1 + \alpha^2 \mathbf{J}_2 + \dots = \sigma(\mathbf{E}_0 + \alpha \mathbf{E_1} + \alpha^2 \mathbf{E_2} + \dots).
\end{aligned}
$$

Equating orders we find firstly, the zero order Maxwell's equations

$$
\begin{aligned}
\nabla \times \mathbf{E_0} &= 0, \\
\nabla \times \mathbf{H_0} &= \mathbf{J_0},
\end{aligned}
$$

and first order Maxwell's equations

$$
\begin{aligned}
\nabla \times \mathbf{E_1} + \partial_\tau \mathbf{B_0} &= 0 \\
\nabla \times \mathbf{H_1} - \partial_\tau \mathbf{D_0} &= \mathbf{J_1} .
\end{aligned}
\tag{A.2}
$$

In the standard approach, we would start with the zero order fields, solving in the static case and by substituting these results into the first order equations we can then solve these equations and so on, up to as many orders as required to converge to the exact solution. These are then substituted into equations of the form Eq. (A.1) to find an approximation to the full time varying field.

Chua (1971) argued for a new electrical component, that established a link between $\mathbf{D}_1$ and $\mathbf{B}_1$, which are the first order fields in the quasistatic expansion, and that these quantities are evaluated instantaneously. From Ohm's law and constitutive relations, Chua writes the relationships between the first order fields as

$$
\begin{aligned}
\mathbf{J}_1 &= \mathcal{J}(\mathbf{E}_1), \\
\mathbf{B}_1 &= \mathcal{B}(\mathbf{H}_1), \\
\mathbf{D}_1 &= \mathcal{D}(\mathbf{E}_1),
\end{aligned}
$$

where $\mathcal{J}$, $\mathcal{B}$, and $\mathcal{D}$ are one-to-one continuous functions defined over space coordinates only. When $\mathbf{E}_0, \mathbf{D}_0, \mathbf{B}_0$ and $\mathbf{J}_0$ are negligible in the quasistatic expansion of Maxwell's equations, using Eqs. (A.2) we are then led to a relationship between $\mathbf{D}_1$ and $\mathbf{B}_1$, which Chua used as a basis to postulate the memristor.

A.2.1   Derivation of memristor category

From the relation $\mathbf{D_1} = \mathcal{F}(\mathbf{B_1})$ we find in terms of the scalar magnitudes

$$
\epsilon \frac{\partial E}{\partial \alpha} = \frac{\partial f(B)}{\partial \alpha} = f(w)\frac{\partial B}{\partial \alpha}
$$

where $f(w)$, dependent on a state variable w, must not be a function of B or the time scale α. Hence $\epsilon dE = f(w)dB$ or for a circuit element assuming $E = V/D$ we have

$$
\frac{\epsilon}{D}V = f(w)f(s)\frac{\mu i}{2\pi}
$$

where $f(s,z) \approx 1/s$ gives the spatial distribution of B, where s is the radius in cylindrical coordinates. Hence we find

$$
V = R(w)\frac{dq}{dt} .
$$

Hence Chua's relationship between $\mathbf{D_1}$ and $\mathbf{B_1}$ implies a memristor type element depending on a state variable w. The HP memristor, for example, has w proportional to q.

A.3   Quasi-static expansion of Maxwell's equations using geometric algebra

The quasi-static expansion of Maxwell's equations was used by Chua in order justify the existence of a new circuit element he called the memristor. Geometric algebra (GA) (Doran *et al.* 2003) is known to produce a very efficient representation of Maxwell's four equations, requiring just a single equation, and so by producing the quasi-static expansion in GA, clearer insights may be forthcoming. It should be noted that the expansion series is not guaranteed to converge and so perhaps not too much should be read into different components of a perturbation series, however it does provide insights into possible field and current relationships.

In GA, Maxwell's equations can be written in single equation in linear isotropic media (Vold 1993) as

$$(\frac{1}{c}\partial_t + \nabla)F = J,$$

where $F = c\mathbf{D} + i\mathbf{H}$, $J = c\rho - \mathbf{J}$ and c being the speed of light. Geometric algebra typically represents multivector variables such as F and J, in plain type, as opposed to pure vectors which are identified with bold type. Using the expansion given in Eq. (A.1), we can write

$$(\frac{\alpha}{c}\partial_\tau + \nabla)(F_0 + \alpha F_1 + \alpha^2 F_2 + \ldots)$$
$$= (J_0 + \alpha J_1 + \alpha^2 J_2 + \ldots).$$

Hence it is easy to see that the orders of the quasistatic expansion become

$$\begin{aligned} \nabla F_0 &= J_0, \\ \partial_\tau F_0 + \nabla F_1 &= J_1, \\ \partial_\tau F_1 + \nabla F_2 &= J_2, \\ \ldots &= \ldots \end{aligned}$$

The process of solution is now very clear in GA. From the zeroeth order fields we calculate F_0, which is substituted into the first order fields to find F_1, and so on.

Chua also states that $\mathbf{D_0} = \mathbf{H_0} = 0$ and hence $F_0 = 0$. Therefore, we have the relation

$$\nabla F_1 = J_1 \ .$$

This equation fixes the value of F_1, and hence there must be a relationship between $\mathbf{D_1}$ and $\mathbf{H_1}$ or equivalently, $\mathbf{D_1}$ and $\mathbf{B_1}$, as deduced by (Chua 1971), which again is the memristor element.

Confirm equivalence of GA with vector calculus form

The geometric product between two vectors is given by (Doran *et al.* 2003)

$$\mathbf{uv} = \mathbf{u} \cdot \mathbf{v} + i\mathbf{u} \times \mathbf{v} \ .$$

Expanding and equating scalars, vectors, bivectors and trivectors parts in the zeroeth order case, we find

$$
\begin{aligned}
\nabla \cdot D_0 &= \rho_0 & \text{(scalar)}, \\
-\nabla \times H_0 &= -\mathbf{J_0} & \text{(vector)}, \\
\nabla \times D_0 &= 0 & \text{(bivector)}, \\
\nabla \cdot H_0 &= 0 & \text{(trivector)},
\end{aligned}
$$

the expected zeroeth order equations. The magnetic component of force is much smaller than the electric component, and hence we can write $\mathbf{J} = \sigma\mathbf{E}$. Hence for the case with steady currents, inspecting the vector equation, we form a link between H_0 and E_0. The first order equations are

$$
\begin{aligned}
\nabla \cdot D_1 &= \rho_1 & \text{(scalar)}, \\
\frac{\partial \mathbf{D_0}}{dt} - \nabla \times H_1 &= -\mathbf{J_1} & \text{(vector)}, \\
\frac{\partial \mathbf{H_0}}{cdt} + \nabla \times D_1 &= 0 & \text{(bivector)}, \\
i\nabla \cdot H_1 &= 0 & \text{(trivector)},
\end{aligned}
$$

in agreement with the quasi-static expansion in Chua (1971).

References

ABDALLA-H., AND PICKETT-M. D. (2011). SPICE modeling of memristors, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1832–1835.

AHN-S.-E., LEE-M.-J., PARK-Y., KANG-B. S., LEE-C. B., KIM-K. H., SEO-S., SUH-D.-S., KIM-D.-C., HUR-J., XIANYU-W., STEFANOVICH-G., YIN-H., YOO-I.-K., LEE-J.-H., PARK-J.-B., BAEK-I.-G., AND PAR-B. H. (2008). Write current reduction in transition metal oxide based resistance change memory, *Advanced Materials*, **20**(5), pp. 924–928.

AKINAGA-H., AND SHIMA-H. (2010). Resistive random access memory (ReRAM) based on metal oxides, *Proceedings of the IEEE*, **98**(12), pp. 2237–2251.

AL-SARAWI-S. (2002). Low power Schmitt trigger circuit, *Electronics Letters*, **38**(18), pp. 1009–1010.

AL-SARAWI-S., ABBOTT-D., AND FRANZON-P. (1998). A review of 3-D packaging technology, *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging*, **21**(1), pp. 2–14.

ALTED-F. (2010). Why modern CPUs are starving and what can be done about it, *Computing in Science & Engineering*, **12**(2), pp. 68–71.

AMSINCK-C. J., SPIGNA-N. H. D., NACKASHI-D. P., AND FRANZON-P. D. (2005). Scaling constraints in nanoelectronic random-access memories, *Nanotechnology*, **16**(10), pp. 2251–2260.

BAHAR-R., HAMMERSTROM-D., HARLOW-J., JOYNER JR-W., LAU-C., MARCULESCU-D., ORAILOGLU-A., AND PEDRAM-M. (2007). Architectures for silicon nanoelectronics and beyond, *Computer*, **40**(1), pp. 25–33.

BECK-A., BEDNORZ-J. G., GERBER-C., ROSSEL-C., AND WIDMER-D. (2000). Reproducible switching effect in thin oxide films for memory applications, *Applied Physics Letters*, **77**(1).

BENDERLI-S., AND WEY-T. A. (2009). On SPICE macromodelling of TiO$_2$ memristors, *Electronics Letters*, **45**(7), pp. 377–379.

BERMAK-A., AND YUNG-Y. (2006). A DPS array with programmable resolution and reconfigurable conversion time, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **14**(1), pp. 15–22.

BERMAK-A., BOUZERDOUM-A., AND ESHRAGHIAN-K. (2002). A vision sensor with on-pixel ADC and in-built light adaptation mechanism, *Microelectronics Journal*, **33**(12), pp. 1091–1096.

BICKERSTAFF-K., AND SWARTZLANDER-E. (2011). Memristor-based arithmetic, *Asilomar Conference on Signals, Systems and Computers, ASILOMAR*, pp. 1173–1177.

BIOLEK-D., BIOLEK-Z., AND BIOLKOVA-V. (2009a). SPICE modeling of memristive, memcapacitative and meminductive systems, *European Conference on Circuit Theory and Design, ECCTD*, pp. 249–252.

References

BIOLEK-D., BIOLEK-Z., AND BIOLKOVA-V. (2011). PSPICE modeling of meminductor, *International Journal of Analog Integrated Circuits and Signal Processing*, **66**, pp. 129–137.

BIOLEK-Z., BIOLEK-D., AND BIOLKOVÁ-V. (2009b). SPICE model of memristor with nonlinear dopant drift, *Radioengineering*, **18**(2), pp. 210–214.

BLANC-J., AND STAEBLER-D. L. (1971). Electrocoloration in SrTiO$_3$: Vacancy drift and oxidation-reduction of transition metals, *Phys. Rev. B*, **4**(10), pp. 3548–3557.

BORGHETTI-J., SNIDER-G., KUEKES-P., YANG-J., STEWART-D., AND WILLIAMS-R. (2010). 'Memristive' switches enable 'stateful' logic operations via material implication, *Nature*, **464**(7290), pp. 873–876.

BORGHETTI-J., STRUKOV-D., PICKETT-M., YANG-J., STEWART-D., AND WILLIAMS-R. (2009). Electrical transport and thermometry of electroformed titanium dioxide memristive switches, *Journal of Applied Physics*, **106**(12). art no. 124504.

BUOT-F. A., AND RAJAGOPAL-A. K. (1994). Binary information storage at zero bias in quantum-well diodes, *Journal of Applied Physics*, **76**(9), pp. 5552–5560.

BUSCARINO-A., FORTUNA-L., FRASCA-M., GAMBUZZA-L., AND SCIUTO-G. (2011). A new cellular nonlinear network-based memristive chaotic circuit, *10$^\text{th}$ International Symposium on Signals, Circuits and Systems (ISSCS)*, pp. 1–4.

CHANG-T., JO-S.-H., AND LU-W. (2011). Short-term memory to long-term memory transition in a nanoscale memristor, *ACS Nano*, **5**(9), pp. 7669–7676.

CHEN-Y., AND WANG-X. (2009). Compact modeling and corner analysis of spintronic memristor, *Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 7–12.

CHEN-Y., LI-H., CHEN-Y., AND PINO-R. (2011). 3D-ICML: A 3D bipolar ReRAM design with interleaved complementary memory layers, *Design, Automation & Test in Europe Conference & Exhibition, DATE*, pp. 1–4.

CHOI-B., JEONG-D., KIM-S., ROHDE-C., CHOI-S., OH-J., KIM-H., HWANG-C., SZOT-K., WASER-R., REICHENBERG-B., AND TIEDKE-S. (2005). Resistive switching mechanism of TiO$_2$ thin films grown by atomic-layer deposition, *Journal of Applied Physics*, **98**. art no. 033715.

CHOI-H., JUNG-H., LEE-J., YOON-J., PARK-J., SEONG-D.-J., LEE-W., HASAN-M., JUNG-G., AND HWANG-H. (2009). An electrically modifiable synapse array of resistive switching memory, *Nanotechnology*, **20**(34). art no. 345201.

CHUA-L. (1969). *Introduction to Nonlinear Network Theory*, Vol. 43, McGraw-Hill, chapter 5.

CHUA-L. (2003). Nonlinear circuit foundations for nanodevices. I. The four-element torus, *Proceedings of the IEEE*, **91**(11), pp. 1830–1859.

CHUA-L. (2011). Resistance switching memories are memristors, *Applied Physics A: Materials Science & Processing*, **102**(4), pp. 765–783.

CHUA-L. O. (1968). Synthesis of new nonlinear network elements, *Proceedings of the IEEE*, **56**(8), pp. 1325–1340.

CHUA-L. O. (1971). Memristor – the missing circuit element, *IEEE Transactions on Circuit Theory*, **18**(5), pp. 507–519.

CHUA-L. O., AND KANG-S. M. (1976). Memristive devices and systems, *Proceedings of the IEEE*, **64**(2), pp. 209–223.

DELBRIDGE-A. (2001). *The Macquarie Dictionary*, 3rd edn, The Macquarie Library, North Ryde, NSW, Australia.

DELGADO-A. (2009). Input-output linearization of memristive systems, *IEEE Nanotechnology Materials and Devices Conference, NMDC*, pp. 154–157.

DORAN-C. J. L., DORAN-C., AND LASENBY-A. N. (2003). *Geometric Algebra for Physicists*, Cambridge University Press, chapter 2.

DRISCOLL-T., KIM-H. T., CHAE-B. G., DI VENTRA-M., AND BASOV-D. N. (2009). Phase-transition driven memristive system, *Applied Physics Letters*, **95**(4). art no. 043503.

EBONG-I., AND MAZUMDER-P. (2011a). Self-controlled writing and erasing in a memristor crossbar memory, *IEEE Transactions on Nanotechnology*, **10**(6), pp. 1454–1463.

EBONG-I. E., AND MAZUMDER-P. (2011b). CMOS and memristor-based neural network design for position detection, *Proceedings of the IEEE*, . (In press).

ESHRAGHIAN-K., CHO-K.-R., KAVEHEI-O., KANG-S.-K., ABBOTT-D., AND KANG-S.-M. S. (2011a). Memristor mos content addressable memory (MCAM): Hybrid architecture for future high performance search engines, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **19**(8), pp. 1407–1417.

ESHRAGHIAN-K., KAVEHEI-O., CHO-K., CHAPPELL-J., IQBAL-A., AL-SARAWI-S., AND ABBOTT-D. (2011b). Memristive device fundamentals and modeling: Applications to circuits and systems simulation, *Proceedings of the IEEE*, . (Invited, in process).

FANO-R., CHU-L., AND ADLER-R. (1968). *Electromagnetic Fields, Energy, and Forces*, MIT Press, chapter 6.

FLOCKE-A., AND NOLL-T. G. (2007). Fundamental analysis of resistive nano-crossbars for the use in hybrid Nano/CMOS-memory, *European Solid State Circuits Conference, ESSCIRC*, pp. 328–331.

FLOCKE-A., NOLL-T. G., KÜGELER-C., NAUENHEIM-C., AND WASER-R. (2008). A fundamental analysis of nano-crossbars with non-linear switching materials and its impact on TiO_2 as a resistive layer, *IEEE Conference on Nanotechnology, NANO*, pp. 319–322.

FREITAS-R. (2008). Storage class memory and the data center of the future, *The Future of Data Centers-GSRC Workshop*, Vol. 4.

GAO-B., ZHANG-H., YU-S., SUN-B., LIU-L., LIU-X., WANG-Y., HAN-R., KANG-J., YU-B., AND WAN-Y. (2009). Oxide-based RRAM: Uniformity improvement using a new material-oriented methodology, *Symposium on VLSI Technology*, pp. 30–31.

GEORGIOU-P. S., BARAHONA-M., YALIRAKI-S. N., AND DRAKAKIS-E. M. (2011). Device properties of Bernoulli memristors, *Proceedings of the IEEE*, . (In press).

References

GERGEL-HACKETT-N., HAMADANI-B., DUNLAP-B., SUEHLE-J., RICHTER-C., HACKER-C., AND GUNDLACH-D. (2009). A flexible solution-processed memristor, *IEEE Electron Device Letters*, **30**(7), pp. 706–708.

GERGEL-HACKETT-N., TEDESCO-J. L., AND RICHTER-C. A. (2011). Memristors with flexible electronic applications, *Proceedings of the IEEE*, . (In press).

GIBBONS-J., AND BEADLE-W. (1964). Switching properties of thin NiO films, *Solid State Electronics*, **7**, pp. 785–797.

GRIFFITHS-D., AND INGLEFIELD-C. (1999). *Introduction to Electrodynamics*, Prentice Hall, chapter 2.

GUANRONG-X. (2010). *Memristor Micro-Devices Fabrication and I-V Characterisation of the Fourth Circuit Element*, Master thesis, RMIT University, Melbourne, Australia.

HAMMERSTROM-D., AND ZAVERI-M. S. (2010). CMOL/CMOS implementations of Bayesian inference engine: Digital and mixed-signal architectures and performance/price a hardware design space exploration, *CMOS Processors and Memories, Part 1, Editor: Iniewski, Krzysztof*, Analog Circuits and Signal Processing, Springer Netherlands, pp. 97–138.

HAN-J. (2004). *Fault-Tolerant Architectures for Nanoelectronic and Quantum Devices*, Doctoral dissertation in Applied Sciences, Delft University of Technology, Netherlands.

HANSON-S., FOO-Z., BLAAUW-D., AND SYLVESTER-D. (2010). A 0.5 V sub-microwatt CMOS image sensor with pulse-width modulation read-out, *IEEE Journal of Solid-State Circuits*, **45**(4), pp. 759–767.

HASEGAWA-T., OHNO-T., TERABE-K., TSURUOKA-T., NAKAYAMA-T., GIMZEWSKI-J. K., AND AONO-M. (2010). Learning abilities achieved by a single solid-state atomic switch, *Advanced Materials*, **22**(16), pp. 1831–1834.

HAYASHI-Y. (1980). Switching phenomena in thin-insulator metal-insulator-semiconductor diodes, *Applied Physics Letters*, **37**(4), pp. 407–408.

HEUER-A., MURUGAVEL-S., AND ROLING-B. (2005). Nonlinear ionic conductivity of thin solid electrolyte samples: Comparison between theory and experiment, *Physical Review B*, **72**(17). art no. 174304.

HINCKLEY-S., JANSZ-P., GLUSZAK-E., AND ESHRAGHIAN-K. (2002). Modelling of device structure effects on electrical crosstalk in back illuminated CMOS compatible photodiodes, *Conference on Optoelectronic and Microelectronic Materials and Devices*, pp. 397–400.

HUBEL-D., AND WIESEL-T. (1959). Receptive fields of single neurones in the cat's striate cortex, *Journal of physiology*, **148**(3), p. 574.

HU-M., LI-H., CHEN-Y., WANG-X., AND PINO-R. E. (2011). Geometry variations analysis of TiO_2 thin-film and spintronic memristors, *Proceedings of the 16th Asia and South Pacific Design Automation Conference, ASPDAC*, pp. 25–30.

IELMINI-D., NARDI-F., AND CAGLI-C. (2011). Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories, *Nanotechnology*, **22**(25). art no. 254022.

IGNATIEV-A., WU-N. J., CHEN-X., NIAN-Y. B., PAPAGIANNI-C., LIU-S. Q., AND STROZIER-J. (2008). Resistance switching in oxide thin films, *Phase Transitions*, **7**(8), pp. 791–806.

INDIVERI-G., LINARES-BARRANCO-B., HAMILTON-T. J., VAN SCHAIK-A., ETIENNE-CUMMINGS-R., DELBRUCK-T., LIU-S.-C., DUDEK-P., HÄFLIGER-P., RENAUD-S., SCHEMMEL-J., CAUWENBERGHS-G., ARTHUR-J., HYNNA-K., FOLOWOSELE-F., SAIGHI-S., SERRANO-GOTARREDONA-T., WIJEKOON-J., WANG-Y., AND BOAHEN-K. (2011). Neuromorphic silicon neuron circuits, *Frontiers in Neuroscience*, **5**. *http://tinyurl.com/neurosi*.

INOUE-I., ROZENBERG-M., YASUDA-S., SANCHEZ-M., YAMAZAKI-M., MANAGO-T., AKINAGA-H., TAKAGI-H., AKOH-H., AND TOKURA-Y. (2005). Strong electron correlation effects in non-volatile electronic memory devices, *Non-Volatile Memory Technology Symposium*, pp. 131–136.

ITOH-M., AND CHUA-L. O. (2008). Memristor oscillators, *International Journal of Bifurcation and Chaos, IJBC*, **18**(11), pp. 3183–3206.

ITRS (2009). International Technology Roadmap for Semiconductors, Emerging Research Devices.

JELTSEMA-D., AND DO ANDRIA CEREZO-A. (2011). Port-Hamiltonian formulation of systems with memory, *Proceedings of the IEEE*, . (In press).

JOGLEKAR-Y. N., AND WOLF-S. J. (2009). The elusive memristor: properties of basic electrical circuits, *European Journal of Physics*, **30**(4), p. 661.

JONES-R. (2009). Computing with molecules, *Nature Nanotechnology*, **4**(4), p. 207.

JO-S. H., CHANG-T., EBONG-I., BHADVIYA-B. B., MAZUMDER-P., AND LU-W. (2010). Nanoscale memristor device as synapse in neuromorphic systems, *Nano Letters*, **10**(4), pp. 1297–1301.

JOSHUA YANG-J., MIAO-F., PICKETT-M., OHLBERG-D., STEWART-D., LAU-C., AND WILLIAMS-R. (2009). The mechanism of electroforming of metal oxide memristive switches, *Nanotechnology*, **20**. art no. 215201.

KAGAWA-K., YOSHIDA-N., TOKUDA-T., OHTA-J., AND NUNOSHITA-M. (2004). Building a simple model of a pulse-frequency-modulation photosensor and demonstration of a 128×128-pixel pulse-frequency-modulation image sensor fabricated in a standard 0.35-μm complementary metal-oxide semiconductor technology, *Optical Review*, **11**(3), pp. 176–181.

KALININ-S., YANG-J., AND DEMMING-A. (2011). Non-volatile memory based on nanostructures, *Nanotechnology*, **22**. art no. 250201.

KANG-S. M. (1975). *On The Modeling of Some Classes of Nonlinear Devices and Systems*, Doctoral dissertation in Electrical and Electronics Engineering, 76-15-251, University of California, Berkeley, CA.

KAVEHEI-O., AL-SARAWI-S., CHO-K., ESHRAGHIAN-K., AND ABBOTT-D. (2011a). An analytical approach for memristive nanoarchitectures, *IEEE Transactions on Nanotechnology*, . Arxiv preprint arXiv:1106.2927.

References

KAVEHEI-O., AL-SARAWI-S., CHO-K., IANNELLA-N., KIM-S., ESHRAGHIAN-K., AND ABBOTT-D. (2011b). Memristor-based synaptic networks and logical operations using in-situ computing, *International Conference Series on Intelligent Sensors, Sensor Networks and Information Processing, ISSNIP*. Arxiv preprint arXiv:1108.4182.

KAVEHEI-O., AL-SARAWI-S., SRIRAM-S., BHASKARAN-M., CHO-K., ESHRAGHIAN-K., AND ABBOTT-D. (2011c). Non-volatile complementary resistive switch-based content addressable memory, , . Arxiv preprint arXiv:1108.3716.

KAVEHEI-O., CHO-K., LEE-S., KIM-S., AL-SARAWI-S., ABBOTT-D., AND ESHRAGHIAN-K. (2011d). Fabrication and modeling of Ag/TiO$_2$/ITO memristor, *54th IEEE International Midwest Symposium on Circuits and Systems, MWSCAS*, pp. 1–4.

KAVEHEI-O., IQBAL-A., KIM-Y. S., ESHRAGHIAN-K., AL-SARAWI-S. F., AND ABBOTT-D. (2010). The fourth element: characteristics, modelling and electromagnetic theory of the memristor, *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Science*, **466**(2120), pp. 2175–2202.

KAVEHEI-O., KIM-Y., IQBAL-A., ESHRAGHIAN-K., AL-SARAWI-S., AND ABBOTT-D. (2009). The fourth element: Insights into the memristor, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 921–927.

KIM-H., SAH-M. P., YANG-C., ROSKA-T., AND CHUA-L. O. (2011a). Memristor bridge synapses, *Proceedings of the IEEE*, . (In press).

KIM-K. H., KANG-B. S., LEE-M. J., AHN-S. E., LEE-C. B., STEFANOVICH-G., XIANYU-W. X., KIM-C. J., AND PARK-Y. (2009a). Multilevel programmable oxide diode for cross-point memory by electrical-pulse-induced resistance change, *IEEE Electron Device Letters*, **30**(10), pp. 1036–1038.

KIM-K., KIM-G., SONG-S., SEOK-J., LEE-M., YOON-J., AND HWANG-C. (2010). Electrically configurable electroforming and bipolar resistive switching in Pt/TiO$_2$/Pt structures, *Nanotechnology*, **21**. art no. 305203.

KIM-K. M., JEONG-D. S., AND HWANG-C. S. (2011b). Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook, *Nanotechnology*, **22**(25). art no. 254002.

KIM-K., SHIN-S., AND KANG-S.-M. (2011c). Stateful logic pipeline architecture, *IEEE International Symposium on Circuits and Systems, ISCAS*, pp. 2497–2500.

KIM-S., BIJU-K., JO-M., JUNG-S., PARK-J., LEE-J., LEE-W., SHIN-J., PARK-S., AND HWANG-H. (2011d). Effect of scaling WO$_x$-based RRAMs on their resistive switching characteristics, *IEEE Electron Device Letters*, (99), pp. 1–3.

KIM-T., JANG-E., LEE-N., CHOI-D., LEE-K., JANG-J., CHOI-J., MOON-S., AND CHEON-J. (2009b). Nanoparticle assemblies as memristors, *Nano letters*, **9**(6), pp. 2229–2233.

KIM-W.-G., AND RHEE-S.-W. (2010). Effect of the top electrode material on the resistive switching of TiO$_2$ thin film, *Microelectronic Engineering*, **87**, pp. 98–103.

KIM-Y., AHN-H., KIM-S., AND JEONG-D. (2009c). A high-speed range-matching TCAM for storage-efficient packet classification, *IEEE Transactions on Circuits and Systems I: Regular Papers*, **56**(6), pp. 1221–1230.

KOPPA-S., JOO-Y., VENKATARAMASUBRAMANI-M., AND TANG-L. (2010). Nanoscale biosensor chip, *53*rd *IEEE International Midwest Symposium on Circuits and Systems, MWSCAS*, pp. 268–271.

KRIEGER-J. H., TRUBIN-S. V., VASCHENKO-S. B., AND YUDANOV-N. F. (2001). Molecular analogue memory cell based on electrical switching and memory in molecular thin films, *Synthetic Metals*, **122**(1), pp. 199–202.

KROEMER-H. (2001). Nobel lecture: Quasielectric fields and band offsets, teaching electrons new tricks, *Reviews of Modern Physics*, **73**(3), pp. 783–793.

KRZYSTECZKO-P., MUNCHENBERGER-J., SCHAFERS-M., REISS-G., AND THOMAS-A. (2012). The memristive magnetic tunnel junction as a nanoscopic synapse-neuron system, *Advanced Materials*, . (In press).

KUEKES-P., STEWART-D., AND WILLIAMS-R. (2005). The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits, *Journal of Applied Physics*, **97**(3). art no. 034301.

KUMAKI-T., KURODA-Y., ISHIZAKI-M., KOIDE-T., MATTAUSCH-H., NODA-H., DOSAKA-K., ARIMOTO-K., AND SAITO-K. (2007). Real-time Huffman encoder with pipelined CAM-based data path and code-word-table optimizer, *IEICE - Transactions on Information and Systems*, **E90-D**(1), pp. 334–345.

KVATINSKY-S., FRIEDMAN-E., KOLODNY-A., AND WEISER-U. (2011). Memristor-based IMPLY logic design flow, *IEEE International Conference of Computer Design, ICCD*, pp. 142–147.

KWON-D., KIM-K., JANG-J., JEON-J., LEE-M., KIM-G., LI-X., PARK-G., LEE-B., HAN-S., KIM-M., AND HWANG-C. (2010). Atomic structure of conducting nanofilaments in TiO_2 resistive switching memory, *Nature Nanotechnology*, **5**(2), pp. 148–153.

LAI-C., KING-Y., AND HUANG-S. (2006). A 1.2-V 0.25-μm clock output pixel architecture with wide dynamic range and self-offset cancellation, *IEEE Sensors Journal*, **6**(2), pp. 398–405.

LAM-Y. (1972). Formulation of normal form equations of nonlinear networks containing memristors and coupled elements, *IEEE Transactions on Circuit Theory*, **19**(6), pp. 585–594.

LEE-K.-J., CHO-B.-H., CHO-W.-Y., KANG-S., CHOI-B.-G., OH-H.-R., LEE-C.-S., KIM-H.-J., PARK-J.-M., WANG-Q., PARK-M.-H., RO-Y.-H., CHOI-J.-Y., KIM-K.-S., KIM-Y.-R., SHIN-I.-C., LIM-K.-W., CHO-H.-K., CHOI-C.-H., CHUNG-W.-R., KIM-D.-E., YOON-Y.-J., YU-K.-S., JEONG-G.-T., JEONG-H.-S., KWAK-C.-K., KIM-C.-H., AND KIM-K. (2008). A 90 nm 1.8 V 512 Mb diode-switch pram with 266 Mb/s read throughput, *IEEE Journal of Solid-State Circuits*, **43**(1), pp. 150–162.

LEE-S., KAVEHEI-O., HONG-Y., CHO-T., YOU-Y., CHO-K., AND ESHRAGHIAN-K. (2010). 3-D system-on-system (SoS) biomedical-imaging architecture for health-care applications, *IEEE Transactions on Biomedical Circuits and Systems*, **4**(6), pp. 426–436.

References

LEHTONEN-E., AND LAIHO-M. (2010). CNN using memristors for neighborhood connections, *12*th *International Workshop on Cellular Nanoscale Networks and Their Applications, (CNNA)*, pp. 1–4.

LEHTONEN-E., POIKONEN-J., AND LAIHO-M. (2010). Two memristors suffice to compute all Boolean functions, *Electronics Letters*, **46**(3), pp. 239–240.

LEWIS-D. L., AND LEE-H. H. S. (2009). Architectural evaluation of 3D stacked RRAM caches, *IEEE International Conference on 3D System Integration, 3DIC*, pp. 1–4.

LIANG-J., AND WONG-H. (2010). Cross-point memory array without cell selectors-device characteristics and data storage pattern dependencies, *IEEE Transactions on Electron Devices*, **57**(10), pp. 2531–2538.

LI-C., WEI-M., AND YU-J. (2009). Chaos generator based on a PWL memristor, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 944–947.

LI-H., AND CHEN-Y. (2010). Emerging non-volatile memory technologies: From materials, to device, circuit, and architecture, *53*rd *IEEE International Midwest Symposium on Circuits and Systems, MWSCAS*, pp. 1–4.

LIKHAREV-K., AND STRUKOV-D. (2005). CMOL: Devices, circuits, and architectures, *Introducing Molecular Electronics*, pp. 447–477.

LINARES-BARRANCO-B., AND SERRANO-GOTARREDONA-T. (2009). Memristance can explain spike-time-dependent-plasticity in neural synapses, *Nature Precedings*, p. npre.2009.3010.1.

LINN-E., ROSEZIN-R., KÜGELER-C., AND WASER-R. (2010). Complementary resistive switches for passive nanocrossbar memories, *Nature Materials*, **9**(5), pp. 403–406.

LIN-Z. H., AND WANG-H. X. (2009). Image encryption based on chaos with PWL memristor in Chua's circuit, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 964–968.

LIU-S., WU-N., IGNATIEV-A., AND LI-J. (2006). Electric-pulse-induced capacitance change effect in perovskite oxide thin films, *Journal of Applied Physics*, **100**(5), pp. 1–3.

LU-S. K., AND HSU-C. H. (2006). Fault tolerance techniques for high capacity RAM, *IEEE Transactions on Reliability*, **55**(2), pp. 293–306.

MALLÉGOL-S. (2003). *Caractérisation et Application de Matériaux Composites Nanostructurés á la Réalisation de Dispositifs Hyperfréquences Non Réciproques*, Doctoral dissertation in Electronic, (in French), Université de Bretagne Occidentale, France.

MEDEIROS-RIBEIRO-G., PERNER-F., CARTER-R., ABDALLA-H., PICKETT-M. D., AND WILLIAMS-R. S. (2011). Lognormal switching times for titanium dioxide bipolar memristors: origin and resolution, *Nanotechnology*, **22**. art no. 095702.

MIAO-F., YANG-J. J., BORGHETTI-J., MEDEIROS-RIBEIRO-G., AND WILLIAMS-R. S. (2011). Observation of two resistance switching modes in TiO_2 memristive devices electroformed at low current, *Nanotechnology*, **22**(25). art no. 254007.

MIAO-F., YANG-J. J., STRACHAN-J. P., STEWART-D., WILLIAMS-R. S., AND LAU-C. N. (2009). Force modulation of tunnel gaps in metal oxide memristive nanoswitches, *Applied Physics Letters*, **95**(11). art no. 113503.

MOHAN-N., AND SACHDEV-M. (2009). Low-leakage storage cells for ternary content addressable memories, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **17**(5), pp. 604–612.

MOHR-P. J., AND TAYLOR-B. N. (2005). CODATA recommended values of the fundamental physical constants: 2002, *Reviews of Modern Physics*, **77**(1), pp. 1–107.

MOTT-N., AND GURNEY-R. (1964). *Electronic Processes in Ionic Crystals*, Dover, chapter 2.

MOUTTET-B. (2009). Proposal for memristors in signal processing, *Nano-Net*, pp. 11–13.

MOUTTET-B. (2010). The business landscape for mem-resistor electronics. *http://tinyurl.com/blaisemouttet1* (visited on 3/9/2011).

OHNO-T., HASEGAWA-T., TSURUOKA-T., TERABE-K., GIMZEWSKI-J., AND AONO-M. (2011). Short-term plasticity and long-term potentiation mimicked in single inorganic synapses, *Nature Materials*, **10**, pp. 591–595.

OHTA-J., UEHARA-A., TOKUDA-T., AND NUNOSHITA-M. (2000). Pulse-modulated vision chips with versatile-interconnected pixels, *in* J. H. G. Goos., and J. van Leeuwen. (eds.), *Parallel and Distributed Processing*, Vol. 1800 of *Lecture Notes in Computer Science*, pp. 1063–1071.

OSTER-G. (1974). A note on memristors, *IEEE Transactions on Circuits and Systems*, **21**(1), pp. 152–152.

OVSHINSKY-S. (2011). New transformative possibilities for ovonic devices, *the European Symposium on Phase Change and Ovonic Science, E*PCOS*, pp. 321–324. *http://tinyurl.com/a01ovshinsky* (visited on 4/8/2011).

PAGIAMTZIS-K., AND SHEIKHOLESLAMI-A. (2006). Content-addressable memory (CAM) circuits and architectures: A tutorial and survey, *IEEE Journal of Solid-State Circuits*, **41**(3), pp. 712–727.

PARK-D., JOO-Y., AND KOPPA-S. (2010). A simple and robust self-reset CMOS image sensor, *53*rd *IEEE International Midwest Symposium on Circuits and Systems, MWSCAS*, pp. 680–683.

PARK-S., JUNG-S., SIDDIK-M., JO-M., LEE-J., PARK-J., LEE-W., KIM-S., SADAF-S. M., LIU-X., AND HWANG-H. (2011). Memristive switching behavior in $Pr_{0.7}Ca_{0.3}MnO_3$ by incorporating an oxygen-deficient layer, *Physica Status Solidi (RRL) Rapid Research Letters*, **5**(10–11), pp. 409–411.

PERSHIN-Y., AND DI VENTRA-M. (2010). Practical approach to programmable analog circuits with memristors, *IEEE Transactions on Circuits and Systems I: Regular Papers*, **57**(8), pp. 1857–1864.

PERSHIN-Y., AND DI VENTRA-M. (2011). Memory effects in complex materials and nanoscale systems, *Advances in Physics*, **60**(2), pp. 145–227.

PERSHIN-Y. V., FONTAINE-S. L., AND VENTRA-M. D. (2009). Memristive model of amoeba learning, *Phys. Rev. E*, **80**(2). art no. 021926.

PICKETT-M. D., STRUKOV-D. B., BORGHETTI-J. L., YANG-J. J., SNIDER-G. S., STEWART-D. R., AND WILLIAMS-R. S. (2009). Switching dynamics in titanium dioxide memristive devices, *Journal of Applied Physics*, **106**(7). art no. 074508.

References

PORAT-M., AND ZEEVI-Y. (1988). The generalized Gabor scheme of image representation in biological and machine vision, *IEEE Transactions on Pattern Analysis and Machine Intelligence*, **10**(4), pp. 452–468.

POTLAPALLI-H., AND LUO-R. (1998). Fractal-based classification of natural textures, *IEEE Transactions on Industrial Electronics*, **45**(1), pp. 142–150.

PRODROMAKIS-T., PEH-B. P., PAPAVASSILIOU-C., AND TOUMAZOU-C. (2011). A versatile memristor model with nonlinear dopant kinetics, *IEEE Transactions on Electron Devices*, **58**(9), pp. 3099–3105.

QURESHI-M. S., PICKETT-M., MIAO-F., AND STRACHAN-J. P. (2011). CMOS interface circuits for reading and writing memristor crossbar array, *IEEE International Symposium on Circuits and Systems, ISCAS*, pp. 2954–2957.

RAGHAVAN-N., PEY-K., LI-X., LIU-W., WU-X., BOSMAN-M., AND KAUERAUF-T. (2011). Very low reset current for an RRAM device achieved in the oxygen-vacancy-controlled regime, *IEEE Electron Device Letters*, **32**(6), pp. 716–718.

RAJA-T., AND MOURAD-S. (2009). Digital logic implementation in memristor-based crossbars, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 939–943.

ROBERTS-D. (2011). *Efficient Data Center Architectures Using Non-Volatile Memory and Reliability Techniques*, Doctoral dissertation in Computer Science and Engineering, The University of Michigan, Ann Arbor, MI.

ROSE-G., AND MANEM-H. (2010). A Hybrid CMOS-Nano FPGA based on majority logic: From devices to architecture, *CMOS Processors and Memories*, pp. 139–161.

ROSE-G. S., RAJENDRAN-J., MANEM-H., KARRI-R., AND PINO-R. E. (2011). Leveraging memristive systems in the construction of digital logic circuits, *Proceedings of the IEEE*, . (In press).

ROSEZIN-R., LINN-E., KÜGELER-C., BRUCHHAUS-R., AND WASER-R. (2011). Crossbar logic using bipolar and complementary resistive switches, *IEEE Electron Device Letters*, **32**(6), pp. 710 –712.

RUDOLPH-D., SINCLAIR-P., AND COGGINS-J. (1998). Automatic computerized radiographic identification of cephalometric landmarks, *American Journal of Orthodontics and Dentofacial Orthopedics*, **113**(2), pp. 173–179.

RUSSO-U., IELMINI-D., CAGLI-C., AND LACAITA-A. (2009). Filament conduction and reset mechanism in NiO-based resistive-switching memory (RRAM) devices, *IEEE Transactions on Electron Devices*, **56**(2), pp. 186–192.

RUSSO-U., IELMINI-D., CAGLI-C., LACAITA-A., SPIGA-S., WIEMER-C., PEREGO-M., AND FANCIULLI-M. (2007). Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM, *IEEE International Electron Devices Meeting, IEDM*, pp. 775–778.

SACCHETTO-D., DE MICHELI-G., AND LEBLEBICI-Y. (2011). Multiterminal memristive nanowire devices for logic and memory applications: A review, *Proceedings of the IEEE*, . (In press).

SEKAR-D. (2010). Resistive RAM: Technology and market opportunities. *http://tinyurl.com/2010novsekarrram* (visited on 15/3/2011).

SEO-K., KIM-I., JUNG-S., JO-M., PARK-S., PARK-J., SHIN-J., BIJU-K. P., KONG-J., LEE-K., LEE-B., AND HWANG-H. (2011). Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device, *Nanotechnology*, **22**. art no. 254023.

SHIBATA-T. (2009). Computing based on the physics of nano devices–a beyond-CMOS approach to human-like intelligent systems, *Solid-State Electronics*, **53**(12), pp. 1227–1241.

SHIN-J., KIM-I., BIJU-K. P., JO-M., PARK-J., LEE-J., JUNG-S., LEE-W., KIM-S., PARK-S., AND HWANG-H. (2011a). TiO_2-based metal-insulator-metal selection device for bipolar resistive random access memory cross-point application, *Journal of Applied Physics*, **109**(3). art no. 033712.

SHIN-S., KIM-K., AND KANG-S. (2010). Compact models for memristors based on charge-flux constitutive relationships, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **29**(4), pp. 590–598.

SHIN-S., KIM-K., AND KANG-S. (2011b). Complementary structure of memristive devices based passive memory arrays, *IEEE International Symposium on Circuits and Systems, ISCAS*, pp. 321–324.

SHIN-S., KIM-K., AND KANG-S.-M. (2009). Memristor-based fine resolution programmable resistance and its applications, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 948–951.

SHKABKO-A., AGUIRRE-M. H., HUG-P., WEIDENKAFF-A., MAROZAU-I., AND LIPPERT-T. (2010). The effects of switching time and $SrTiO_{3-x}N_y$ nanostructures on the operation of $Al/SrTiO_{3-x}N_y/Al$ memristors, *IOP Conference Series: Materials Science and Engineering*, **8**(1). art no. 074508.

SHOUSHUN-C., BOUSSAID-F., AND BERMAK-A. (2008). Robust intermediate read-out for deep submicron technology CMOS image sensors, *IEEE Sensors Journal*, **8**(3), pp. 286–294.

SIMMONS-J. G. (1963). Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film, *Journal of Applied Physics*, **34**(6), pp. 1793–1803.

SKLYAR-R. (2009). Analytical treatment of the signal propagation in an EM transistor/memristor (EMTM), *International Workshop on Nonlinear Dynamics and Synchronization, INDS*, pp. 116–120.

SNIDER-G. (2011). Instar and outstar learning with memristive nanodevices, *Nanotechnology*, **22**. art no. 015201.

SNIDER-G., AMERSON-R., CARTER-D., ABDALLA-H., QURESHI-M., LE ANDVEILLE AND-J., VERSACE-M., AMES-H., PATRICK-S., CHANDLER-B., GORCHETCHNIKOV-A., AND MINGOLLA-E. (2011). From synapses to circuitry: Using memristive memory to explore the electronic brain, *Computer*, **44**(2), pp. 21–28.

SNIDER-G. S. (2008a). Cortical computing with memristive nanodevices, *SciDAC Review*, **10**, pp. 58–65.

SNIDER-G. S. (2008b). Spike-timing-dependent learning in memristive nanodevices, *IEEE International Symposium on Nanoscale Architectures*, pp. 85–92.

SONG-S., MILLER-K., AND ABBOTT-L. (2000). Competitive Hebbian learning through spike-timing-dependent synaptic plasticity, *Nature Neuroscience*, **3**, pp. 919–926.

References

STANDARDS AUSTRALIA COMMITTEE ME/71, QUANTITIES, UNITS AND CONVERSIONS. (1998). *AS ISO 1000—1998: The international system of units (SI) and its application*, Australian Standard.

STEWART-D. R., OHLBERG-D. A. A., BECK-P. A., CHEN-Y., WILLIAMS-R. S., JEPPESEN-J. O., NIELSEN-K. A., AND STODDART-J. F. (2004). Molecule-independent electrical switching in Pt/Organic Monolayer/Ti devices, *Nano Letters*, **4**(1), pp. 133–136.

STRACHAN-J. P., STRUKOV-D. B., BORGHETTI-J., YANG-J. J., MEDEIROS-RIBEIRO-G., AND WILLIAMS-R. S. (2011). The switching location of a bipolar memristor: chemical, thermal and structural mapping, *Nanotechnology*, **22**(25). art no. 254015.

STRUKOV-D. (2011). Nanotechnology: Smart connections, *Nature*, **476**(7361), pp. 403–405.

STRUKOV-D., AND LIKHAREV-K. (2005). CMOL FPGA: a reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices, *Nanotechnology*, **16**(6), pp. 888–900.

STRUKOV-D., AND LIKHAREV-K. (2007). Defect-tolerant architectures for nanoelectronic crossbar memories, *Journal of Nanoscience and Nanotechnology*, **7**(1), pp. 151–167.

STRUKOV-D., AND LIKHAREV-K. (2011). *Reconfigurable Nano-Crossbar Architectures*, Contribution to R. Waser's collection "Nanoelectronics and Information Technology", 3rd ed., Wiley, *http://tinyurl.com/was11* (visited on 5/8/2011).

STRUKOV-D., AND WILLIAMS-R. (2009a). Exponential ionic drift: fast switching and low volatility of thin-film memristors, *Applied Physics A: Materials Science & Processing*, **94**(3), pp. 515–519.

STRUKOV-D., AND WILLIAMS-R. (2009b). Four-dimensional address topology for circuits with stacked multilayer crossbar arrays, *Proceedings of the National Academy of Sciences*, **106**(48). art no. 20155.

STRUKOV-D. B. (2006). *Digital Architectures for Hybrid CMOS/Nanodevice Circuits*, Doctoral dissertation in Electrical Engineering, Stony Brook University, NY.

STRUKOV-D., SNIDER-G., STEWART-D., AND WILLIAMS-R. (2008). The missing memristor found, *Nature*, **453**(7191), pp. 80–83.

SUN-W., LI-C., AND YU-J. (2009a). A memristor based chaotic oscillator, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 955–957.

SUN-W., LI-C., AND YU-J. (2009b). A simple memristor based chaotic oscillator, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 952–954.

SUN-X., LI-G., DING-L., YANG-N., AND ZHANG-W. (2011). Unipolar memristors enable "stateful" logic operations via material implication, *Applied Physics Letters*, **99**. art no. 072101.

SUN-Z., MIZUGUCHI-M., MANAGO-T., AND AKINAGA-H. (2004). Magnetic-field-controllable avalanche breakdown and giant magnetoresistive effects in gold/ semi-insulating-gaas schottky diode, *Applied physics letters*, **85**(23), pp. 5643–5645.

SWAROOP-B., WEST-W. C., MARTINEZ-G., KOZICKI-M. N., AND AKERS-L. A. (1998). Programmable current mode Hebbian learning neural network using programmable metallization cell, *IEEE International Symposium on Circuits and Systems, ISCAS*, Vol. 3, pp. 33–36.

SZOT-K., SPEIER-W., BIHLMAYER-G., AND WASER-R. (2006). Switching the electrical resistance of individual dislocations in single-crystalline $SrTiO_3$, *Nature Materials*, **5**(4), pp. 312–320.

TAPPERTZHOFEN-S., LINN-E., NIELEN-L., ROSEZIN-R., LENTZ-F., BRUCHHAUS-R., VALOV-I., B"OTTGER-U., AND WASER-R. (2011). Capacity based nondestructive readout for complementary resistive switches, *Nanotechnology*, **22**. art no. 395203.

TAVAKOLI-M., AND SARPESHKAR-R. (2005). A sinh resistor and its application to tanh linearization, *IEEE Journal of Solid-State Circuits*, **40**(2), pp. 536–543.

THAKOOR-S., MOOPENN-A., DAUD-T., AND THAKOOR-A. (1990). Solid-state thin-film memistor for electronic neural networks, *Journal of Applied Physics*, **67**(6), pp. 3132–3135.

TULINA-N. A., BORISENKO-I. Y., AND SIROTKIN-V. V. (2008). Reproducible resistive switching effect for memory applications in heterocontacts based on strongly correlated electron systems, *Physics Letters A*, **372**(44), pp. 6681–6686.

TYSHCHENKO-O., AND SHEIKHOLESLAMI-A. (2008). Match sensing using match-line stability in content-addressable memories (CAM), *IEEE Journal of Solid-State Circuits*, **43**(9), pp. 1972–1981.

UEHARA-A., KAGAWA-K., TOKUDA-T., OHTA-J., AND NUNOSHITA-M. (2003). Back-illuminated pulse-frequency-modulated photosensor using silicon-on-sapphire technology developed for use as epi-retinal prosthesis device, *Electronics Letters*, **39**, p. 1102.

VALOV-I., WASER-R., JAMESON-J. R., AND KOZICKI-M. N. (2011). Electrochemical metallization memories-fundamentals, applications, prospects, *Nanotechnology*, **22**(25). art no. 254003.

VARGHESE-D., AND GANDHI-G. (2009). Memristor based high linear range differential pair, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 935–938.

VENTRA-M. D., PERSHIN-Y., AND CHUA-L. (2009). Circuit elements with memory: Memristors, memcapacitors, and meminductors, *Proceedings of the IEEE*, **97**(10), pp. 1717–1724.

VERMA-N., AND CHANDRAKASAN-A. (2008). A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy, *IEEE Journal of Solid-State Circuits*, **43**(1), pp. 141–149.

VERSACE-M., AND CHANDLER-B. (2010). The brain of a new machine, *IEEE Spectrum*, **47**(12), pp. 30–37.

VILAN-A. (2007). Analyzing molecular current-voltage characteristics with the Simmons tunneling model: Scaling and linearization, *The Journal of Physical Chemistry C*, **111**(11), pp. 4431–4444.

VILLA-C., MILLS-D., BARKLEY-G., GIDUTURI-H., SCHIPPERS-S., AND VIMERCATI-D. (2010). A 45 nm 1 Gb 1.8 V phase-change memory, *IEEE International Solid-State Circuits Conference Digest of Technical Papers, ISSCC*, pp. 270–271.

VOLD-T. G. (1993). An introduction to geometric calculus and its application to electrodynamics, *American Journal of Physics*, **61**, pp. 505–505.

VONTOBEL-P. O., ROBINETT-W., KUEKES-P. J., STEWART-D. R., STRAZNICKY-J., AND WILLIAMS-R. S. (2009). Writing to and reading from a nano-scale crossbar memory based on memristors, *Nanotechnology*, **20**(42). art no. 425204.

References

WANG-D., ZHAO-H., AND YU-J. (2009a). Chaos in memristor based Murali-Lakshmanan-Chua circuit, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 958–960.

WANG-F. Y. (2008). Memristor for introductory physics, *Preprint arXiv:0808.0286*, .

WANG-W., YU-Q., XU-C., AND CUI-Y. (2009b). Study of filter characteristics based on PWL memristor, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 969–973.

WANG-X., CHEN-Y., XI-H., LI-H., AND DIMITROV-D. (2009c). Spintronic memristor through spin-torque-induced magnetization motion, *IEEE Electron Device Letters*, **30**(3), pp. 294–297.

WANG-X., WONG-W., AND HORNSEY-R. (2006). A high dynamic range CMOS image sensor with inpixel light-to-frequency conversion, *IEEE Transactions on Electron Devices*, **53**(12), pp. 2988–2992.

WASER-R., AND AONO-M. (2007). Nanoionics-based resistive switching memories, *Nature Materials*, **6**(11), pp. 833–840.

WASER-R., DITTMANN-R., STAIKOV-G., AND SZOT-K. (2009). Redox-based resistive switching memories - nanoionic mechanisms, prospects, and challenges, *Advanced Materials*, **21**(25-26), pp. 2632–2663.

WIDROW-B. (1960). An adaptive 'ADALINE' neuron using chemical "memistors", *Technical Report TR-1553-2 23, Oct.*, Stanford Electronics Laboratories Technical Report.

WILLIAMS-R. (2008). How we found the missing memristor, *IEEE Spectrum*, **45**(12), pp. 28–35.

WILLIAMS-S. (2010). HP collaborates with Hynix to bring the memristor to market in next-generation memory. *http://tinyurl.com/hpmemristor* (visited on 3/9/2011).

WITRISAL-K. (2009). Memristor-based stored-reference receiver–the UWB solution?, *Electronics Letters*, **45**(14), pp. 713–714.

XIA-Q. (2011). Nanoscale resistive switches: devices, fabrication and integration, *Applied Physics A: Materials Science & Processing*, **102**, pp. 955–965.

XIA-Q., PICKETT-M. D., YANG-J. J., LI-X., WU-W., MEDEIROS-RIBEIRO-G., AND WILLIAMS-R. S. (2011a). Two-and three-terminal resistive switches: Nanometer-scale memristors and memistors, *Advanced Functional Materials*, **21**(14), pp. 2660–2665.

XIA-Q., PICKETT-M. D., YANG-J. J., ZHANG-M.-X., BORGHETTI-J., LI-X., WU-W., MEDEIROS-RIBEIRO-G., AND WILLIAMS-R. S. (2011b). Impact of geometry on the performance of memristive nanodevices, *Nanotechnology*, **22**(25). art no. 254026.

XIE-Y. (2011). Modeling, architecture, and applications for emerging memory technologies, *Design & Test of Computers*, **28**(1), pp. 44–51.

XU-C., DONG-X., JOUPPI-N., AND XIE-Y. (2011). Design implications of memristor-based RRAM cross-point structures, *Design, Automation & Test in Europe Conference & Exhibition, DATE*, pp. 1–6.

XU-C., KI-W., AND CHAN-M. (2002). A low-voltage CMOS complementary active pixel sensor (CAPS) fabricated using a 0.25 μm CMOS technology, *IEEE Electron Device Letters*, **23**(7), pp. 398–400.

XUE-K. (2010). *Device physics of Correlated Electron Random Access Memory*, Doctoral dissertation in Electrical and Electronics Engineering, University Of Colorado, Colorado Springs.

YAGI-M., AND SHIBATA-T. (2003). An image representation algorithm compatible with neural-associative-processor-based hardware recognition systems, *IEEE Transactions on Neural Networks*, **14**(5), pp. 1144–1161.

YANG-J., PICKETT-M., LI-X., OHLBERG-D., STEWART-D., AND WILLIAMS-R. (2008). Memristive switching mechanism for metal/oxide/metal nanodevices, *Nature nanotechnology*, **3**(7), pp. 429–433.

YI-W., PERNER-F., QURESHI-M., ABDALLA-H., PICKETT-M., YANG-J., ZHANG-M.-X., MEDEIROS-RIBEIRO-G., AND WILLIAMS-R. (2011). Feedback write scheme for memristive switching devices, *Applied Physics A: Materials Science & Processing*, **102**, pp. 973–982.

YU-Q., QIN-Z., YU-J., AND MAO-Y. (2009). Transmission characteristics study of memristors based op-amp circuits, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 974–977.

YU-S., AND WONG-H. (2011). Compact modeling of conducting-bridge random-access memory (CBRAM), *IEEE Transactions on Electron Devices*, **58**(5), pp. 1352–1360.

YU-S., LIANG-J., WU-Y., AND WONG-H. (2010). Read/write schemes analysis for novel complementary resistive switches in passive crossbar memory arrays, *Nanotechnology*, **21**. art no. 465202.

ZAMARREÑO-RAMOS-C., CAMUÑAS-MESA-L., PÉREZ-CARRASCO-J., MASQUELIER-T., SERRANO-GOTARREDONA-T., AND LINARES-BARRANCO-B. (2011). On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex, *Frontiers in Neuroscience*, **5**.

ZHANG-C., SRIVASTAVA-A., AND AJMERA-P. (2003). Low voltage CMOS schmitt trigger circuits, *Electronics Letters*, **39**(24), pp. 1696–1698.

ZHANG-Y., ZHANG-X., AND YU-J. (2009). Approximated SPICE model for memristor, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 928–931.

ZHIRNOV-V., CAVIN-R., MENZEL-S., LINN-E., SCHMELZER-S., BRÄUHAUS-D., SCHINDLER-C., AND WASER-R. (2010). Memory devices: Energy–space–time tradeoffs, *Proceedings of the IEEE*, **98**(12), pp. 2185–2200.

Glossary

The physical constants used in this thesis are in accordance with a recommendation of the Committee on Data for Science and Technology (Mohr and Taylor 2005). For example:

Quantity	Symbol	Value
Boltzmann constant	k_B	$1.380\,6505(24) \times 10^{-23}$ J/K
		$8.617\,343(15) \times 10^{-5}$ eV/K
electron volt	eV	$1.602\,176\,53(14) \times 10^{-19}$ J

Acronyms

Acronyms

FPN	Fixed pattern noise, 104
FSM	Finite state machine, 157
HfO_2	Hafnia, 24
HfO_2	Hafnium oxide, 186
HRS	High resistance state, 60
IP	Internet protocol, 143
ISI	Inter-spike interval, 177
ITO	Indium thin oxide, 59
KCL	Kirchhoff's current law, 129
LCO	Light-control oscillator, 108
LER	Line edge roughness, 135
LRS	Low resistance state, 60
LTM	Long-term memory, 173
LTP	Long-term potentiation, 176
MCAM	Memristor-based content addressable memory, 143
MIM	Metal-insulator-metal, 15
MRI	Magnetic resonance imaging, 101
MRM	Metal-resistor-metal, 73
mSTDP	Memristor-based spike-timing-dependent plasticity, 85
NiO	Nickel oxide, 24
OTP	One-time programmable, 30
PCM	Phase change memory, 53
PD	Photodiode, 104
PFM	Pulse-frequency modulation, 108

TiO_2	Titanium dioxide, 24
TLB	Translation lookaside buffer, 143
TMO	Transition metal oxides, 24
UWB	Ultra-wide band, 27
ZrO_2	Zirconia, 24
ZrO_2	Zirconium oxide, 186

Index

Index

Biography

Omid Kavehei was born in Arak, Iran, in 1981. From 1999 to 2003, he was educated at Arak Azad University, in his hometown, where he obtained a Bachelor's Degree in Computer System Engineering with the highest rank in that year. His final year research project was carried out under A/Prof Keivan Navi on *Current-Mode Computing*. Soon after graduating, he joined the Microelectronics group at the National University of Iran (aka: Shahid Beheshti University), Tehran, Iran, in 2003. He obtained his Master's Degree in Computer Systems Architecture Engineering again with highest rank, under A/Prof Keivan Navi on *Very Large Scale Integration (VLSI) Design Aspects of Arithmetic Circuits: Adders, Compressors, and Multipliers*. He also carried out several research projects on system-on-chip, digital signal processing, analogue computing, operating systems, and bioinformatics. He served at his *alma mater* as a research and teaching assistant and a casual lecturer. In this role, he conducted VLSI Design course and Digital Logic Design Labs in the Department of Computer Engineering.

In 2008, he was granted an Australian Endeavour International Postgraduate Research Scholarship (EIPRS) and University of Adelaide Scholarship to pursue his PhD under Dr Said Al-Sarawi and Prof Derek Abbott, the School of Electrical & Electronic Engineering, The University of Adelaide. In 2009 and 2010, he was a Visiting Scholar at the Technology Park, the Chungbuk National University, South Korea, hosted by Prof Kamran Eshraghian. During his candidature, Mr Kavehei has received an D.R. Stranks Travelling Fellowship, 2009, Simon Rockliff Scholarship for the most outstanding postgraduate mentorship from the School of Electrical & Electronic Engineering and DSTO, 2010, Research Abroad Scholarship, 2010, and the Korea's World Class University program research fellowships, 2009 and 2010. He is also a student member of the IEEE, IEEE Communications Society, the Institution of Engineers Australia, Australasian Association for Engineering Education, WCU (KOSEF) project member, and an executive member of the SA IEEE student chapter called the Electrical and Electronic Engineering Society of Adelaide University. In 2011, he was awarded the Young Nanotechnology Ambassador awarded form the ARC Australian Nanotechnology Network. He is currently a Postdoctoral Research Fellow at the University of Melbourne.

<div align="right">

Omid Kavehei

omid@eleceng.adelaide.edu.au

http://www.eleceng.adelaide.edu.au/personal/kavehei/

</div>

Scientific Genealogy of
Omid Kavehei

—— *Formalised supervisor relationship*
····· *Mentoring relationship*
👤 *Nobel prize*

1668 – MA, University of Cambridge, Isaac Newton

1706 – MA, University of Cambridge, Roger Cotes

1715 – MA, University of Cambridge, Robert Smith

1723 – MA, University of Cambridge, Walter Taylor

1742 – MA, University of Cambridge, Stephen Whisson

1774 – MA, University of Cambridge, John Cranke   1756 – MA, University of Cambridge, Thomas Postlethwaite

1800 – MA, University of Cambridge, John Hudson   1782 – MA, University of Cambridge, Thomas Jones

1816 – MA, University of Cambridge, George Peacock   1811 – MA, University of Cambridge, Adam Sedgwick

1827 – BA, University of Cambridge, Augustus De Morgan   1830 – MA, University of Cambridge, William Hopkins

1857 – MA, University of Cambridge, Edward John Routh

1868 – MA, University of Cambridge, John William Strutt (Lord Rayleigh) 👤

1883 – MA, University of Cambridge, Joseph John Thomson 👤

1903 – MA, U of Cambridge, John Sealy Edward Townsend

1923 – DPhil, University of Oxford, Victor Albert Bailey

1911 – MSc, University of Melbourne, Edward (Eddy) Byam Brown   1948 – MSc, University of Sydney, Ronald Ernest Aitchison

1945 – MA, University of Melbourne, Eric Osbourne Willoughby   1964 – PhD, University of Sydney, Peter Harold Cole

1968 – PhD, University of Adelaide, Bruce Raymond Davis   1980 – PhD, University of Adelaide, Kamran Eshraghian

1995 – PhD, University of Adelaide, Derek Abbott   2003 – PhD, University of Adelaide, Said Al-Sarawi

2011 – PhD, University of Adelaide, **Omid Kavehei**