Reference Spurs in an Integer-N Phase-Locked Loop: Analysis, Modelling and Design

by

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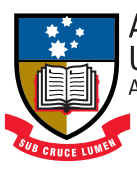

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Abstract

The Phase-Locked Loop (PLL) is commonly used for frequency synthesis in RF transceivers. It can be implemented in two architectures, namely, fractional-N and integer-N. In this thesis, the integer-N architecture is chosen due to its suitability for frequency planning.

Here, a PLL with a low noise output is important to ensure signal purity. There are two dominant noise sources in a PLL, namely, phase noise and periodic noise. In the integer-N PLL, periodic noise is also referred to as a reference spur, where the noise gives rise to multiple reference frequency offsets at the PLL output. Of these two noise sources, this thesis is focused on the analysis and suppression of reference spurs. It is because less work has been carried in the literature regarding spurs, and phase noise is better studied. The main factors underlying reference spurs are discussed. These factors are mainly from the charge pump and phase/frequency detector (PFD) circuit non-idealities, namely, PFD delay, charge pump current leakage, charge pump current mismatch, and rise and fall times characteristic of the charge pump current.

Reference spur magnitude can be predicted via a transient analysis. The simulation is time consuming, as the reference spur magnitude can only be captured after the PLL in its locked state. Therefore, the simulation period has to be set long enough to ensure enough data can be obtained to read that state. In this thesis, a reference spur mathematical analysis is presented to accurately estimate the reference spur magnitude. In the analysis, all the circuit non-idealities that contribute to the reference spur are considered. Circuit parameters required in the mathematical analysis can be obtained from transistor level simulation for each circuit. As the simulation for each circuit can be carried out separately, a large amount of simulation time can be saved. The proposed mathematical analysis also can be used to determine the major contributing factor to the problem of reference spurs.

The reference spur also can be estimated via behavioural modelling simulation. Behavioural modelling of the PLL using Simulink is presented in this thesis. Each PLL component is modelled separately, and circuit non-idealities contributing to the reference spur are included in the behavioural model. In addition to reference spur estimation,

the PLL behavioural model also can be used to visualise the dynamic behaviour of the system.

Results from the spur analysis show that a slight mismatch current in the charge pump helps to improve the reference spur performance. This thesis presents an analysis to determine an optimum charge pump current ratio for reference spur suppression, which is caused by the charge pump current mismatch and the switching delay. Further, a ratioed current charge pump circuit is proposed to replace the conventional charge pump circuit for a reference spur performance improvement. This spur suppression technique is implemented using a 180 nm SiGe BiCMOS technology for performance evaluation.

Statement of Originality

This work contains no material that has been accepted for the award of any other degree or diploma in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published written by another person, except where due reference has been made in the text.

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Noorfazila Kamal

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Thesis Conventions

The following conventions have been adopted in this Thesis:

1. **Notation.** The acronyms used in this thesis are defined in the List of Acronyms on page 169.

2. **Spelling.** Australian English spelling conventions have been used, as defined in the Macquarie English Dictionary (A. Delbridge (Ed.), Macquarie Library, North Ryde, NSW, Australia, 2001). Where two alternative spellings are allowed such as *biassing* or *biasing*, the shorter option is chosen. Also the word *analogue* is written *analog* due to its widespread usage in the engineering literature, even though it is not an Australian spelling.

3. **Typesetting.** This document was compiled using LaTeX2e. TeXnicCenter was used as text editor interfaced to LaTeX2e. TGIF was used to produce schematic diagrams and other drawings.

4. **Mathematics.** MATLAB code was written using MATLAB Version R2009a.

5. **Referencing.** The Harvard style has been adopted for referencing.

5. **Punctuation.** The Oxford convention for commas has been used for punctuation.

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Publications

KAMAL-N., AL-SARAWI S. F., AND ABBOTT-.D. (2012). An accurate analytical spur model for an integer-*N* phase-locked loop, *Proceedings of 4th International Conference on Intelligent and Advanced Systems, (ICIAS 2012)*, Vol. 2, pp. 659-664

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Chapter 1

Introduction

THE presented research is a part of the Gigabit Low-cost Integrated Millimeter-wave Radio (GLIMMR) project. This chapter briefly presents the GLIMMR project. Then, the role of a frequency synthesiser in RF transceivers is also presented. The motivation and a summary of novelty of contributions are also provided. Finally, the thesis structure is presented.

1.1 Introduction

This chapter gives an overview of this thesis. This thesis is a part of the Giga-Hertz Low-cost Integrated Millimeter-wave Radio (GLIMMR) project, where the overall objective is to develop a 60 GHz RF wireless communication system. An overview of the project is provided in Section 1.2. This thesis only focuses on the PLL based frequency synthesiser for 60 GHz transceivers, where the role of frequency synthesiser in RF transceivers is discussed in Section 1.3.

In Section 1.4, the motivation for this project is provided. In addition, the scope and objectives of the work are also presented. Next, Section 1.5 summarises the major contributions presented in this thesis. Finally, organisation of this thesis is presented in Section 1.6.

1.2 GLIMMR

The GLIMMR project is carried out at three universities, namely, Macquarie University, University of South Australia, and The University of Adelaide. This project is funded by an Australian Research Council (ARC) Linkage Grant, together with the main commercial sponsor, NHEW R&D Pty. Ltd., with Cadence Design System, Jazz Semiconductor, Peregrine Semiconductor, Inter Corporation, and AWR as supporting sponsors.

The aim of the GLIMMR project is to develop an inexpensive and low power on-chip system for a mm-wave short range communication using the 60 GHz band with a high speed data rates of Gbps (Weste *et al.* 2007, Howarth *et al.* 2005). To achieve this goal, a 180 nm SiGe technology is chosen for the circuit implementation (Weste *et al.* 2007, Howarth *et al.* 2005). A detail discussion on why the 60 GHz band is chosen is presented in Section 1.2.1.

The GLIMMR project has two major components, which are at RF and baseband. The RF components, including the antenna, were designed at Macquarie University and The University of Adelaide, while the digital baseband and Medium Access Control (MAC) layer were tackled by a research group at the University of South Australia.

For the RF components, GLIMMR proposes a dual conversion superheterodyne architecture with the first local oscillator (LO) operating at 48 GHz, and the intermediate

frequency (IF) is at 12 GHz (Weste *et al.* 2007, Howarth *et al.* 2005). The proposed receiver architecture is shown in Figure 1.1.

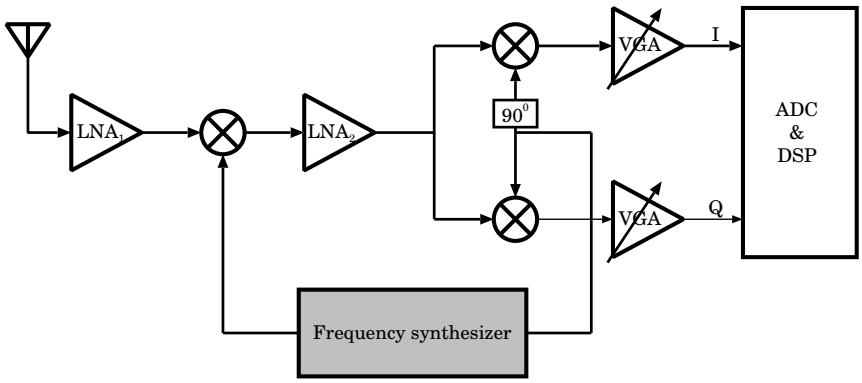


Figure 1.1. A double conversion receiver proposed by GLIMMR. Here, LNA is the low noise amplifier, VGA is the variable gain amplifier, ADC is the analog-to-digital converter, and DSP is the digital signal processing. The frequency synthesizer provides two reference frequencies for frequency translation, where the first frequency is at 48 GHz, while the I & Q frequency is at 12 GHz.

Since 2006, three GLIMMR test chips (GTC) have been designed and fabricated. The first test chip, GTC1, contained individual RF and analog components for design validation. Then, a complete transmitter and receiver including bond-wire antennas were developed in test chip GTC2. Also, a frequency synthesiser and a prescaler test circuit was also fabricated in GTC2. Lastly, in the third test chip, GTC3, subdicing was performed to completely separate the transmitter and receiver, hence independent transmit and receive modules were obtained. Images of these three test chips are included in Appendix B.1.

This thesis focuses on part of the RF transceiver design. An RF transceiver consists of an antenna, amplifier, mixer and a local oscillator (LO). This work is only concentrates on the local oscillator (LO) design for the RF transceiver. The LO provides a frequency to translate a baseband to an RF signal. This can be achieved by using a phase locked loop (PLL) based frequency synthesiser.

1.2.1 60 GHz Band

Nowadays, wireless communications became a part of our life. Wireless devices such as mobile phones, wireless local area networks (WLAN), and bluetooth are widely

used. These devices operate around the 2.4 GHz and 5 GHz bands, giving rise to microwave band traffic congestion. Furthermore, the data rate is limited to only up to a few Mbps. Therefore, the millimeter-wave (mm-wave) band is explored to accommodate higher bandwidth RF communication applications.

The mm-wave band ranges from 30 mm to 300 mm in wavelength, which is between 30 GHz and 300 GHz in frequency. However, only the band around 60 GHz is of particular interest, because it is an industrial, scientific and medical (ISM) free license band. A few countries have allocated the free band. America, Korean, and Canada allocate 7 GHz bandwidth from 57 GHz to 64 GHz. Australia has a smaller band between 59.5 GHz to 62.9 GHz, while Japan allocates 59 GHz to 66 GHz, and Europe has the largest band between 57 GHz and 66 GHz. Chart in Figure 1.2 shows the allocated bands.

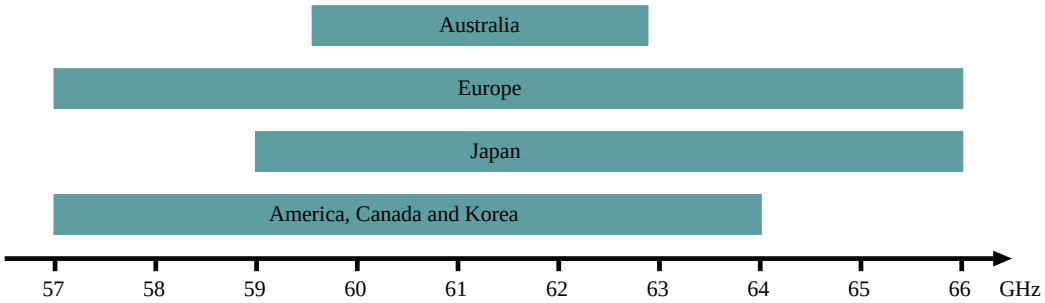


Figure 1.2. International band allocation in the 60 GHz region. This chart indicates that there is a range of at least 3 GHz where all allocated bands overlap. Therefore, this is a useful target region for commersial application.

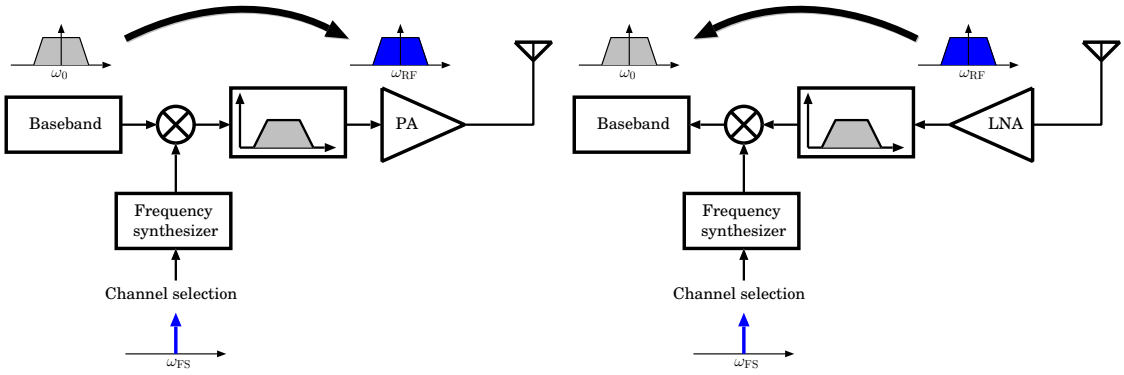
Compared to prior wireless communications, the 60 GHz band provides a very large bandwidth. The 2.4 GHz ISM band only has 100 MHz bandwidth from 2.4 to 2.5 GHz, while the 5 GHz band covers 600 MHz from 5.2 to 5.8 GHz. Meanwhile, the 60 GHz band provides at least 3.4 GHz bandwidth, as shown in Figure 1.2. The transmitting signal at this high GHz band also enables high data rate applications. The targeted data rate for the 60 GHz band is greater than 2 Gb/s (Doan *et al.* 2004).

The 60 GHz band has interesting characteristics, making the band very suitable for a short range wireless communication. A prominent characteristic of the band is that the signal is highly absorbed by oxygen, with 10-15 dB/km. The signal propagation is also affected by the indoor environment. For example, a 2.5 cm thickness dry wall attenuates the signal by 6 dB and a 1.9 cm thickness office whiteboard attenuates the signal by 9.6 dB (Smulders 2003). These characteristics make the 60 GHz band only suitable

for short range communications ($<$ 1km) (Smulders 2003, Kornegay 2003). Also, it provides high security communications since the signal unable to travel far away from the intended area. In addition, the attenuation property reduces interference from other users and improves frequency reuse.

1.3 Frequency Synthesiser

A frequency synthesiser plays a very important role in RF transceivers. The synthesiser provides a reference frequency for frequency translation in an RF transceiver. In an up-conversion process, a baseband signal modulates the synthesiser signal resulting in an RF signal ready for transmission. On the other hand, during the down-conversion process, the synthesiser signal modulates the RF signal in order to recover the baseband signal. Figure 1.3 shows the role of frequency synthesiser in RF transceivers.



(a) Up-conversion in an RF transmitter. (b) Down-conversion in an RF receiver.

Figure 1.3. Roles of a frequency synthesiser in RF transceivers. A frequency synthesiser provides a reference frequency for frequency translation in the up-conversion and down-conversion process.

For channel selection, a frequency synthesiser output is required to vary for the full RF bandwidth. For example, the 60 GHz band conventionally has a 7 GHz bandwidth from 54 GHz to 64 GHz. Therefore, the frequency synthesiser output must be able to vary in this wide frequency range. In other words, the frequency synthesiser acts as a channel selector in RF transceivers.

A frequency synthesiser can be classified into two types, namely, a direct and indirect synthesiser (Chenakin 2007, Bu *et al.* 2006, Marques *et al.* 1998). A direct synthesiser directly produces an output signal from a reference clock frequency without a feedback

loop. This type of synthesiser can be implemented in analog or digital (Chenakin 2007). A direct synthesiser enables fast switching speed (Chenakin 2007, Bu *et al.* 2006). However, this topology only gives a limited frequency coverage (Chenakin 2007), and is not suitable for a high frequency system (Marques *et al.* 1998).

The indirect synthesiser can be implemented using phase-locked loop (PLL). The PLL is a negative feedback system that compares its output frequency to a reference frequency. The main advantage of PLLs are that they can provide a very high frequency signal, however, they suffer from a longer switching time compared to a direct synthesiser (Chenakin 2007). As the PLL provides a high frequency output signal, this type of synthesiser is commonly used in RF transceivers (Bu *et al.* 2006, Lagareste *et al.* 2005).

1.4 Motivation

The 60 GHz band appears to be a very good alternative for short range communications such as in wireless personal area networks (WPAN). However, designing an RF transceiver at 60 GHz that has low noise, low power, and low cost is a significant challenge. Monolithic integration not a significant issue because higher frequencies lead to smaller RF components.

For a frequency synthesiser in 60 GHz transceivers, a low noise PLL output to cover a wide bandwidth is very hard to achieve. Noise in PLLs can be classified into phase noise and periodic noise. The phase noise is mainly contributed by device flicker, shot, and thermal noise. Meanwhile, periodic noise is caused by switching events in the PLL and are exacerbated by circuit non-idealities. The periodic noise is also referred to as *reference spurs* because the noise appears at multiple reference frequency offsets from the carrier signal.

The phase noise is mainly contributed by the voltage controlled oscillator (VCO) in the PLL. For a 60 GHz system, the VCO has to produce a wide frequency range to cover the wide channel bandwidth. With current low voltage technology, a large varactor is required to cover the wide bandwidth, resulting in a high VCO gain. This high VCO gain makes the VCO very sensitive to any noise. A small noise variation at the input is amplified by the VCO gain, resulting in a much higher phase noise at the output.

The high VCO gain also causes high reference spurs in the PLL output. The reference spur is caused by a periodic ripple in the VCO input voltage. The ripple magnitude

has a linear relationship with the VCO gain. Therefore, a higher VCO gain results in a higher reference spur. Several works have been carried out to model and estimate the reference spur magnitude (Shu and Sinencio 2005, Manassewitsch 2005). However, these estimations never been compared with the measurement or simulation results.

The reference spur simulation is time consuming, as the spur magnitude can only be obtained after the PLL is locked. Therefore, a long simulation period is required to ensure the PLL is locked before the data can be captured. Alternatively, a behavioural modelling simulation can help to save simulation time. Each circuit non-ideality has to be included in the behavioural model in order to accurately predict the spur magnitude.

In this thesis, reference spurs in an integer-N PLL are analysed in time domain. The analysis is found to accurately estimate the spur magnitude. Based on this mathematical analysis, the affect of each circuit non-ideality on the reference spur magnitude is investigated. Further, a PLL behavioural model for reference spur estimation is also presented. Each circuit non-ideality is included in the behavioural model. Finally, a spur suppression technique is proposed to decrease reference spur magnitude in the PLL output.

1.5 Major Contributions

This thesis presents three major contributions as follows:

- Reference spur mathematical analysis (Chapter 4):
  The reference spur is a serious problem in RF transceivers as it can degrade the signal-to-noise ratio in data reception and transmission. The spur is dominated by non-idealities in the phase/frequency detector (PFD) and charge pump circuits, namely, PFD delay, charge pump current leakage, current mismatch, switching delay, and rise and fall time characteristics. In this work, a time domain analysis is presented in order to estimate the spur. Each non-ideality in the PFD and charge pump is included in order to accurately analyse the spur magnitude. In addition, the major contributing factor to the reference spur can be determined using this mathematical analysis.

- Reference spur behavioural modelling (Chapter 5):
  The PLL transistor level simulation is time consuming. A long period transient

simulation has to be performed to ensure enough data is obtained. A power spectral density of the PLL output after it is locked is obtained in order to estimate reference spurs. This work introduces behavioural modelling to accurately estimate the reference spur magnitude in a very short simulation time, using a Simulink based behavioural model. The behavioural modelling can save significant amount of simulation period compared to transistor level simulation without significant loss in simulation accuracy.

- Reference spur suppression techniques (Chapters 6 and 7):
  This thesis proposes a method to calculate an optimum charge pump current to minimise the ripple on the tuning voltage caused by the charge pump current mismatch and switching delay, hence improving the reference spur performance. This approach can be implemented by optimum sizing of the transistors in the charge pump. With this minimal change to the circuit, this approach can be combined with other spur suppression techniques such as low VCO gain, current leakage compensation and charge distribution techniques to further suppress the reference spur. Using the proposed optimum charge pump current calculation, a ratioed current charge pump circuit is proposed to replace the conventional charge pump circuit in the PLL for reference spur suppression. The effectiveness of the proposed technique is demonstrated through the design of a PLL that employs the ratioed current charge pump using a 180 nm SiGe BiCMOS technology.

1.6 Thesis Outline

This thesis is divided into two parts. The first part discusses the PLL fundamentals and its noise, which is provided in Chapters 2 and 3. The second part covered in Chapters 4, 5, 6 and 7, contain the novel work in this thesis. A summary of each chapter is as follows:

Chapter 2 provides the PLL fundamentals. Three types of PLL, namely, an analog, digital, and all-digital PLL are reviewed. Also, two types of PLL architecture that are commonly used are discussed. Further, a detailed discussion of a charge pump PLL and its components are presented. Finally, challenges in the design of PLL for a 60 GHz transceiver are discussed.

A low noise PLL is very important in RF transceivers. Two types of noise in the PLL, namely, phase noise and periodic noise are discussed in Chapter 3. The affect of these noise sources on RF communications are also presented.

In Chapter 4, a time domain analysis is presented to estimate the reference spur magnitude. Each main factor that contributes to the reference spur is included in the analysis. Further, using the analysis, the main factor that gives the largest effect to the reference spur magnitude is determined.

Chapter 5 presents PLL behavioural modelling in Simulink. The behavioural model also can be used to estimate the reference spur magnitude, and PLL dynamic behaviour. Each PLL component is modelled separately. The PFD and charge pump non-idealities that contribute to the reference spur are included in the model.

In Chapter 6, a review of several spur suppression design techniques are presented. Then, an analysis to determine an optimum charge pump current ratio to improve the reference spur performance is presented. This optimum charge pump current ratio can be implemented by resizing transistors in the charge pump circuit, and the circuit is thereby named a *ratioed current charge pump*.

In Chapter 7, the ratioed current charge pump, as proposed in Chapter 6, is implemented in the transistor level circuit. The reference spur magnitude of the proposed circuit is compared with a conventional charge pump PLL.

Finally, a conclusion and suggestion for further work are presented in Chapter 8.

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Chapter 2

Phase-Locked Loop Fundamentals

A PHASE-Locked Loop (PLL) based frequency synthesiser is commonly used in RF transceivers. There are three types of PLL, namely, an analog PLL, digital PLL, and all-digital PLL. A given PLL can be implemented in various different architectures, but integer-N and fractional-N architectures are commonly used. This work uses an integer-N charge pump PLL, as this architecture is suitable for our proposed frequency planning. This chapter reviews PLL types and architectures. A charge pump PLL is chosen, and detailed discussion on each component in the charge pump PLL is presented. In addition, challenges in designing a PLL for a 60 GHz transceiver are also reviewed.

2.1 Introduction

The PLL is commonly used as a frequency synthesiser in RF transceivers because of its low noise output. As discussed in the previous chapter, a low noise reference frequency is very important in both the up-conversion and down-conversion processes in an RF transceiver to maintain the purity of the data while transmitting it.

Ideally, a crystal oscillator can be used because of its superior phase noise performance, however, there are two major problems with the crystal oscillator, that makes it unsuitable for use in frequency synthesis. First, a crystal oscillator is only available at low frequency, thus it cannot be used for an RF transceiver operating at a few GHz or more. Secondly, a crystal oscillator can only provide one fixed frequency. Multiple frequencies are required in RF transceivers for channel selection purposes. As an alternative, a current-controlled oscillator (CCO) or voltage-controlled oscillator (VCO) can be used, and the latter is most commonly used.

The VCO uses a resonance circuit that generates an output signal at a frequency, f_{out}, according to its control voltage. The output frequency can be tuned by varying the control voltage, thus allowing channel selection. The drawback of this system is the output frequency is vulnerable to noise from the control voltage. Also, internal noise from the VCO contributes noise to the control voltage and is directly transferred to the output, resulting in the oscillation being tuned out of the required channel after a period of time as the output frequency drifts.

The advantage of a crystal oscillator's low noise and the frequency tunability of a VCO are combined in a PLL in order to provide a low noise carrier signal. Note that a PLL is a negative feedback system, which compares the VCO output with a reference frequency provided by a crystal oscillator. The basic PLL functional blocks are shown in Figure 2.1.

The VCO output phase, θ_{out}, is divided by N before comparing it with the reference phase provided by the crystal oscillator. A divider is required in the feedback loop to allow operation at much higher output frequencies compared to the frequency from the crystal oscillator. A phase detector (PD) compares the output phase to the reference phase and produce an error phase, θ_e. This phase error is converted to a voltage and is filtered before feeding it to the VCO. Therefore, the VCO control voltage is proportional to the phase error. The VCO control voltage then changes the output frequency. The process continues until θ_e approaches zero or some stable equilibrium value. At this

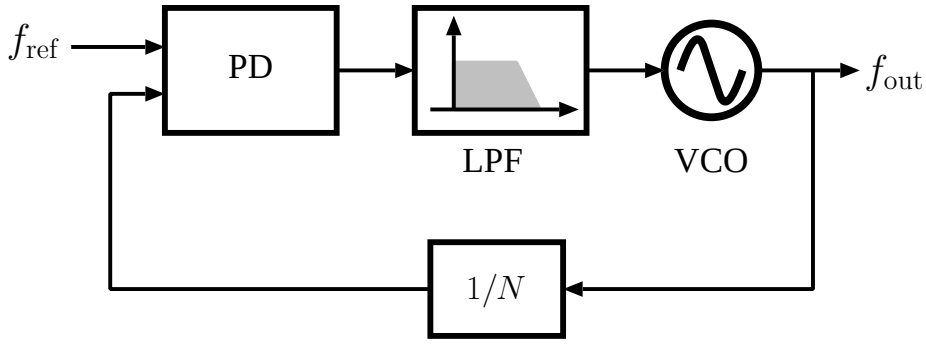


Figure 2.1. Phase-Locked Loop. The phase detector (PD) compares the phase between reference signal, f_{ref}, and divided output signal, f_{out}/N. The phase difference is converted into a voltage and is filtered by a low pass filter (LPF) before being coupled into the VCO. The VCO generates an oscillation frequency that is function of the input control voltage.

state, the PLL is considered locked and the loop maintains the output frequency. If the output frequency drifts, a small θ_e is produced and a corresponding voltage is produced to tune the VCO in order to recover the desired frequency.

Stability is an issue in a PLL design as it is a feedback system. Therefore, PLL performance is not only depends on the noise level at the output but is also based on a few parameters such as locking time (also known as settling time or switching time), acquisition range (also known as capture or pull-in range), and tracking range (or lock range). Locking time is the time required for the PLL to lock when channel switching occurs. Acquisition range is the maximum value of the phase error for which an unlocked PLL can eventually reach the lock state. In other words, a PLL will never lock if the phase error is more than the acquisition range. The tracking range is the maximum phase error offset for which a locked PLL will remain locked. Outside the tracking range, the PLL loses lock.

There are many ways to implement a PLL, depending on the application. This chapter discusses different kinds of PLLs and their implementation in Section 2.2. In Section 2.3, two commonly used PLL architectures are presented and discussed. Then, Section 2.4 focuses on the components of a charge pump PLL. This is then followed by PLL requirements for our 60 GHz application in Section 2.5 and lastly a summary is given Section 2.6.

2.2 Phase-Locked Loop Types

A PLL may be classified in three different types, namely, a linear PLL (also known as an analog PLL), digital PLL, and all-digital PLL (ADPLL). In principle, all operate in the same way but are constructed differently. All components in a linear PLL are constructed using analog circuits, while an ADPLL is developed using digital circuits. A digital PLL is an analog PLL with a digital phase detector (the frequency divider also may be digitally implemented). This means, the digital PLL has both, analog and digital circuits, and clearly differs from the ADPLL where all the components are digital. Another type of PLL is called the charge pump PLL. A charge pump PLL is similar to a digital PLL, except that an extra charge pump circuit is used in the loop to improve immunity to power supply noise.

2.2.1 Linear PLL

A linear PLL is constructed using three components, namely: (i) multiplier, which functions as a phase detector, (ii) low pass filter, and (iii) VCO. The operation of each component is explained in the following.

Phase detector

In a linear PLL, a multiplier is used as a phase detector. Let the reference signal and output signal be in sine waves with different phases, $v_{\text{ref}}(t)$ and $v_{\text{out}}(t)$, respectively with:

$$v_{\text{ref}}(t) = V_{\text{ref}} \sin(\omega_{\text{ref}} t + \theta_{\text{ref}}) \,, \tag{2.1}$$

$$v_{\text{out}}(t) = V_{\text{out}} \cos(\omega_{\text{out}} t + \theta_{\text{out}}) \,. \tag{2.2}$$

Multiplying these signals will produce:

$$\begin{aligned} v_{\text{pd}}(t) = {} & \frac{1}{2} V_{\text{ref}} V_{\text{out}} \left[\sin((\omega_{\text{ref}} - \omega_{\text{out}})t + \theta_{\text{ref}} - \theta_{\text{out}})\right] \\ & + \frac{1}{2} V_{\text{ref}} V_{\text{out}} \left[\sin((\omega_{\text{ref}} + \omega_{\text{out}})t + \theta_{\text{ref}} + \theta_{\text{out}})\right] \,. \end{aligned} \tag{2.3}$$

The multiplier output consist of a dc component, $V_{\text{ref}}V_{\text{out}}/2$, and the difference and the sum of reference and output frequency. With assumption $\omega_{\text{out}} \approx \omega_{\text{ref}}$, Equation 2.3 can be simplified to

$$v_{\text{pd}}(t) = \frac{1}{2} V_{\text{ref}} V_{\text{out}} \left[\sin(\theta_{\text{ref}} - \theta_{\text{out}}) + \sin(2\omega_{\text{ref}} t + \theta_{\text{ref}} + \theta_{\text{out}})\right] . \tag{2.4}$$

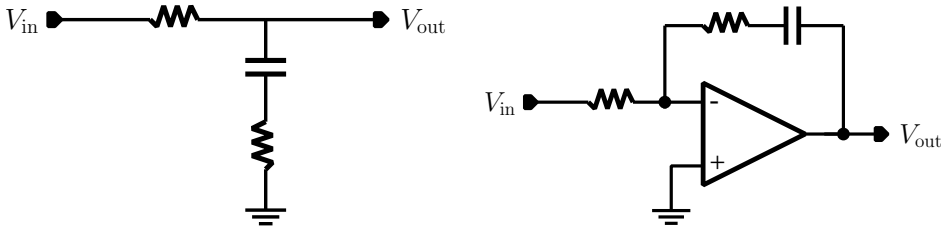
Only the dc and difference frequency components are wanted, while the sum component is filtered out by a low pass filter. Neglecting the sum component, the multiplier output can be rewritten as

$$v_{\text{pd}}(t) = K_{\text{pd}} \sin(\theta_{\text{e}}) , \tag{2.5}$$

where K_{pd} is the phase detector gain, which is the dc component, and θ_{e} is the phase error, which is given by $\theta_{\text{ref}}(t) - \theta_{\text{out}}(t)$. When the PLL is locked, which means the phase error is zero, v_{pd} is zero. In this state, the input and output frequency are the same but with a $\pi/2$ phase difference.

Loop filter

As mentioned previously, a low pass filter is required to eliminate the higher frequency term from the multiplier output. A number of low pass filter designs can be implemented, however, a lead-lag filter is most frequently used (Best 1999). Figure 2.2 shows a first-order passive and active lead-lag filter commonly used in a linear PLL.



(a) Passive lead-lag filter (b) Active filter

Figure 2.2. Low pass filter for linear PLL. Example of first order passive and active filter that can be used in a linear PLL.

VCO

The filtered signal is coupled to the VCO. As its name suggests, the VCO output frequency is changing as a function of the filtered error voltage signal until a steady state

is met. In this case, a steady state is met when the voltage is zero, where the reference input phase is 90° difference with the VCO output phase.

The VCO output frequency changes depending on its input voltage and the VCO gain, as given by

$$f_o = f_c + K_v V_{in}\,, \tag{2.6}$$

where f_o is output frequency, f_c is oscillator centre frequency, K_v is VCO gain (Hertz/-Volt), and V_{in} is VCO input voltage. Assume the PLL is locked initially, and the reference frequency changes to 10°. According to Equation 2.5, the amplitude of error signal, v_{pd}, then increases to 0.09, with assumption K_{pd} is unity. The output frequency increases according to Equation 2.6, hence the output phase changes linearly. As a result the phase error decreases, and the amplitude of the error signal also decreases. This process continues until the phase error becomes zero.

A linear PLL is an ideal PLL. Unfortunately, real components in a PLL are non-linear. Therefore, a linear PLL is not applicable in real design, but only applicable for approximate linear analysis.

2.2.2 All-digital PLL

An all-digital PLL (ADPLL) is developed using digital circuits, which are a phase-to-digital (P2D) converter acting as phase detector, digital loop filter, digitally controlled oscillator (DCO), and a frequency divider. All signals within the system are digital except for the DCO output. The phase-to-digital converter senses the phase difference between reference clock, f_{ref}, and divided DCO output and converts it to a digital format. This information is filtered by the digital filter and then is used to control the DCO.

Phase-to-digital converter

The phase-to-digital converter can be implemented in several ways, such as an RS flip-flop counter and a Hilbert transform. A common phase-to-digital converter in an ADPLL is a time-to-digital converter (TDC). Note that a TDC plays a very important role in the ADPLL as its resolution determines the ADPLL performance. A high resolution TDC is required to achieve a low in-band phase noise. According to Staszewski *et al.*

(2004), the phase noise spectrum at the ADPLL output due to the TDC timing quantization is

$$\mathcal{L} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{\text{inv}}}{T_{\text{v}}}\right)^2 \frac{1}{f_{\text{ref}}}, \tag{2.7}$$

where Δt_{inv} is a single inverter delay, which is the TDC resolution. The shorter delay time, the higher TDC resolution, resulting in an improved noise performance. The noise spectrum also depends on the VCO output period, T_{v}, and reference frequency, f_{ref}.

Digital Controlled Oscillator

For the DCO, if a ring oscillator based DCO is used, tuning can be performed by digitally turning on and off the bias current source. If an LC based DCO is employed, frequency tuning is carried out by switching on and off the tank capacitors.

The advantages of an ADPLL are small area, low voltage, scalability, and ease of redesign with process changes or scaling (Kratyuk *et al.* 2007). In addition, a digital implementation of a PLL eliminates the noise-susceptible analog control voltage for the VCO. Unfortunately, the operating frequency for an ADPLL is limited. Although much work has been carried out to implement an ADPLL, the maximum operating frequency reported is only up to 3.5 GHz (Temporiti *et al.* 2010, Staszewski *et al.* 2005). The limitation is due to the resolution of the TDC. A high resolution is necessary to achieve a low phase noise. Thus, a very short TDC quantization time is required. Due to process variation, the time quantization can be affected, resulting in a poor phase noise performance.

2.2.3 Digital PLL

Another type of PLL is a digital PLL. It is called a digital PLL because the phase detector is digitally implemented, whilst the rest is analog. The frequency divider also may be constructed using digital circuitry.

Phase detector

The phase detector can be implemented as an XOR logic gate, JK flip-flop or phase/frequency detector (PFD). Phase tracking for an XOR phase detector is limited between

$-\pi/2 < \theta_e < +\pi/2$. Meanwhile, a JK flip-flop phase detector tracks the phase different between $-\pi < \theta_e < +\pi$. The PFD is commonly used as it tracks the phase error between $-2\pi < \theta_e < +2\pi$. Thus, a PFD offers a much wider pull-in range, which guarantees PLL acquisition.

Figure 2.3 shows a PFD with a tri-state output in a digital PLL. When the UP signal is ON, the capacitor in the loop filter is charged. On the other hand, switching ON the DN signal discharges the capacitor. If both UP and DN signals are OFF, where the output is in high impedance, the capacitor in the loop filter holds the charge, hence the voltage across the capacitor remains unchanged.

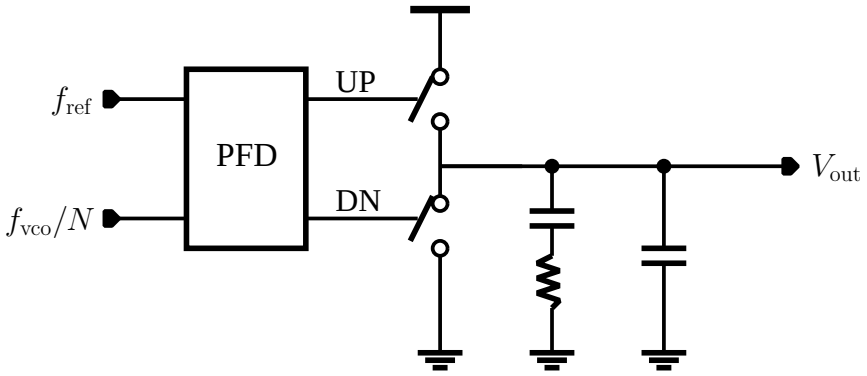


Figure 2.3. A tri-state PFD in a digital PLL. The UP and DN switches control charging and discharging activity of the capacitor in the loop filter, hence determine the VCO tuning voltage.

A drawback of this topology is that the system is vulnerable to supply voltage variation. In order to eliminate the power supply noise coupling to the circuits, a charge pump circuit is used. A charge pump PLL has similar components to a digital PLL except it has a charge pump circuit to replace the tri-state after the PFD. Further detail on this type of PLL is discussed in Section 2.4.

2.3 Phase-Locked Loop Architectures

As a frequency synthesiser, a PLL must be able to provide a range of different output frequencies, depending on how many channels are in the system. This may be carried out by a few techniques, such as combining two or more PLLs or adjusting the divider ratio in the loop. The latter technique is more popular (Floyd 2008, Lee *et al.* 2008, Woo *et al.* 2008), because it saves extra componentry.

There are several architectures that achieve the required dividing ratio, such as the integer-N, fractional-N or hybrid architectures (combination between integer-N and fractional-N). Integer-N and fractional-N architectures are the most common reported. This section provides further discussion on these two architectures.

2.3.1 Integer-N

The integer-N architecture provides channel spacing at the reference frequency or at multiples of the reference frequency. For example, if the reference frequency is 1 MHz, the possible channel spacings are 1 MHz, 2 MHz, 3 MHz, etc. The architecture is implemented by adding a prescaler before the PFD to determine the PLL dividing ratio. The prescaler is constructed by using a dual-modulus divider, a program counter (P counter), and a swallow counter (S counter), as shown in Figure 2.4. The dual-modulus divider is controlled by the P and S counters. Prescaler division ratio, M is given by

$$M = N \times P + S \,, \tag{2.8}$$

where N is dividing ratio, P is program counter value, and S is swallow counter value. The S counter value depends on the selected channel.

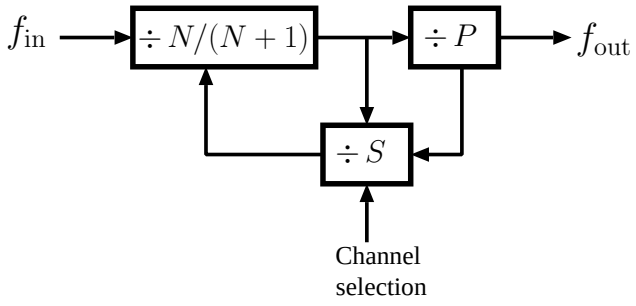


Figure 2.4. Prescaler in an integer-N architecture. The prescaler is implemented by three main components, which are a dual-modulus divider, a P counter, and an S counter. Channel selection is given by a digital signal that represent the channel number.

When the circuit begins at the reset state, the S counter is loaded with a value determined by channel number and the P counter set to full. The prescaler divides the VCO output signal by $N + 1$ until S counter is zero. Then, the prescaler divides the VCO output by N for $P - S$ times, until the P counter is zero. The process is repeated continuously.

Current low GHz RF communication has a limited channel bandwidth. Therefore, the system can only afford a small channel spacing. Because of the integer-N architecture, the output can only be integer multiples of the reference frequency, hence a small reference frequency is required for a small channel spacing. This increases the dividing ratio, hence increasing the output phase noise in the PLL. In addition, due to loop stability issues, the loop bandwidth is limited to 10% of the reference frequency. A lower reference frequency causes a smaller loop bandwidth, resulting in a longer settling time. Because of this limitation, an integer-N architecture is not popular in low GHz RF communication. Instead, a fractional-N architecture is used because the output frequency can be a fraction of the reference frequency. On the other hand, 60 GHz RF communications has a very wide channel bandwidth: 7 GHz that extends from 57 GHz to 64 GHz. Therefore, the integer-N architecture is suitable for a 60 GHz system (Scheir *et al.* 2009, Lee *et al.* 2008, Herzel *et al.* 2008a, Floyd *et al.* 2006).

2.3.2 Fractional-N

Fractional-N PLL provides channel spacing at a fraction of the reference frequency. Therefore, a higher reference frequency can be used, and the dividing ratio can be reduced. This can helps to improve phase noise performance (Rhee *et al.* 2000). The output frequency in fractional-N PLL is given by

$$f_{\text{out}} = f_{\text{ref}} \left(N + \frac{K}{F} \right) , \tag{2.9}$$

where f_{out} is VCO output frequency, f_{ref} is reference frequency, N is dividing ratio, K is channel number, and F is fractional resolution with respect to the reference frequency. Here, N, K and F are integer numbers. Channel spacing for the system is given by f_{ref}/F. For example, if the output frequency is 100.01 MHz and channel spacing 10 kHz, a reference frequency at 100 kHz with fractional resolution, $F = 10$, can be used in a fractional-N PLL. The dividing ratio N is only 1000. For integer-N PLL, the reference frequency must be the same as reference frequency, which is 10 kHz. Therefore, the dividing ratio will be 10,001, which is about 10 times higher than in a fractional-N PLL. A small dividing ratio in a fractional-N can help reduce phase noise at the output (Glisic and Winkler 2006).

Implementation of a fractional-N architecture is almost similar to an integer-N architecture. The only difference is the divider component. In a fractional-N PLL, a digital

accumulator is used to control the dual-modulus divider. The main problem in the fractional-N PLL is the presence of fractional spurs that appear at fractional multiples the reference frequency. A common technique to minimise fractional spurs is by using a $\Delta\Sigma$ modulator to replace the digital accumulator (Kenny *et al.* 1999, Riley *et al.* 1993).

2.4 Charge Pump PLL Component

A charge pump PLL is a popular frequency synthesiser in RF transceivers. The components in the charge pump PLL are similar to the digital PLL except for the tri-state output, which is replaced by a charge pump circuit. This circuit helps the loop to have improved immunity to power supply noise. Figure 2.5 shows the components of a charge pump PLL, which are a reference clock, phase/frequency detector (PFD), charge pump, low pass filter, VCO, and frequency divider.

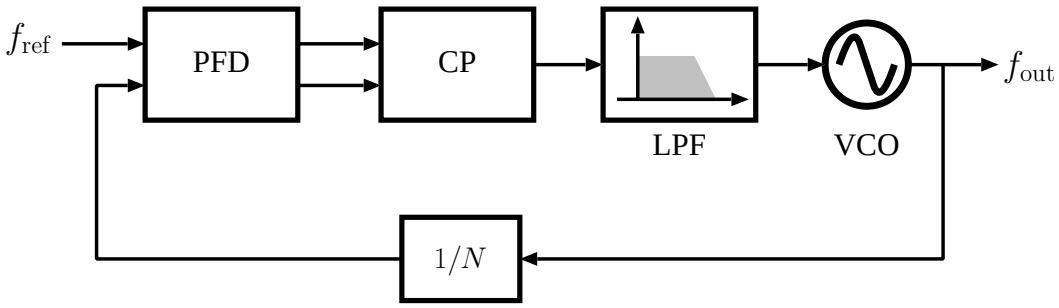


Figure 2.5. A charge pump PLL. It consists of a reference clock (f_{ref}), phase/frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage-controlled oscillator (VCO), and frequency divider ($1/N$). This type of PLL is similar to a digital PLL, except for the charge pump circuit in this PLL replace the tri-state circuit in the digital PLL. The charge pump circuit helps PLL to improve immunity to power supply noise.

2.4.1 Reference clock

A crystal oscillator is commonly used as a reference clock in a PLL, as it provides an outstanding noise performance. Phase noise contributed by a crystal clock is very low compared to other components in a PLL. Hence, reference noise contribution can be neglected.

However, not all the desired reference frequencies are available from crystal oscillators in the market. Therefore, many PLLs use a crystal clock together with a frequency

divider in order to obtain the desired reference frequency. On the other hand, the phase noise contributed by the divider has to be considered.

In this work, a reference clock from a crystal oscillator is used. This is because a noise contribution from this source is negligible when compared with noise contributions from other PLL components.

2.4.2 Phase/frequency detector

A phase/frequency detector (PFD) is used as a phase detector in a charge pump PLL. Here, a PFD is implemented using two resettable edge triggered D flip-flops and an AND gate as shown in Figure 2.6. The clock for one of D flip-flop is from reference signal f_{ref}, while the second uses the divided output signal f_{out}/N as a clock, while the inputs for both flip-flops are connected to a logic high. The PFD outputs are named UP and DN.

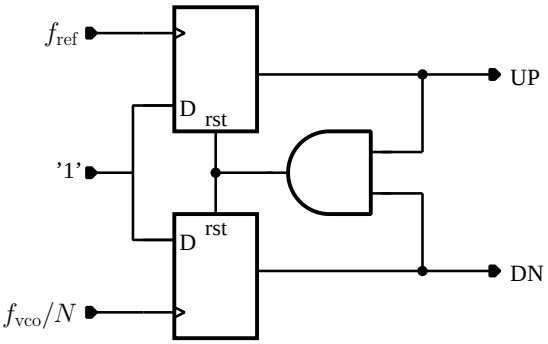


Figure 2.6. Phase/frequency detector (PFD). The PFD is constructed from two D flip-flops, where their inputs are connected to the reference frequency, f_{ref}, and divided output frequency, f_{out}/N, respectively. The AND gate provides a delay in the reset path.

As shown in the timing diagram in Figure 2.7, if f_{ref} is leading f_{out}, UP signal is HIGH until f_{out} goes HIGH. When both PFD outputs are HIGH, the AND gate activates the reset of both flip-flops. Thus, the UP and DN signals remain HIGH simultaneously for a duration given by total delay through the AND gate and reset path of the flip-flop. On the other hand, when f_{out} leads f_{ref}, the DN signal is HIGH until f_{ref} turns HIGH. The input-output characteristic of the PFD is shown in Figure 2.8. The PFD can track the phase difference up to $\pm 2\pi$. This helps the PLL to have an improved acquisition range.

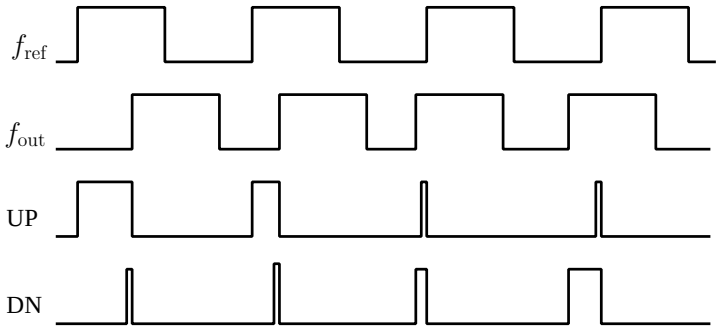


Figure 2.7. PFD timing diagram. The PFD inputs, f_{ref} and f_{out} is from reference oscillator and divided VCO output, respectively. Meanwhile, UP and DN are the PFD output signals. Here, UP is HIGH when f_{ref} leads f_{out} and DN is HIGH when f_{out} leads f_{ref}.

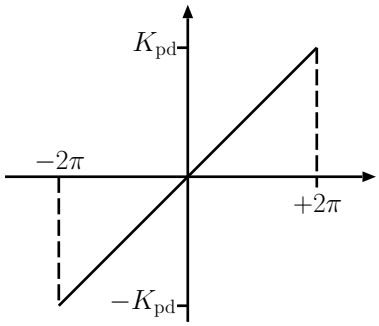


Figure 2.8. PFD input output characteristic. The PFD is able to track phase difference in the range -2π and $+2\pi$, resulting in improved acquisition.

2.4.3 Charge pump

The charge pump together with the loop filter converts the phase error information provided by PFD into a voltage. Figure 2.9 shows a charge pump circuit. It consists of two current sources, namely, I_{up} and I_{dn} together with a switch for each current source. The switches are controlled by UP and DN signals from the PFD. The UP signal controls I_{up}, while the DN signal controls I_{dn}. The current output from the charge pump is filtered by a low pass filter before it goes to the VCO.

The charge pump can be implemented in three different topologies, namely, a source switch charge pump, a drain switch charge pump, and a gate switch charge pump (Magnusson and Olsson 2003, Rhee 1999). Figure 2.10(a) shows a drain switch charge pump. The switches are at the drain terminals of the current source. If the DN switch is OFF, the drain terminal of M1a is pulled to ground. When the switch turns ON, the drain terminal voltage increases the loop filter voltage. During this time, M1a is in a linear region and a high peak current is generated caused by the voltage difference of

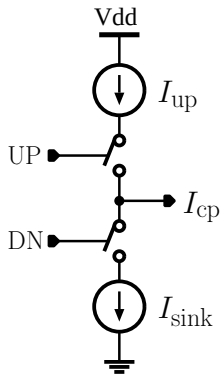
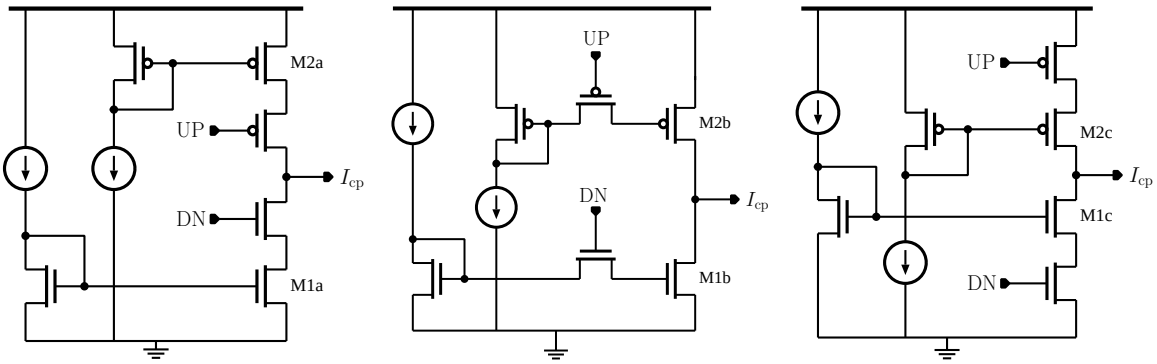


Figure 2.9. A basic charge pump schematic. Here, I_{up} and I_{dn} are current sources, and I_{cp} is the output current. The loop filter converts the output current into voltage. Here, the UP and DN switches are controlled by the PFD output.

two series turn-on resistors from M1a and DN switch (Rhee 1999). The same situation also occurs when the UP switch turns on. The current spikes between the UP and DN switching are not matched as the current varies with the output voltage due to channel length modulation.



(a) Drain switch charge pump (b) Gate switch charge pump (c) Source switch charge pump

Figure 2.10. Charge pump topology. Three different charge pump topologies are given, and discussed in the text.

Another charge pump topology is the gate switch charge pump as shown in Figure 2.10(b). In this topology, M1b and M2b either OFF or in saturation mode. Therefore, this topology does not have a current spike problem. However, switch transistors connected to the gate terminals increase the gate capacitance of M1b and M2b, which limit the operating frequency of the charge pump.

The commonly used charge pump topology is the source switch type. The UP and DOWN switches are at the source terminals of the current source circuit as shown in Figure 2.10(c). This topology can handle a higher operating frequency compared to

gate switching topology. It also minimises the current spike while switching, as M1c and M2c are always in saturation mode.

Besides these three topologies, a few techniques have been used in charge pump design in order to improve its performance, such as current steering, differential charge pump, and charge pump with active amplifier. However, the source switch charge pump is the most popular due to its simple structure, and low power consumption, for a comparable switching time (Rhee 1999).

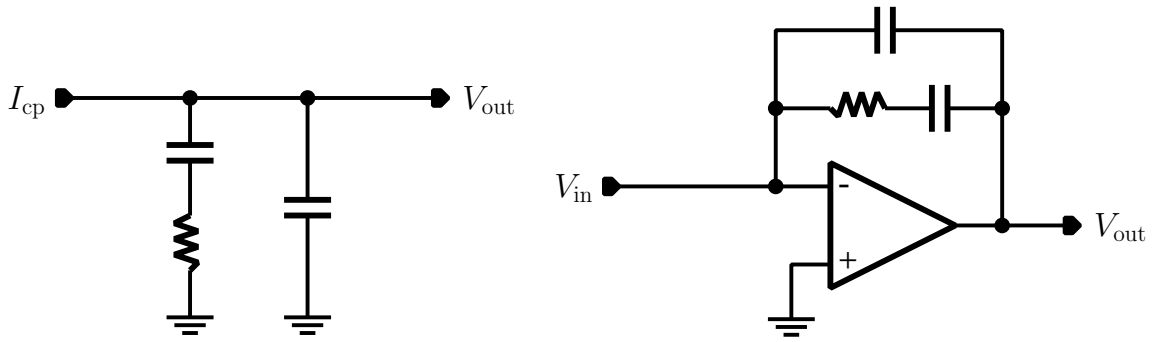
2.4.4 Loop filter

The loop filter determines the loop bandwidth in the PLL. It is constructed using a low pass filter. Two options are available for the loop filter implementation, passive or active. Each type has its own pros and cons. Passive filter implementation is simpler and consumes low power since only passive components, such as resistors and capacitors are employed. However, in a charge pump PLL, the voltage range is limited in order to maintain the current source in the saturation region when the PLL is locked. The voltage range for the charge pump output is $V_{cp} - 2V_{sat}$. This issue is a limitation in low voltage technology because only a very small tuning voltage for the VCO is available.

The voltage limitation of passive filters can be solved by using active filters. These filters use an op-amp together with resistors and capacitors. The op-amp adds extra gain to the loop. Normally, an active filter is used when a large VCO tuning voltage is required. However, the active filter consumes more power and die area. It also increases the complexity of the design. Therefore, many PLL designers prefer to use a passive filter in contrast to an active filter.

Figure 2.11 shows second order passive and active filters. A higher order loop filter can be used. It offers improved reference spur attenuation. However, it has to be designed carefully because it affects the loop stability. For a higher order filter, extra poles are added to the filter transfer function. The extra pole degrades the phase margin, hence decreases the loop stability margin (Thompson and Brennan 2005).

This work concentrates on a third order passive filter, because it offers an improved attenuation compared to a second order filter. Further discussion is presented in Chapter 7.



(a) Passive filter (b) Active filter

Figure 2.11. Second order low pass filter. Passive filters are commonly used in charge pump PLLs compared to active filters. This is because op-amp in the active filter increases the circuit power consumption, die area, and noise.

2.4.5 Voltage-Controlled Oscillator

A voltage-controlled oscillator (VCO) can be implemented in several ways. Two types of oscillator that are most common are ring oscillators and LC tank oscillators. A ring oscillator is implemented by connecting several inverters in a closed loop such that the sum of phase delays are an integer multiple of 2π. The advantage of a ring oscillator is that it can provide a large tuning range. However, it suffers from poor phase noise performance. Also, active devices in the ring oscillator consume high power.

In contrast, an LC tank oscillator uses passive devices, an inductor and capacitor to form a resonant circuit. Therefore it consumes less power compared to ring oscillator. Furthermore, an LC oscillator gives improved noise performance, which makes this type of oscillator more common in an RF frequency synthesisers. There are a number of architectures for implementing an LC tank oscillator, such as cross-coupled, Colpitts, and Hartley oscillators. A cross-coupled configuration is commonly used. Figure 2.12 shows a cross-coupled LC tank oscillator. The drawback of an LC tank oscillator is that it consumes a large die area.

The resonant LC cross-coupled oscillator can be represented as an RLC parallel circuit as shown in Figure 2.13. In an ideal LC tank, there is no resistance. However, in the real implementation, the inductor and capacitor suffer from resistive components, which is represent as a lumped R_p in the Figure 2.13. In order to maintain oscillation, a negative resistance has to be added in parallel. The negative resistance concept is further discussed later in this section. The resonance frequency of the LC tank, f_{res}, is

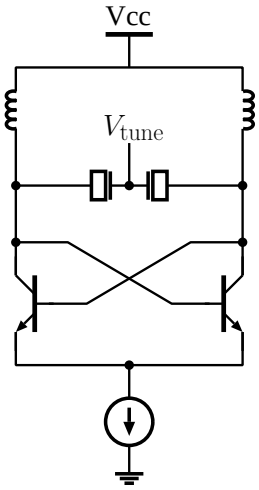


Figure 2.12. Differential cross-coupled LC oscillator. This topology is common in PLL based frequency synthesisers due to improved noise performance. The differential BJT pair provides a negative resistance to the LC tank, to sustain oscillation.

given by

$$f_{\text{res}} = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}\,. \tag{2.10}$$

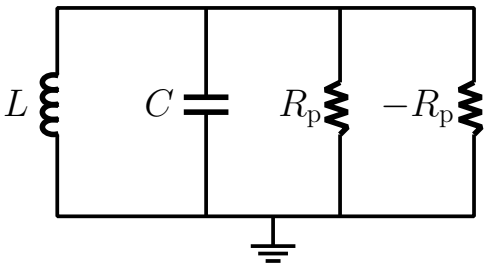


Figure 2.13. An RLC parallel circuit. Resistive components of the inductor and capacitor is presented as a parallel resistance, R_{p}. A negative resistance, $-R_{\text{p}}$, is added to compensate the loss from R_{p}.

Negative g_m oscillator

In the LC tank circuits, an infinite impedance is required to sustain oscillation. In other words, the quality factor, Q, is infinity in the LC tank. However, the resistive component in the inductor and capacitor limits the quality factor and makes the resonance frequency dependent on this resistance. The resistive component is mainly contributed

by the inductor (Do Vale Neto 2004) and can be simplified into an equivalent parallel resistance, R_p and is given by

$$R_p \approx Q^2 R_s \,, \tag{2.11}$$

where R_s is inductor and capacitor series resistance. This resistive component causes an energy loss in the tank, hence damping the output signal and eventually stopping the oscillation. In order to sustain oscillation, the same energy loss in the tank is required to be compensated. Energy source devices, BJTs or MOSFETs can be used to compensate the energy loss. These devices provide a negative transconductance (or $-g_m$) to compensate for the energy loss by the parallel resistance. Figure 2.14 shows BJT components as the negative resistance in a differential LC tank circuit. Impedance of the circuit, R_{in}, viewing from emitter terminals of the BJTs is $-2/g_m$.

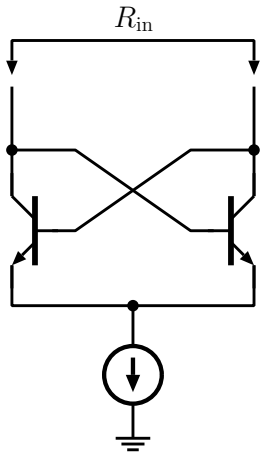


Figure 2.14. A $-g_m$ oscillator. The cross-coupled BJT provides a negative resistance to compensate the resistive loss in the LC tank.

In order to start oscillation, the negative g_m must be equal or larger than the parallel resistance from the LC tank circuit. In the real circuit, the thermal noise from resistive components helps the circuit to initiate oscillation.

Frequency tuning

As shown in Equation 2.10, output frequency of an LC tank VCO depends on inductance and capacitance of the LC tank circuit. By varying these values, a range of output frequencies can be achieved. A common practice for implementing this is to use a varactor, which is a voltage controlled capacitance device. Changing the voltage, varies the device capacitance, thus changes the VCO output frequency.

A commonly used varactor is the pn-junction diode connected in reverse bias. However, a diode varactor has a small tuning range due to its small depletion capacitance. Also, it has a non-linear relation between the control bias voltage and the depletion capacitance. Furthermore, a varactor diode has a poor quality factor. The quality factor drops quickly as a forward-bias is approached, thus impairs the diode tuning range capability.

Another type of varactor is the MOS varactor. The MOS varactor can be operated in inversion or accumulation mode. For inversion mode (also known as an I-MOS varactor), the varactor can be implemented in p-channel (PMOS) or n-channel (NMOS). For PMOS, the bulk terminal is connected to the power supply voltage, and the voltage at the gate terminal determines the capacitance. On the other hand, for NMOS, the bulk terminal is connected to ground, and also the voltage on the gate terminal determines the capacitance. The NMOS inversion varactor has an advantage of a lower parasitic resistance than the PMOS varactor (Andreani and Mattisson 2000). However, since NMOS cannot be implemented in a separate p-well, it is more sensitive to substrate-induced noise (Andreani and Mattisson 2000).

A commonly used MOS varactor makes use of the accumulation mode, and is also known as an A-MOS varactor. The A-MOS varactor provides a larger tuning range and lower parasitic resistance (Andreani and Mattisson 2000). The varactor is a combination of an n-channel and p-channel MOSFET, with n+ doping at the drain and source terminal placed within an n-well, as shown in Figure 2.15.

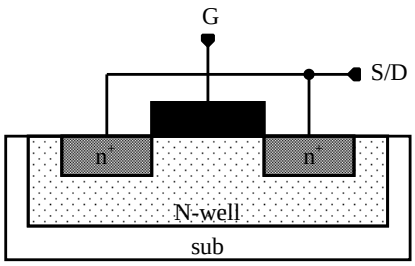


Figure 2.15. Accumulation MOS varactor. The n^+ doping is at the drain and source terminals, which is connected together, and is placed within an n-well. The A-MOS varactor gives rise to a larger tuning range and lower parasitic resistance compared to a pn-junction varactor, hence it is more common in a VCO design.

Recently, active varactors have been introduced to overcome the tuning range limitation in a passive varactor. Two approaches have been used in active varactor that are (i) the Miller-effect (Stadius *et al.* 2001, Lont *et al.* 2009, Chen and Chiu 2010), and (ii)

the balance variable impedance converter (Chen and Wu 1998). In the Miller theorem based varactor, a voltage amplifier with a capacitive feedback as shown in Figure 2.16 is used as a varactor.

The effective capacitance, C_{eff} is given by

$$C_{\text{eff}} = C(1 - A) \; . \tag{2.12}$$

The effective capacitance is proportional to the voltage gain, A. Therefore, a large tuning range can be achieved by implementing a large gain amplifier. The highest reported tuning range for a Miller theorem based varactor is 30% as reported in Stadius *et al.* (2001).

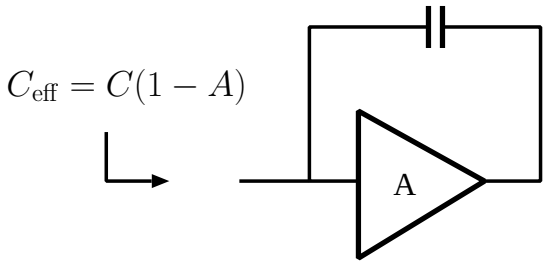


Figure 2.16. A Miller theorem based varactor. A large tuning range can be achieved using this type of varactor by enlarging the voltage gain of the amplifier (A).

Another approach for active varactor implementation is by using a balanced variable impedance converter (VIC). This technique was introduced by Chen and Wu (1998). The capacitance is tuned by the amount of current flowing through it. The current flow is controlled by a current steering circuit as shown in Figure 2.17. The transistor pairs, Q_{1p} & Q_{1m} and Q_{2p} & Q_{2m}, determine the current flowing through the capacitor, depending on their input voltages, V_c^+ and V_c^-. Therefore, the equivalent capacitance of the VIC varactor is determined by the voltage input, V_c. If Q_{1p} and Q_{1m} are on, while Q_{2p} and Q_{2m} are off, the capacitance is C. On the opposite site, where the current flows in reverse direction, the capacitance is $-C$. When all Q_{1p}, Q_{2p}, Q_{1m}, and Q_{2m} are on and in balance, no current flows through the capacitor. Hence, the capacitance value is only from parasitics of the transistors.

Although an active varactor promises a much higher tuning voltage, phase noise is still a significant issue. A large tuning range active varactor have been reported with low noise performance (Lont *et al.* 2009, Stadius *et al.* 2001). In addition, an active varactor increases the power consumption and complexity of the oscillator design. Therefore,

Figure 2.17. A VIC connected to an LC cross-coupled VCO. Differential voltage input, V_c^+ and V_c^-, determine the equivalent capacitance of the variable impedance converter (VIC), hence determine the VCO output frequency. Here, Q_4 and Q_5 act as a level shifter for the VIC (Chen and Wu 1998).

a passive varactor is still common in VCO design as it offers lower complexity and improved noise performance compared to active varactor.

2.4.6 Frequency divider

The VCO output frequency is normally much larger than the reference frequency. Therefore, a series of frequency dividers (also known as a prescaler) are used to decrease the VCO output frequency to match the reference frequency. The design of first frequency divider after the VCO is crucial due to high operating frequency. Furthermore, current low-supply voltage technology makes the design even harder. Frequency dividers are also used for the generation of quadrature output signals in the PLL.

A frequency divider can be implemented in digital or analog. In digital implementation, two D flip-flops are connected in series as shown in Figure 2.18. This topology is called master-slave, where the first flip-flop is called the master, while the second is called the slave. The inverted output of the slave is fed back to the master input.

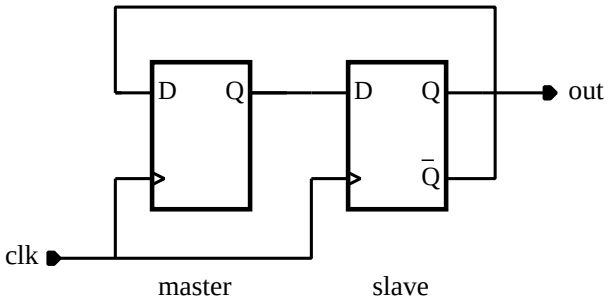


Figure 2.18. A master-slave frequency divider. This divide-by-two circuit is implemented using two D flip-flops. The output frequency is half of the clk frequency.

The D flip-flop in the master slave can be implemented in static or dynamic logic, but the static implementation is more common. The circuit can be implemented in CMOS logic. For high speed operation, current mode logic (CML) circuit is used. The differential digital logic with a smaller voltage swing in CML helps to increase the divider operating frequency. Note that CML can be implemented in FET or BJT technology. An implementation of CML in FET technology is called source coupled logic (SCL) and a bipolar implementation is called emitter coupled logic (ECL).

D flip-flops in a CML implementation require many transistors. The number of transistors can be reduced by using a dynamic implementation. A commonly used dynamic implementation is true single-phase clocking (TSPC).

A digital frequency divider has an operating speed limitation. Analog divider can provide a higher operating frequency. An analog divider, namely, a regenerative frequency divider, based on injection locking phenomenon was introduced in Miller (1939). A regenerative frequency divider consists of a mixer and a loop filter as shown in Figure 2.19. The input signal, f_{in}, is mixed with the output signal, f_{out}, where the output signal frequency is half of the input frequency. The mixer produces output at frequency $nf_{in}/2$, where n is an odd number. However, only $f_{in}/2$ is taken as the output, where other frequencies are filtered out.

2.5 PLL for 60 GHz RF Transceiver

A charge pump PLL is widely used as a frequency synthesiser in RF transceivers as its performance is improved compared to other types of PLL. The charge pump PLL

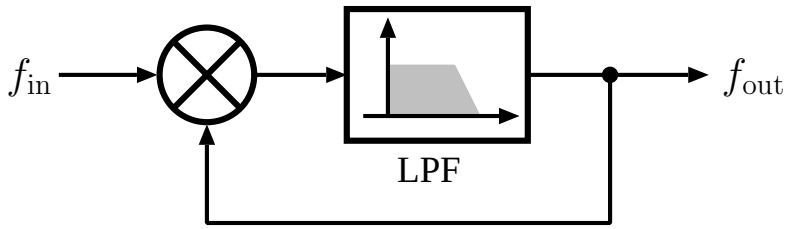


Figure 2.19. A regenerative frequency divider. The output frequency, f_{out}, which is half of the input frequency, f_{in}, is mixed with the input frequency resulting in signals at $nf_{\text{in}}/2$, where n is an odd number. The low pass filter only passes $f_{\text{in}}/2$ to the output.

implementation for a 60 GHz RF transceiver system has many issues related to architecture selection and circuit design technique. This section reviews some issues in the PLL design for the 60 GHz transceiver.

Two types of transceiver can be used, namely, direct conversion or superheterodyne. A few studies have been carried out for a direct conversion 60 GHz transceiver (Marcu *et al.* 2009, Mitomo *et al.* 2008, Razavi 2005, Bosco *et al.* 2004). Direct conversion appears to be a good choice for a 60 GHz system due to its simplicity, low cost and low power consumption (Laskar *et al.* 2005). However, self mixing from LO leakage is a serious issue to consider. In addition, a low noise high frequency VCO operating around 60 GHz, with wide tuning range to cover the whole channel bandwidth is challenging to design.

Alternatively, a superheterodyne architecture can be chosen for the 60 GHz transceiver (Razavi 2008, Reynolds *et al.* 2006, Howarth *et al.* 2005). Normally, dual IF conversion is chosen where the RF signal around 60 GHz is down-converted to a lower IF before it is down-converted again to the baseband. A high IF frequency is chosen, so that the image frequency is located far away from the RF, making the image filter easier to implement. In Floyd (2008), 12 different IF possibilities are presented together with their frequency planning for each proposed IF. Meanwhile, in Sun *et al.* (2007) an IF at 5 GHz is chosen because it is compatible with the 802.11a WLAN standard. On the other hand, Thangarasu *et al.* (2009) proposed to reuse the standard architecture for car technology at 24 GHz as IF in order to reduce the development cost. Our work uses a dual conversion superheterodyne architecture with the first IF is at 6/7 of the RF signal, and the second IF is at 1/7 of the RF. The IF is chosen so that the image frequency, which is located at 2IF away from the RF frequency, is large enough to ease the image filter implementation. The receiver architecture is shown in Figure 2.20.

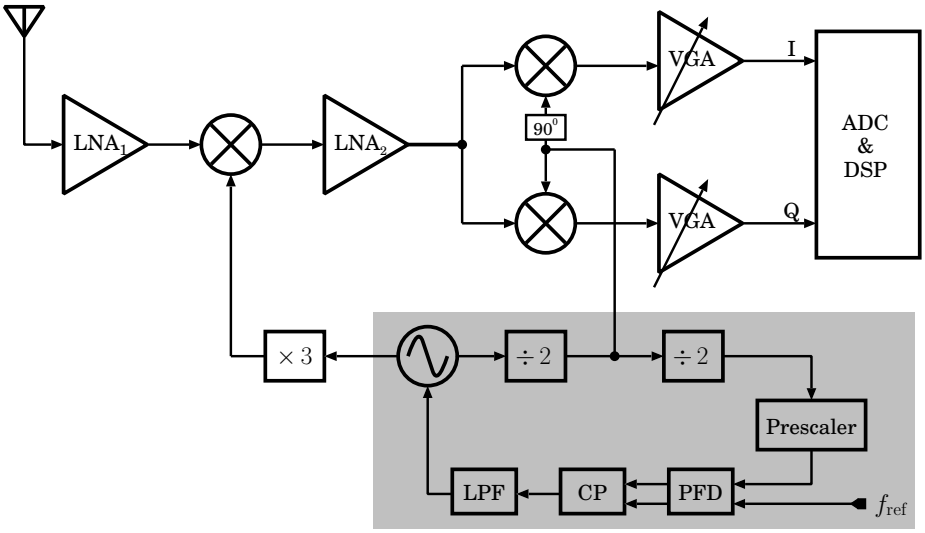


Figure 2.20. A double-conversion super-heterodyne architecture. This receiver architecture is proposed for this work. Although, this work only concentrates on the PLL based frequency synthesiser, which is shown in the grey shaded area.

2.5.1 PLL planning

As mentioned in Section 2.3, an integer-N architecture is chosen for this work. For this purpose, a 71.43 MHz reference frequency is used. The frequency planning is shown in Table 2.1. The PLL needs to provide two different frequencies for the transceiver in this work. The first IF is at 6/7 of the RF signal, while the second IF is at 1/7 of the RF signal. One way to implement this is to design a PLL operating at the first IF frequency, and obtain the second IF by dividing the PLL output by 6. In order to do this, a VCO operating at around 51 GHz has to be designed. A good performance VCO with high operating frequency is harder to design compared to a lower frequency counterpart. In addition, design of the first frequency divider after the VCO is also an issue. The divider must operate at the VCO output frequency. Normally, a high operating frequency divider consumes large current, hence increases the power consumption of the circuit. Also, a higher supply voltage is required for the divider circuit (Floyd 2008). More than one supply voltage on a single chip is not a practical solution.

Alternatively, a PLL with a lower operating frequency can be designed. The PLL output is then increased by a frequency multiplier. In this work, the PLL output must be combined with a frequency tripler in order to obtain the first IF frequency. The second IF can be achieved by obtaining half of the PLL output. The advantage of this architecture is that a lower frequency VCO can be used. For this work, the VCO is only

Table 2.1. Frequency planning. The first and second IF is 6/7 and 1/7 of the RF signal, respectively. The VCO frequency is 1/3 of the first IF.

RF (GHz)	IF_1 (GHz)	IF_2 (GHz)	f_{VCO} (GHz)
57	48.858	8.143	16.286
58	49.715	8.286	16.572
59	50.572	8.429	16.857
60	51.430	8.572	17.143
61	52.287	8.714	17.429
62	53.144	8.857	17.715
63	54.000	9.000	18.000
64	54.858	9.143	18.286

required to operate around 17 GHz, which is much lower compared to the above architecture where 51 GHz is required. Therefore, an improved noise performance can be achieved and also simplifies the frequency divider design in the PLL. On the other hand, the disadvantage of this architecture is the extra frequency multiplier circuit after the PLL also introduces noise. The noise from the multiplier degrades the PLL output performance by $20\log(N)$ (in dB), where N is the multiplication factor. In this case, when a tripler is used ($N = 3$), this results in 9.5 dB noise degradation from the PLL output.

2.5.2 PLL simulation challenge

Simulating the PLL is very time consuming since the difference between the output frequency and the reference frequency is large. The transistor level phase noise simulation time can be decreased by simulating phase noise of each component separately. Then, the noise magnitude from each component is added in order to obtain the PLL phase noise. This method helps to significantly reduces the simulation time. Detail discussion on the PLL phase noise is given in Chapter 3.

For the transistor level reference spur simulation, a very long simulation period is required, as the reference spur can only be captured after the PLL is locked. To save the simulation period, a behavioural model simulation can be used. Matlab and Verilog can be used for PLL behavioural simulation. However, according to the literature, only phase noise is considered in the PLL behavioural model. Therefore, a reference spur

simulation using a behavioural modelling is proposed in our work. Reference spurs can be modelled by including all the parameters that contribute to the spur magnitude in the model. Details regarding the PLL behavioural simulation is presented in Chapter 5.

2.5.3 PLL design challenge

A PLL consist of 5 different circuit blocks, which are designed separately. Designing a circuit operating at high frequency is a great challenge. In addition, a low supply voltage limitation and a low power requirement further increases the design challenges. The VCO and the first frequency divider are circuits that operating at high frequency. Design issues and techniques for these circuits are reviewed in the following sub-sections.

VCO design

In a 60 GHz system, a wide tuning range VCO is required to cover 7 GHz bandwidth. Since a dual-IF conversion superheterodyne transceiver is considered in our work, a lower tuning range can be used. Referring to Table 2.1, a VCO operating between 16.3 GHz and 18.3 GHz with 2 GHz tuning range is required. The large tuning range requires a large varactor. Also, with a small tuning voltage (from charge pump), a high VCO gain is necessary to cover the whole frequency range. For example, a 1 V tuning voltage makes the VCO gain 2 GHz/V but a 2 V tuning voltage only makes the VCO gain at 1 GHz/V. The voltage gain represents VCO sensitivity to the input noise. Therefore, a lower VCO gain is preferable because the VCO is less sensitive to the input noise.

One way to tackle the high VCO gain issue is by using switched capacitors together with a small varactor as shown in Figure 2.21 (Floyd 2008). One or more capacitors are connected in parallel with varactor. MOS switches are used to control the capacitor connection to the VCO circuit. If the switch is ON, the capacitor is connected to the VCO, hence increases capacitance in the LC tank, consecutively decreases the VCO output frequency. Otherwise, if the switch is OFF, the capacitor is disconnected from the VCO, resulting in a lower capacitance in the tank, thus increases the VCO output frequency. Therefore, the VCO output frequency depends on how many switched capacitors are on. Since the switched capacitors help to increase or decrease tank capacitance in the VCO, a smaller varactor with a lower VCO gain can be used. Therefore,

the VCO is less sensitive to the input noise, hence an improved noise performance can be achieved.

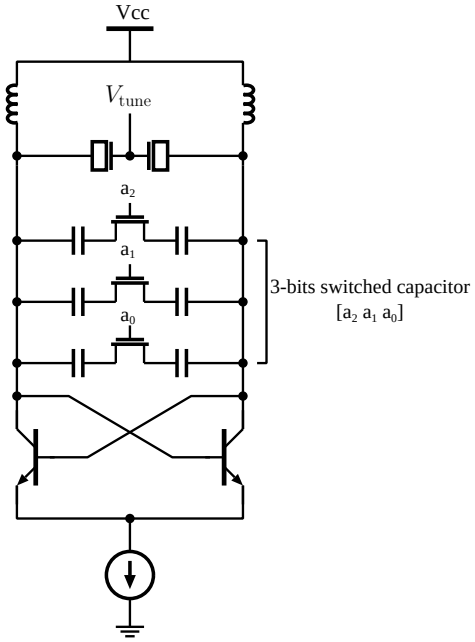


Figure 2.21. A switched capacitor VCO. Here, MOS switches, a_2, a_1, and a_0, control effective capacitance of the LC tank, hence determines the VCO output frequency. A smaller varactor can be used in a switched capacitor VCO, hence improve the phase noise. However, the MOS switch capacitances increase the tank capacitance, hence decreases the tuning range. Also, the circuit implementation increases the design complexity.

The switched capacitors approach appear to be a simple principle. However, the circuit implementation increases the design complexity. Each switched capacitor gives a different range of VCO output voltage. Therefore, the designers have to verify all the switching combinations can cover all the bandwidth. In addition, the MOS switches capacitance increase the tank capacitance, hence decrease the VCO tuning range. The switches resistance while it is ON also has to be considered.

Another approach to improve the VCO noise performance is by using two pairs of varactors as shown in Figure 2.22 (Herzel *et al.* 2008b, Winkler *et al.* 2005). One pair of varactors are much larger than the other pair. The large varactors are for a coarse tuning, while the smaller varactors are for a fine tuning. The varactors in the coarse tuning loop are connected to a large capacitor, while in the fine tuning loop, the varactors are connected to a low pass filter. Initially, when the PLL is in unlock state, the coarse tuning loop dominates the operation. Once the PLL is locked, the fine tuning loop takes over. Since the varactors that coupled into the fine tuning loop are very small, the VCO

is less sensitive to its input noise. On the other hand, noise from the coarse tuning loop is suppressed by the large capacitor that connected to the large varactors. The disadvantage of this approach is two charge pumps are required to provide tuning voltages for the two different varactors.

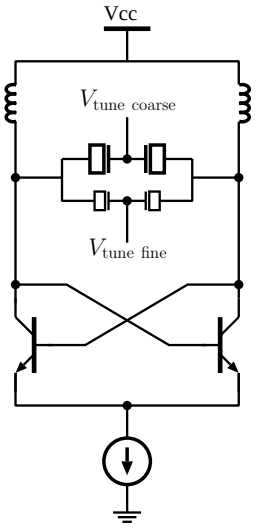


Figure 2.22. Coarse and fine tuning VCO. Two pairs different size varactors are used. The large varactor pair is for coarse tuning, while the small varactor pair is for fine tuning.

The VCO sensitivity to its input noise is also can be reduced by using a common mode noise rejection principle. This approach can be realised by using a differential tuning control signals as shown in Figure 2.23 (Kim *et al.* 2005, Fong *et al.* 2003). The VCO is implemented using two pairs of varactors, where one pair is connected to the anode, while another pair is connected to the cathode. Any common mode noise introduced by one of the varactor pair is cancelled out by the other pair, preventing the noise from modulating the varactor. In addition, the differential tuning helps to increase the VCO tuning voltage. The disadvantage of this technique is a differential charge pump and two sets of loop filters are required. These extra components increase the die area and also the power consumption.

Frequency divider

The first frequency divider that coupled into the VCO is required to operate at the high VCO output frequency. Designing the divider circuit with a low power supply limitation is a challenge. Implementing the PLL at lower frequency and combines it with a frequency multiplier can helps to simplifies the divider design. Another approach is to use a high supply voltage for the high operating frequency divider (Floyd 2008).

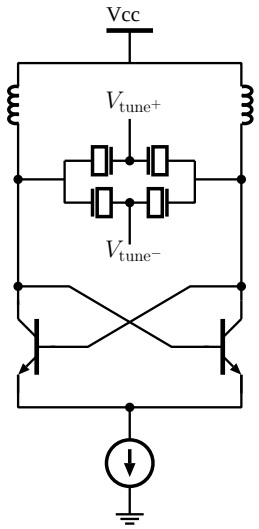


Figure 2.23. Differential tuning VCO. A differential tuning voltage is used to control two pairs of varactors. Note that V_{tune}^{+} is connected to the cathode, while V_{tune}^{-} is connected to the anode.

However, this approach requires a multi voltage power supply, which is not a practical design.

2.5.4 Reference spur issue

A periodic switching mechanism in the non-idealities PFD and charge pump circuits results in a periodic ripple in the VCO input voltage. In the frequency domain, this periodic ripples are visualised as signals at the reference frequency and at multiples of the reference frequency offsets from the VCO output signal, and it is known as reference spurs. As mentioned earlier, a large VCO gain is required in the PLL, results in the VCO sensitive to its input noise. Therefore, small ripples caused by the switching mechanism resulting in a high reference frequency. Further discussion on the reference spur is presented in Chapter 3.

2.6 Chapter Summary

In this chapter, the principle operation of a PLL is presented. Types of PLLs and the differences between each other are reviewed. In addition, PLL architectures are also discussed in this chapter. Since, a charge pump PLL is chosen for this work, a detailed explanation for each component in the charge pump PLL is provided. Also, the rationale behind choosing an integer-N architecture for this work is also explained. This

chapter also reviews challenges in designing a PLL based frequency synthesiser for a 60 GHz transceiver. The challenge includes PLL simulation, circuit design and also architecture selection.

A high performance PLL that can provide low noise and spur is very important in a PLL design. After reviewing the components that comprise a PLL, the noise contribution from each component has to be understand in order to minimise it. Thus, in the next chapter we examine noise contribution from each circuit to the PLL. Both types of noises, namely, phase noise and reference spurs are discussed. How these noise affects the RF communication is also provided.

Chapter 3

Phase-Locked Loop Noise

LOW noise is a key performance requirement in PLLs, which is measured at the VCO output. Nevertheless, the VCO is not the only component that contributes noise to the PLL, rather all components in the loop affect the PLL performance. This chapter briefly discusses phase noise theory and how the phase noise affects RF communication systems. The discussion is narrowed down to phase noise in PLLs, where both, random and periodic noise are included. Noise effects from each component and how the loop helps to filter the noise are explained.

3.1 Introduction

Ideally, the synthesiser output is a pure sinusoidal waveform and can be represented as a delta function in the power spectrum—also referred to as a Power Spectral Density (PSD). However, in reality the signal has disturbances from a variety of noise sources and it manifests as a skirt shape around the desired frequency in the power spectrum as shown in Figure 3.1.

There are two types of noise that we consider, namely, random and periodic noise. The random noise is generated by unavoidable sources in electronic components, such as thermal noise, shot noise, and flicker noise. These forms of noise manifest themselves in the frequency domain, and are commonly referred to as phase noise. In the time domain, the noise manifests itself as a timing jitter.

The periodic noise in PLLs arises from digital switching events in the PFD and charge pump. Non-idealities in the PFD and charge pump circuits cause a periodic signal disturbance in the VCO tuning voltage, hence produce a periodic noise on the VCO output. This periodic noise is referred to as *reference spurs*.

A synthesiser output performance is measured by the phase noise at a certain frequency offset from the desired carrier frequency. The phase noise at $\Delta\omega$ offset from the carrier is defined as the ratio of power at the offset frequency in 1 Hz bandwidth to the carrier power. The measurement unit is in dBc/Hz (Figure 3.1). The phase noise is commonly plotted on a frequency normalised log-log scale spectrum, where the plot represents noise power relative to the total power in the signal. The normalised spectrum plot is used in this thesis.

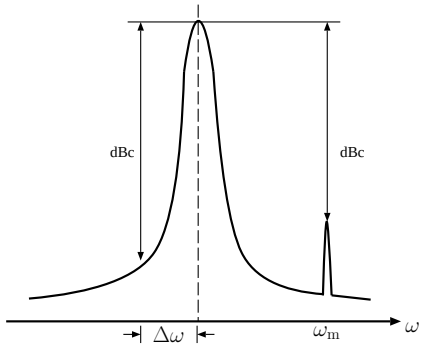


Figure 3.1. Power Spectral Density (PSD) of a synthesiser output. The arrow on the left shows the phase noise at $\Delta\omega$ offset from the carrier, meanwhile the arrow on the right shows sideband spurs.

This chapter briefly reviews a mathematical analysis of phase noise and periodic noise in Section 3.2. The effect of phase noise on RF communications is discussed in Section 3.3. Then, the discussion is narrowed down to the phase noise in PLLs as presented in Section 3.4. Section 3.5 presents the reference spur in PLLs, and followed by a summary in Section 3.6.

3.2 Phase Noise

Oscillator noise is caused by amplitude and phase fluctuations in the signal, and can be written as

$$V(t) = [V_o + \alpha(t)] \cos(\omega_o t + \theta(t)) , \tag{3.1}$$

where V_o is the oscillation amplitude, $\alpha(t)$ is the amplitude noise, and $\theta(t)$ is the phase noise. The amplitude noise and phase noise have equal power contribution to the output. However, due to an amplitude limiting mechanism present in the VCO, the amplitude noise can be removed, and only the phase noise is considered (Rael and Abidi 2000, Hajimiri and Lee 1998).

The phase fluctuation, $\theta(t)$, in Equation 3.1 can be classified into two types, namely, a random variation, $\varphi(t)$, and periodic variation, $\theta_p \sin(\omega_m t)$. First, let us consider only the random phase variation in the output signal as

$$V(t) = V_o \cos(\omega_o t + \varphi(t)) . \tag{3.2}$$

With the assumption that the root-mean-square (rms) value of $\varphi(t)$ is much smaller than 1 radian ($\varphi_{rms}(t) \ll 1$), PSD of $V(t)$ can be approximated as (Shu and Sinencio 2005)

$$S_V(\omega) = \frac{V_o^2}{2} \left[\delta(\omega - \omega_o) + S_\varphi(\omega - \omega_o)\right] , \tag{3.3}$$

where $S_\varphi(\omega - \omega_o)$ is the phase noise power at frequency offset, ω, from carrier signal, ω_o.

Secondly, let us consider the periodic phase variation in the signal as

$$\begin{aligned} V(t) &= V_o \cos(\omega_o t + \theta_p \sin(\omega_m t)) , \\ &= V_o \left[\cos(\omega_o t) \cos(\theta_p \sin(\omega_m t)) - \sin(\omega_o t) \sin(\theta_p \sin(\omega_m t))\right] . \end{aligned} \tag{3.4}$$

Also assuming the phase variation is very small, then

$$\cos(\theta_{\mathrm{p}}\ \sin(\omega_m t)) \approx 1\ , \tag{3.5}$$

$$\sin(\theta_{\mathrm{p}}\ \sin(\omega_m t)) \approx \theta_{\mathrm{p}} \sin(\omega_m t)\ . \tag{3.6}$$

Substituting Equations 3.5 and 3.6 into Equation 3.4, yields

$$\begin{aligned} V(t) &= V_{\mathrm{o}} \left[\cos(\omega_{\mathrm{o}} t) - \sin(\omega_{\mathrm{o}} t)\theta_{\mathrm{p}} \sin(\omega_m t)\right]\ , \\ &= V_{\mathrm{o}} \left[\sin(\omega_{\mathrm{o}} t) - \frac{\theta_{\mathrm{p}}}{2}\cos((\omega_{\mathrm{o}} - \omega_{\mathrm{m}})t) + \frac{\theta_{\mathrm{p}}}{2}\cos((\omega_{\mathrm{o}} + \omega_m)t)\right]\ . \end{aligned} \tag{3.7}$$

Equation 3.7 shows the periodic phase variation is caused by two sidebands with an amplitude of $\frac{\theta_{\mathrm{p}}}{2}$ appearing at $\pm f_m$ offsets from the carrier frequency, f_{o}.

3.3 Phase Noise Effect on RF Communication Systems

The frequency synthesiser output purity is very important because the output acts as a reference frequency for frequency translations in the up-conversion and down-conversion processes. However, an ideal sinusoidal signal is impossible to produce. Therefore, it is very important to keep the signal phase noise as small as possible.

Consider an RF receiver with the frequency synthesiser output, ω_{FS}, receiving an RF signal, ω_{RF}, as shown in Figure 3.2. The RF signal is also accompanied by a strong interference signal, ω_{i}, in an adjacent channel. Both of the signals, ω_{RF} and ω_{i}, are mixed with the synthesiser output, ω_{FS}, yielding an overlapping down-converted signal at ω_{IF}. The desired signal suffers from a strong noise due to the tail spectrum from the interfering channel. This effect is called reciprocal mixing.

In addition, a bad phase noise synthesiser output at the transmitter also affects the system performance. Assuming an ideal RF signal is located at ω_{RF} as shown in Figure 3.3, and a nearby transmitter generates a strong signal, ω_{t}, close to the weak desired signal. Thus, the noisy ω_{t} corrupts the desired ω_{RF} signal.

A sideband noise or reference spur also affects the system noise performance and can be a limiting factor for some receivers. Figure 3.4 shows the effect of sideband noise in a receiver. In this example, ω_{RF} is an RF signal frequency, ω_{i} is the interference signal, ω_{FS} is the frequency synthesiser output, and ω_m is the frequency synthesiser sideband; if $\omega_{\mathrm{RF}} - \omega_{\mathrm{FS}} = \omega_{\mathrm{i}} - \omega_m = \omega_{\mathrm{IF}}$, the interference signal will be translated

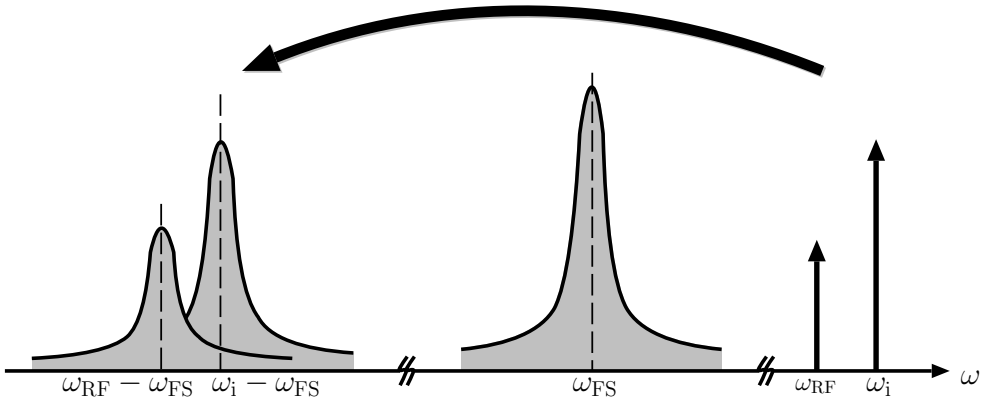


Figure 3.2. Reciprocal mixing. A phenomenon when a noisy synthesiser frequency (ω_{FS} translates a strong nearby channel interferer signal (ω_i) together with the desired RF signal (ω_{RF}), resulting in an overlapping down-converted signal at ω_{IF}, where $\omega_{IF} = \omega_{RF} - \omega_{FS}$.

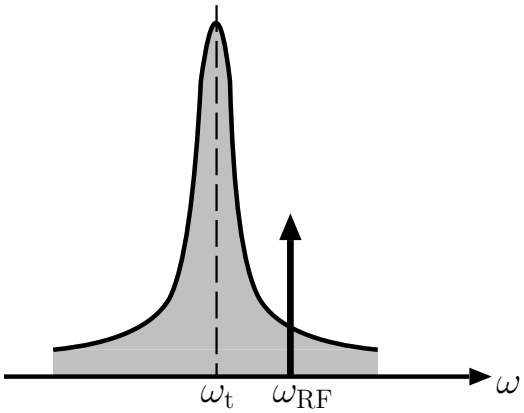


Figure 3.3. Effect of poor phase noise on a transmitter. A strong noisy nearby transmitter at ω_t, corrupts the RF signal (ω_{RF}).

into the desired band. Most of the RF receivers reduce this interference by keeping the sideband power less than 60 dBc (Razavi 1998).

3.4 Phase Noise in PLL

A phase noise significantly affects the quality of RF communication systems. Therefore, a low noise PLL is very important to provide a good noise performance frequency synthesiser in RF transceivers. The PLL phase noise is contributed by each component in the loop. The noise contribution can be modelled in a linear phase model as

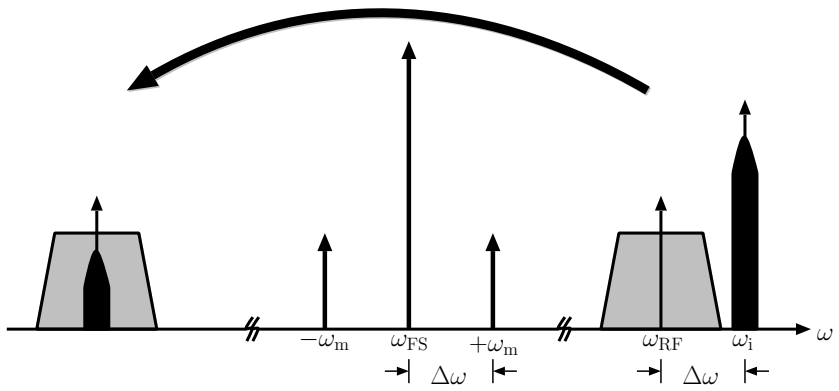


Figure 3.4. Effect of a strong reference spur in the receiver. If the sideband noise, ω_{m}, is located at $\Delta\omega$ away from ω_{FS}, and a strong interference signal (ω_{i}) is also located at $\Delta\omega$ away from ω_{RF}, the interference signal is translated into the desired band.

shown in Figure 3.5, where K_{pd} is the PFD and charge pump gain, and is given by $I_{\mathrm{cp}}/2\pi$ (A/rad), where I_{cp} is the charge pump current. The VCO is modelled as K_{vco}/s where K_{vco} is the VCO gain. The loop filter is presented as its transfer function, $F(s)$, and $1/N$ is the frequency divider.

In the linear phase model, phase noise is added to the component output. As shown in the Figure 3.5, θ_{ref}, θ_{vco}, and θ_{div} represent phase noise contribution from the reference clock, VCO, and frequency divider, respectively. Meanwhile, i_{cp} is the current noise that is contributed by charge pump, and v_{lf} is the voltage noise from the loop filter.

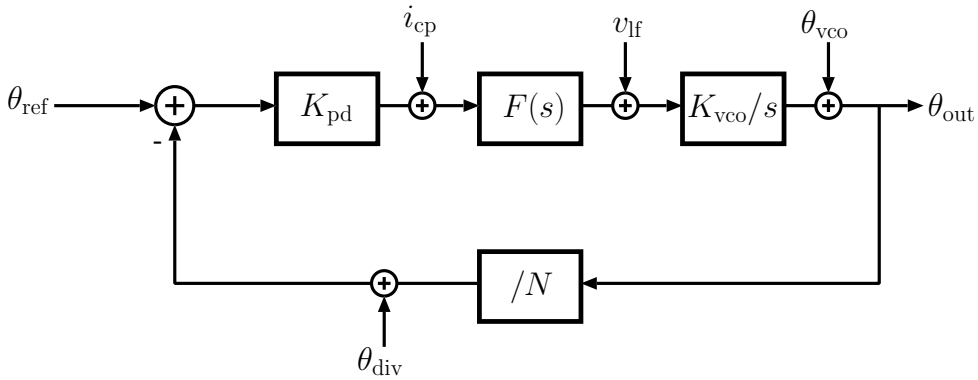


Figure 3.5. Charge pump PLL linear phase model. This model represents the noise contribution from each component in the PLL, which is the VCO (θ_{vco}), frequency divider (θ_{div}), reference clock (θ_{ref}), and loop filter (v_{lf}). Also, noise from PFD and charge pump are combined together as i_{cp}.

The PLL open loop transfer function, $H_{\text{ol}}(s)$, can be defined by disconnecting the feedback loop between the divider and PFD, and is given by

$$H_{\text{ol}}(s) = \frac{K_{\text{pd}} K_{\text{vco}} F(s)}{Ns} \,. \tag{3.8}$$

Considering only one noise contribution at a time, the transfer function from each noise source to the output is obtained. The PLL output to reference noise transfer function is given by

$$\begin{aligned} \frac{\theta_{\text{out}}}{\theta_{\text{ref}}} &= \frac{\frac{K_{\text{pd}} K_{\text{vco}} F(s)}{s}}{1 + \frac{K_{\text{pd}} K_{\text{vco}} F(s)}{Ns}} \,, \\ &= N \frac{H_{\text{ol}}}{1 + H_{\text{ol}}} \,. \end{aligned} \tag{3.9}$$

The charge pump currents only active for a short time of period, according to signals from the PFD output. The PLL output to this current noise transfer function is given by

$$\begin{aligned} \frac{\theta_{\text{out}}}{i_{\text{cp}}} &= \frac{\frac{K_{\text{vco}} F(s)}{s}}{1 + \frac{K_{\text{pd}} K_{\text{vco}} F(s)}{Ns}} \,, \\ &= \frac{N}{K_{\text{pd}}} \frac{H_{\text{ol}}}{1 + H_{\text{ol}}} \,. \end{aligned} \tag{3.10}$$

The PLL output to the loop filter noise transfer function can be written as

$$\begin{aligned} \frac{\theta_{\text{out}}}{v_{\text{f}}} &= \frac{\frac{K_{\text{vco}}}{s}}{1 + \frac{K_{\text{pd}} K_{\text{vco}} F(s)}{Ns}} \,, \\ &= \frac{K_{\text{vco}}}{s} \frac{1}{1 + H_{\text{ol}}} \,. \end{aligned} \tag{3.11}$$

The PLL output to the VCO noise transfer function can be written as

$$\begin{aligned} \frac{\theta_{\text{out}}}{\theta_{\text{vco}}} &= \frac{1}{1 + \frac{K_{\text{pd}} K_{\text{vco}} F(s)}{Ns}} \,, \\ &= \frac{1}{1 + H_{\text{ol}}} \,. \end{aligned} \tag{3.12}$$

The PLL output to the frequency divider noise transfer function is given by

$$\begin{aligned}\frac{\theta_{\text{out}}}{\theta_{\text{div}}} &= \frac{-\frac{K_{\text{pd}}K_{\text{vco}}F(s)}{s}}{1+\frac{K_{\text{pd}}K_{\text{vco}}F(s)}{Ns}}, \\ &= -N\frac{H_{\text{ol}}}{1+H_{\text{ol}}}. \end{aligned} \tag{3.13}$$

In conclusion, in order to obtain a low phase noise, the PLL must have a low dividing ratio (N), a low VCO gain (K_{vco}), and a high charge pump current (I_{cp}). Normally, the N and K_{vco} are chosen according to required system specifications, while a high charge pump current requires a large total capacitance of the loop filter (Li *et al.* 2011). Therefore, a designer has to consider the trade-off between phase noise requirement and total capacitor area on the die, in choosing the charge pump current.

3.4.1 PLL phase noise spectrum

In the previous section, transfer functions from each of the noise sources to the PLL output are given. However, the transfer function does not show the effect of the noise from each component to the PLL output. The output noise power for each noise source is defined by products of the input noise power and the magnitude squared of its transfer function (Osmany *et al.* 2007, Bourdi and Kale 2007, He 2007). The input noise power can be obtained by simulating each PLL component noise separately. Assuming that noise sources from each component are uncorrelated, the PLL output noise power can be calculated by summing the output noise power contributed from each noise sources. This section discusses the noise sources and its output noise power from each PLL component.

VCO noise

Note that VCO noise is the main noise contribution to the PLL output. Such noise extends to outside the loop bandwidth, and is filtered out by the loop bandwidth in the PLL frequency range of interest. In Figure 3.6, the dashed line shows the normalised free running VCO noise spectrum, $S_{\text{v}}(f)$, based on PSS and Pnoise SpectreRF simulation. The VCO output noise spectrum is given by

$$S_{\text{vco}_{\text{cl}}}(f) = S_{\text{v}}(f)\left|\frac{\theta_{\text{o}}}{\theta_{\text{vco}}}\right|^2, \tag{3.14}$$

where $\frac{\theta_o}{\theta_{vco}}$ is given by Equation 3.12. As shown by the solid line in Figure 3.6, the closed loop acts as a high pass filter to the VCO noise. Noise lower than the loop bandwidth (8 MHz for this example) is filtered, meanwhile noise outside the loop bandwidth is passed to the output.

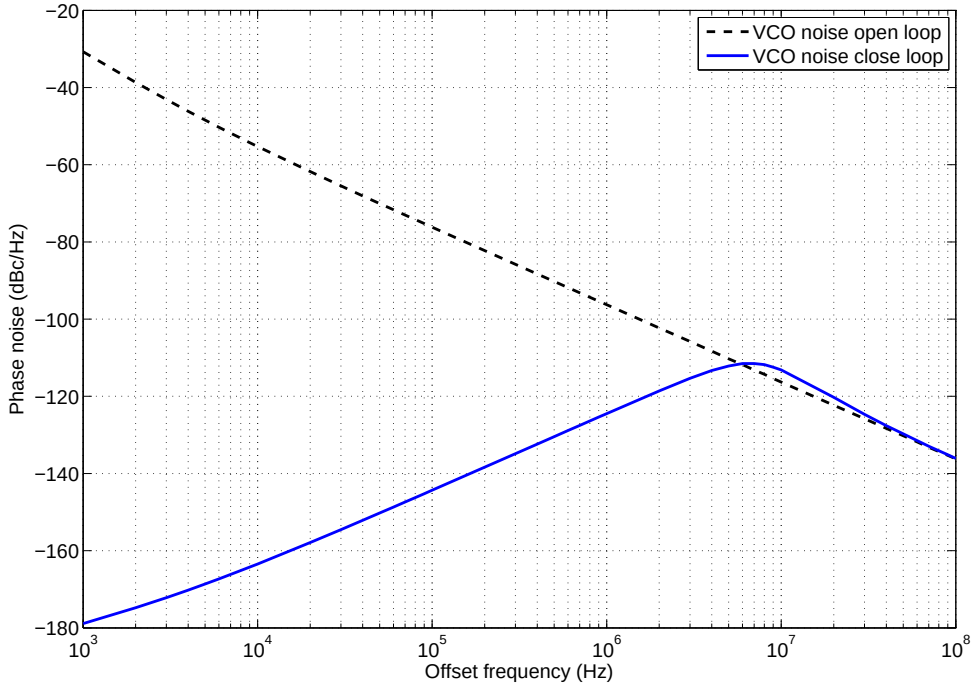


Figure 3.6. VCO noise spectrum. Here, the VCO noise is filtered out at low offset frequency. Noise at offset frequency outside the loop bandwidth is passed to the PLL output.

Reference noise

A crystal oscillator is commonly used as a reference noise. Noise from the crystal oscillator is very low compared to noise from PLL components, hence the reference noise is only dominated at the very low offset frequency. With assumption a low noise crystal oscillator is used in this thesis, noise from the reference frequency at frequency offset higher than 1 kHz is very low, and can be neglected.

Divider noise

Noise from a series of frequency dividers is plotted in Figure 3.7. In the loop, the noise is modified by Equation 3.15 and is shown by the solid line in Figure 3.7.

$$S_{\mathrm{div_{cl}}}(f) = S_{\mathrm{div}}(f)\left|\frac{\theta_o}{\theta_{\mathrm{div}}}\right|^2 . \tag{3.15}$$

The loop acts as a low pass filter to the divider noise. At a low frequency offset, the divider noise is passed to the output. Outside the loop bandwidth, the loop filters out the divider noise. As shown in Figure 3.7, the closed loop divider noise is higher than the open loop divider noise by $20\log(N)$, where N is a dividing ratio. In this example, $N = 128$, therefore the closed loop divider noise is increased by 48 dB. To lower the divider closed loop noise, a small dividing ratio must be used. However, a small dividing ratio requires a high reference frequency, which is not a preferable option because the cost of reference oscillators grows with the frequency (Glisic and Winkler 2006). Therefore, a trade off between phase noise and cost have to be considered in choosing the dividing ratio and reference frequency.

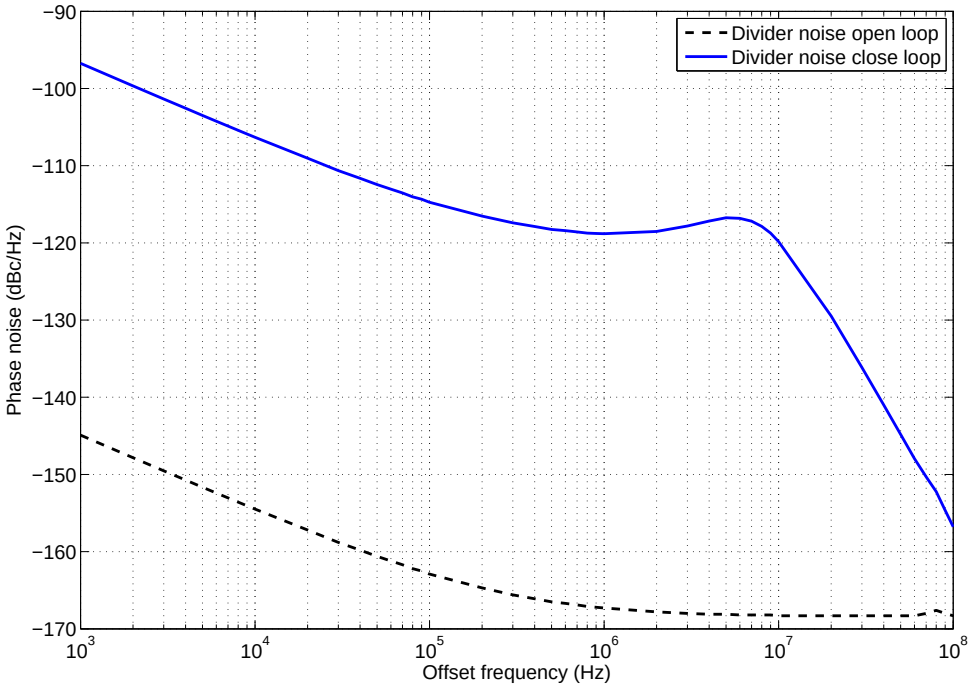


Figure 3.7. Frequency divider noise spectrum. The divider noise is low pass filtered by the loop. The closed loop divider noise is increased by $20\log(N)$, where N is a dividing ratio (48 dB in this case).

PFD and charge pump noise

Open loop PFD and charge pump noise can be obtained by PSS and Pnoise simulation using Cadence Spectre. For the simulation, a PFD is connected to a charge pump and the charge pump output is connected to a voltage source. The open loop charge pump

noise spectrum is shown in Figure 3.8. The open loop noise is modified by the PLL loop and is given by

$$S_{\mathrm{cp_{cl}}}(f) = S_{\mathrm{cp}}(f) \left| \frac{\theta_{\mathrm{o}}}{i_{\mathrm{cp}}} \right|^2 . \tag{3.16}$$

Similarly with the divider noise, the charge pump current noise is also low pass filtered by the PLL loop. Also, the noise increases depending on the dividing ratio, N.

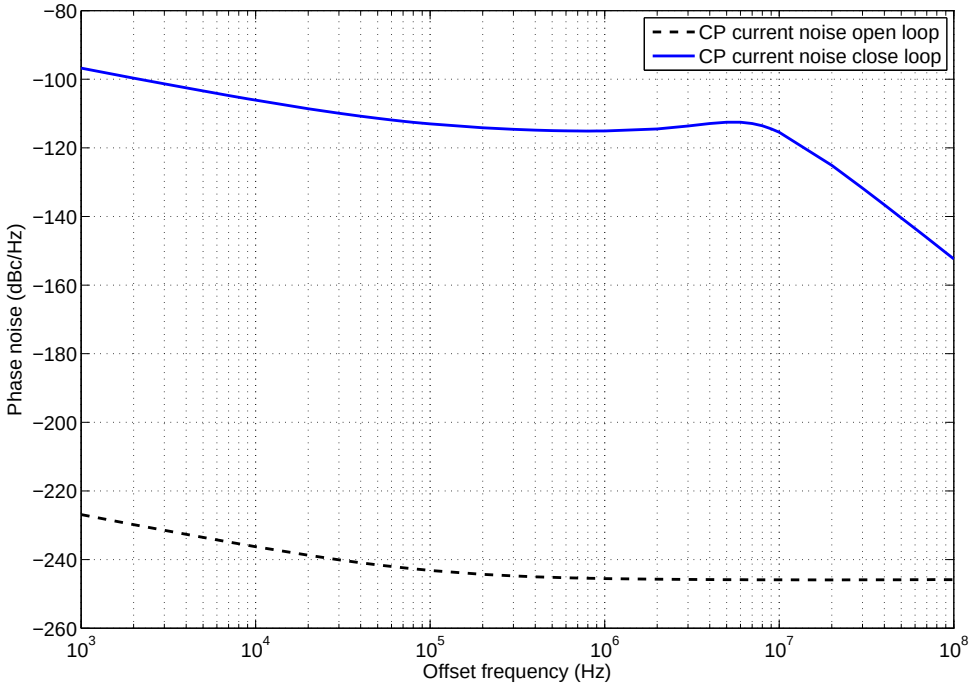


Figure 3.8. Charge pump current noise spectrum. Similar to the divider noise, the charge pump current noise is also low pass filtered by the loop. Also, the noise increases depending on the dividing ratio N.

Filter noise

A passive low pass filter consists of resistor(s) and capacitor(s). The noise is mainly contributed by thermal noise from these components. For a simple RC filter, the major noise is from the resistors (Chye 2004). The single sided power spectral density of the noise is given by

$$S_{\mathrm{f_{ol}}} = 4kTR , \tag{3.17}$$

where k is the Boltzmann constant with value 1.38×10^{-23} JK^{-1}, T is absolute temperature in Kelvin, and R is the total resistor value in the filter.

This noise spectrum is then modified by the loop, and is given by

$$S_{f_{cl}}(f) = S_{f_{ol}}(f) \left| \frac{\theta_o}{v_f} \right|^2 . \tag{3.18}$$

The loop filter thermal noise and its closed loop spectrum are shown in dashed and solid lines, respectively in Figure 3.9. The loop acts as a band pass filter to the filter noise.

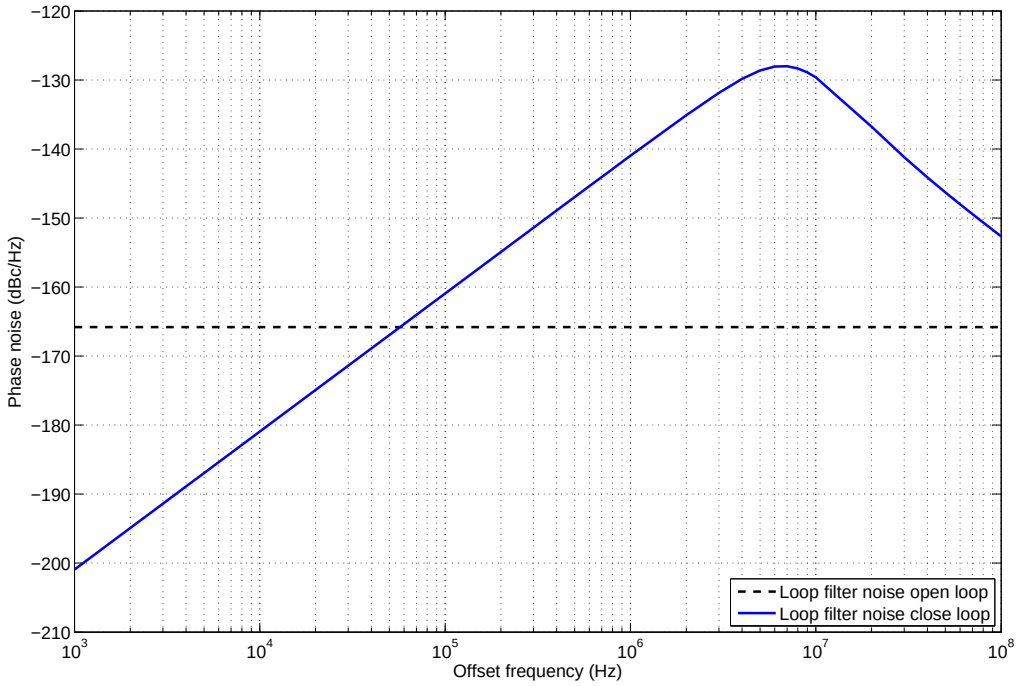


Figure 3.9. Loop filter noise spectrum. The loop filter noise is mainly from thermal noise. The loop acts as a band pass filter to the filter noise.

PLL noise

In order to predict the PLL output spectrum, the output noise power from each component is added as shown in Figure 3.10. At low offset frequencies, charge pump current noise and divider noise are the major contributors to the PLL output. One of the factor for these noise is the dividing ratio, N. Decreasing the N by factor of 2 can improves the noise by 6 dB.

Outside the loop bandwidth, only the VCO noise contributes to the PLL output. Logically, a larger loop bandwidth can provide a better PLL noise performance. Unfortunately, the loop bandwidth is only limited up to 10% of the reference frequency, in order to maintain the loop stability (Gardner 1980). With no option to increase the loop

bandwidth, only low noise VCOs can be used to have an improved PLL noise performance. In order to design a low noise VCO, the noise sources from the VCO have to be understood. Therefore, much research has been carried out to model the VCO phase noise (Mehrotra 2002, Lee and Hajimiri 2000, Rael and Abidi 2000, Samori *et al.* 1998, Leeson 1966).

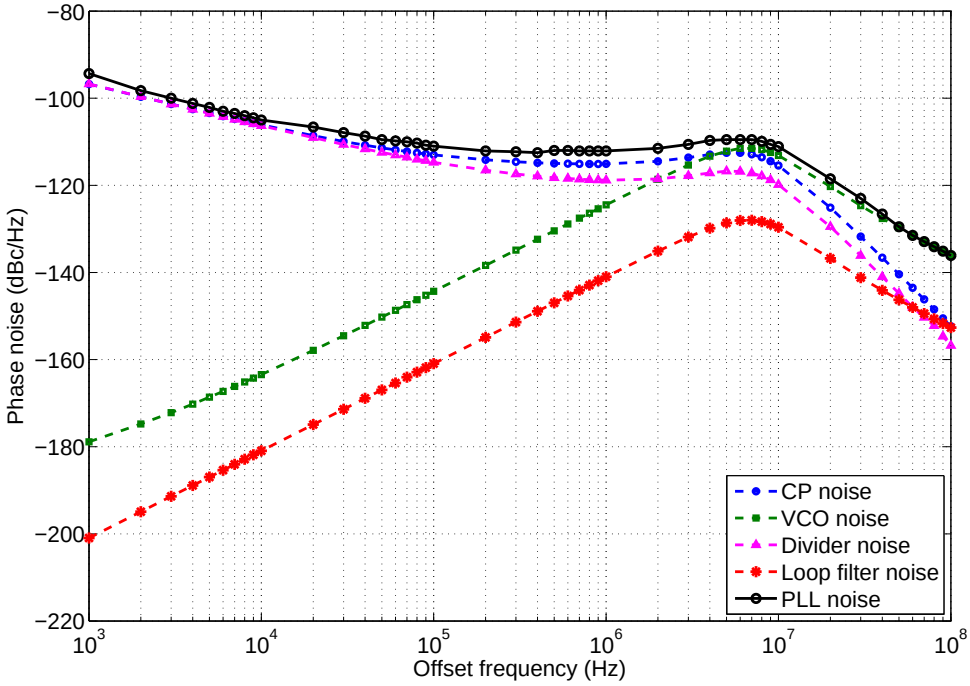


Figure 3.10. PLL noise spectrum. Noise contribution from each component resulting in the PLL closed loop spectrum. Outside the loop bandwidth, VCO dictates the noise at the PLL output. Meanwhile, noise from the charge pump and divider dictate the PLL phase noise at lower frequency offset.

3.5 PLL Reference Spurs

In addition to the phase noise, an integer-N PLL also suffers from reference spurs. The main contributions to the reference spurs are: PFD delay, charge pump switching delay, charge pump current leakage, charge pump current mismatch, charge injection, and charge sharing (Razavi 2001, Rhee 1999). These circuit non-idealities are produced by the PFD and charge pump circuits. Figure 3.11 shows commonly used PFD and charge pump circuits in a PLL. Non-idealities in the PFD and charge pump circuits cause a periodic small pulse in the VCO tuning voltage. These periodic pulses modulate the VCO output frequency and produce a fairly large signal at f_{ref} away from the carrier.

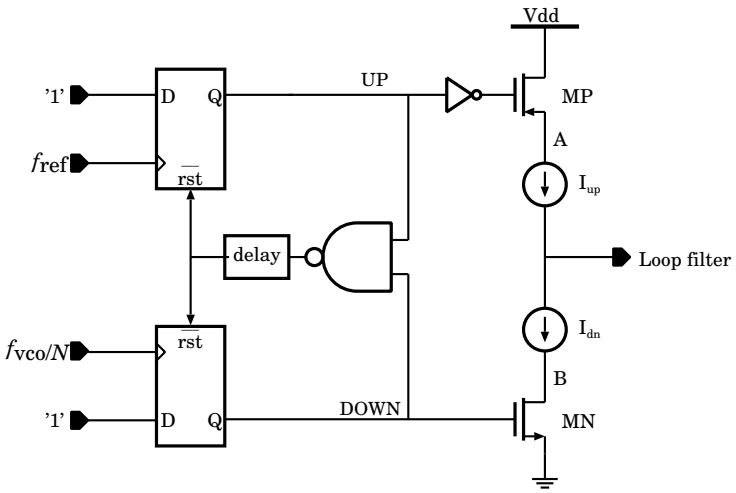


Figure 3.11. PFD and charge pump circuits. Non-idealities in these two circuits, namely, PFD delay, switching delay, charge pump current mismatch, charge pump current leakage, and charge pump current rise and fall time characteristics, are the main contributions to the reference spurs in an integer-N PLL.

The reference spurs also can be contributed by periodic supply and substrate noise due to possible periodic operation of digital circuits in the PLL, which are the PFD, charge pump, and divider (Shu and Sinencio 2005). The supply noise can be reduced by including a huge coupling capacitor to the supply voltage, especially for the VCO. Another technique to minimise the noise coupling from supply and substrate is by using a separate power supply and ground planes for digital and analog circuits (Mota and Christiansen 1998, LaMay and Bogard 1992). Including guard-rings in the layout, to separate the digital from the analog circuits, also helps to minimise noise coupling (Mota and Christiansen 1998, Warren and Jungo 1988). Analysis in this thesis neglects the periodic noise from the supply and substrate as these noise sources are independent of the PLL circuit design.

3.5.1 PFD delay

The PFD compares frequencies and phases between the reference signal and the divided PLL output. A phase difference between these signals produces a pulse on the PFD output, named UP and DOWN signals. The pulses control MP and MN switches in the charge pump as shown in Figure 3.11. Therefore, a sufficient pulse period is required to ensure MP and MN switches can be turned ON, for converting the phase differences into voltages.

When the phase difference is very small, a very small pulse is generated at the PFD output. A propagation delay in the PFD (Charles and Allstot 2006) and the rise and fall times, result in no pulse or a very short pulse on the UP and DOWN signals, hence no switching occurs in the charge pump. In other words, the PFD is unable to detect a very small phase difference between the reference signal and the divided PLL output, hence the phase at the PLL output varies freely within this range, resulting in a higher phase noise (Charles and Allstot 2006). This phenomenon is called a *dead zone*.

The dead zone can be eliminated by adding a delay in the reset path of the PFD. The delay must produce an enough period to ensure the charge pump switching events. Ideally, delays on the UP and DOWN signals are similar. However, a current mismatch in the charge pump circuit cause a difference amount of delay between these signals, results in reference spurs to the PLL output. Further discussion on effect of the PFD delay and charge pump current mismatch to the reference spur magnitude is presented in Section 4.3.1.

3.5.2 Charge pump current mismatch

Another factor contributes to reference spurs is a charge pump current mismatch. Ideally, the charge pump currents, I_{up} and I_{dn} as shown in Figure 3.11 are equal. However, due to channel length modulation and variation of parameters between NMOS and PMOS on the current mirror structures, I_{up} and I_{dn} are slightly different (Mekky and Dessouky 2007).

After the PLL is locked, the total charge transfer to the loop filter is zero. Therefore, if I_{up} and I_{dn} are unequal, the ON period for either the UP or DOWN switches has to be longer than the other, to compensate the charge difference. For example, if $I_{up} > I_{dn}$, the DOWN switch has to be turned ON longer than the UP switch. As mentioned in the previous sub-section, these switches are controlled by the PFD output, hence the current mismatch cause a difference PFD delay between UP and DOWN signals.

3.5.3 Charge pump current leakage

When both UP and DOWN switches in the charge pump are OFF, there must be a zero net current flows to the filter. However, due to a sub-threshold leakage there is still a very small current leaks through the UP and DOWN switches in the charge pump

circuit, hence charge and discharge the capacitor in the loop filter, results in changes on the VCO tuning voltage (Liu and Willson 2010). The amount of leakage current is also affected by the VCO tuning port leakage. Since the VCO input impedance is very large, the current leaks to the loop filter (Gardner 1980). The amount of leakage current is depending on the used technology.

3.5.4 Switching delay

Another main cause of reference spurs is the charge pump switching mismatch between the UP and DOWN switches. Since the UP switch uses a PMOS transistor, an inverter is required to invert signals from the PFD. This inverter introduces a delay to the UP signal as shown in Figure 3.12, hence delays the I_{up} switching.

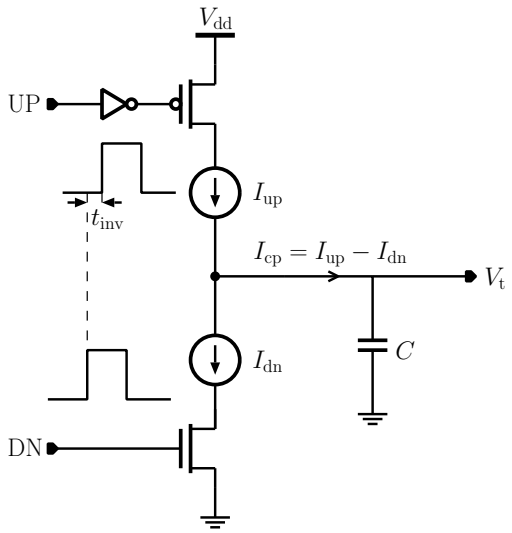
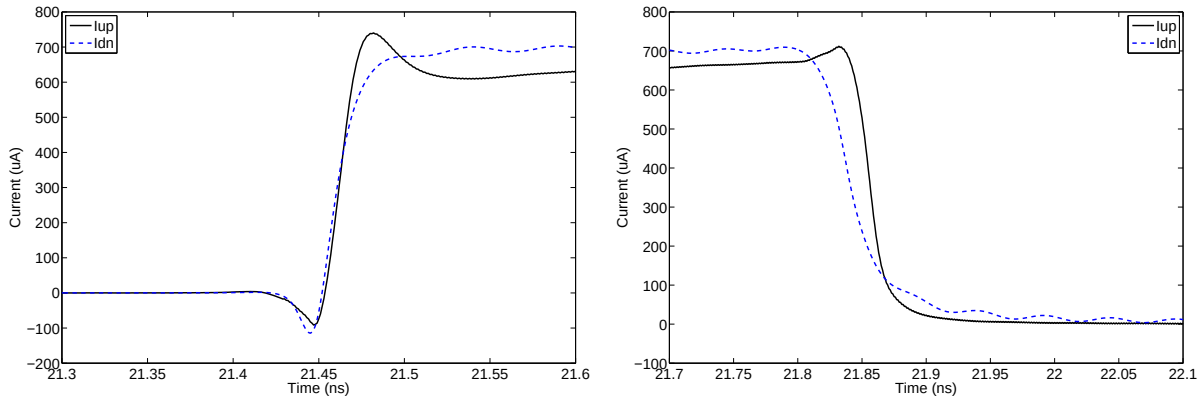


Figure 3.12. Charge pump circuit with a switching delay. An inverter coupled into the UP signal, and delays the I_{up} switching.

The added delay by the inverter to the UP signal affects the VCO tuning voltage, hence causing spurs at the PLL output. The delay can be minimised by using a transmission gate to match the UP and DOWN signals (Razavi 2001) or using a complementary differential cascode inverter to reduce this delay. However, none of the approaches completely eliminates the delay, as a result a reference spur is introduced at the PLL output.

3.5.5 Charge pump current rise and fall time characteristics

The charge pump currents, namely, I_{up} and I_{dn}, contain a different rise and fall times response. The size of PMOS and NMOS transistors in the charge pump circuit affects the rise and fall times of the I_{up} and I_{dn}, respectively. Also, different types and sizes of transistors results in a further difference in the rise and fall times. In addition, a different loop filter also gives a different load to the charge pump, hence affects the rise and fall time characteristics. The difference in rise and fall times then produces a small spike on the VCO tuning voltage, hence cause spurs on the PLL output. Figure 3.13 shows a simulation result on the rise and fall times response of I_{up} and I_{dn}.



(a) Rise time for I_{up} and I_{dn}

(b) Fall time for I_{up} and I_{dn}

Figure 3.13. Charge pump current rise and fall times. A different rise and fall times response between the I_{up} and I_{dn} produces ripples in the VCO tuning voltage.

3.5.6 Charge injection and charge sharing

Other causes of reference spurs are charge injection and charge sharing in transistors MN and MP in Figure 3.11. The charge injection is from charges stored in the channels of the switch transistors when they turn ON or OFF and the charge sharing is from node A and B (shown in Figure 3.11) in the charge pump when both transistors are ON (Charles and Allstot 2008).

The charge injection can be minimised by minimising the size of both, UP and DOWN switch transistors. Therefore, the injected charge at each switching event is minimised (Charles and Allstot 2008). For a charge sharing minimisation, two charge pump topologies can be used, namely, a current steering (Charles and Allstot 2008) and a source switched charge pump (Charles and Allstot 2008, Maxim 2002). The current

steering topology still produces a small charge injection due to mismatches between the UP and DOWN signals and their inverse (Charles and Allstot 2008). Also, the design is more complicated compared to a standard charge pump architecture. This thesis uses the source switched charge pump topology to minimise the charge injection as this topology is less complex compared to current steering.

3.6 Chapter Summary

Phase noise at the PLL output determines the system performance. Therefore, a low noise PLL design is very important. The noise is categorised into two types, namely, phase noise and reference spurs. The PLL phase noise is contributed by each component in the loop. The frequency divider and charge pump are the main phase noise sources at lower offset frequency. Meanwhile, the VCO phase noise contributes to the higher offset frequency.

On the other hand, reference spurs are mainly from circuit non-linearity in the PFD and charge pump. The last section in this chapter discusses the main contributors to the reference spurs. A detailed analysis of how each factor affects the spur magnitude is discussed in the next chapter.

Chapter 4

Reference Spur Analysis

A REFERENCE spur signal is a limiting performance factor in an integer-N PLL. Reference spurs are mainly caused by the PFD and charge pump circuit non-idealities. These non-idealities cause a periodic ripple in the VCO tuning voltage. The VCO modulates this ripple voltage, hence produces spurs at multiple reference frequency offsets from the carrier signal. In addition to circuit non-idealities, a few other factors such as the VCO gain and loop filter, also affect the spur magnitude. This chapter presents a reference spur mathematical analysis to accurately estimate the spur magnitude. A periodic ripple in the VCO tuning voltage is modelled. Also, the affect of charge pump current mismatch, current leakage, switching delay, rise and fall time characteristics, and loop filter on the spur magnitude are discussed. Results from the proposed model are compared to a transistor level simulation using Cadence Spectre.

4.1 Introduction

In Chapter 3, two types of PLL noise, namely, phase noise and reference spurs were discussed. Many works have been carried out in a PLL phase noise modelling, however the reference spur aspect of PLL modelling attracted much less attention (Demir 2006, Von Bueren *et al.* 2009, Mehrotra 2002).

Reference spurs can be modelled using narrow-band frequency modulation theory (Shu and Sinencio 2005, Manassewitsch 2005). Based on the published models, the spur magnitude is predicted, and the model is used in several published works (Maxim 2002, Lee and Hajimiri 2000, Rhee 1999). However, the predicted spur magnitude has not been verified with any measurement or simulation. Also, previous work in the literature does not model the ripples in the VCO tuning voltage, which is the main factor behind the spur magnitude.

In the literature, ripples in the VCO tuning voltage are assumed to be a sinusoidal signal, resulting in an inaccurate spur magnitude estimation. This thesis accurately models the ripples in the tuning voltage, hence an accurate spur magnitude can be estimated. In addition, magnitude of the ripple is also analysed. The ripple voltage is caused by circuit non-idealities in the PFD and charge pump. Three non-idealities, namely, a current leakage, current mismatch, and switching delay have been modelled in the phase domain (Rhee 1999). The relationship between phase error caused by these three non-idealities and the ripple magnitude, are discussed in Shu and Sinencio (2005). However, the non-ideality effects are discussed separately, hence the resulting reference spur magnitude estimation is only considered for that particular non-ideality.

In this thesis, a time domain analysis is considered to model the effect of charge pump current leakage, current mismatch, rise and fall time characteristics, and switching delay on the reference spur. In addition, the VCO tuning port leakage effect on the spur magnitude in a third order PLL, is also discussed. A combination of all these non-idealities are considered together for a reference spur magnitude estimation.

In this chapter, a time-domain reference spur mathematical analysis for an integer-N PLL is presented in Section 4.2. In Section 4.3, ripples in the VCO tuning voltage are modelled. The PFD and charge pump non-idealities are included in the model. The reference spur magnitude that predicted using the proposed model is then compared with a transistor level simulation result in Section 4.4. Using this proposed model, effects of different filters order, VCO gain, charge pump current mismatch and leakage,

and switching delay on the reference spur magnitude are investigated in Section 4.5. Finally, this chapter is summarised in Section 4.6.

4.2 Spur Magnitude

Reference spurs appear when a periodic signal in the VCO tuning voltage, V_t, modulates the output frequency. Ideally, V_t is a straight line without any ripples, however in the real implementation, V_t is a periodic pulse with a pulse repetition rate equals to the reference frequency, as shown in Figure 4.1. This periodic pulse is caused by circuit non-idealities in the PFD and charge pump circuits.

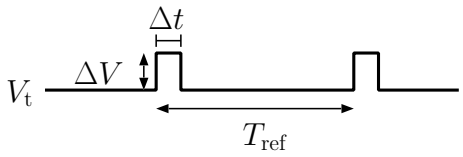


Figure 4.1. VCO tuning voltage. Due to circuit non-idealities, the VCO tuning voltage (V_t) appears as a periodic signal instead of a straight line. Here, δV is the ripple magnitude, δt is the ripple period, and T_{ref} is the reference clock period.

In a locked state, ΔV is very small, hence a narrow-band frequency modulation theory can be used to model the VCO output. The VCO output signal can be presented as

$$V_{vco}(t) = V_o \cos\left(\omega_o t + K_v \int V_t \, dt\right) , \tag{4.1}$$

where V_o is the VCO output amplitude, V_t is an ideal VCO tuning voltage, ω_o is the VCO output frequency when tuning voltage is zero, and K_v is the VCO gain in rad/sV.

Using a Fourier series, the rippled VCO tuning voltage, V_t' can be represented as

$$V_t' = V_t + \frac{\Delta V \Delta t}{T_{ref}} + \frac{2\Delta V}{T_{ref}\omega_{ref}} \sum_{n\neq 0} \frac{\cos(n\omega_{ref}t)\ \sin(n\omega_{ref}\Delta t)}{n} , \tag{4.2}$$

where T_{ref} is the reference clock period, and ω_{ref} is the reference clock frequency. Let the periodic component in V_t' be represented as $A(t)$, and is given by

$$A(t) = \frac{2\Delta V}{T_{ref}\omega_{ref}} \sum_{n\neq 0} \frac{\cos(n\omega_{ref}t)\ \sin(n\omega_{ref}\Delta t)}{n} . \tag{4.3}$$

Substituting V_t in Equation 4.1 with V_t' and $A(t)$ in Equations 4.2 and 4.3, yields

$$V_{vco}(t) = V_o \cos\left(\omega_o t + K_v t\left(V_t + \frac{\Delta V \Delta t}{T_{ref}}\right) + K_v \int A(t)\, dt\right) . \tag{4.4}$$

Let the VCO phase be represented as ω_{vco}, and is given by

$$\omega_{vco} = \omega_o + K_v V_t + K_v \frac{\Delta V \Delta t}{T_{ref}} . \tag{4.5}$$

Substituting Equation 4.5 into Equation 4.4, yields

$$\begin{aligned} V_{vco}(t) &= V_o \cos\left(\omega_{vco} t + K_v \int A(t)dt\right) , \\ &= V_o \cos\left(\omega_{vco} t\right) \cos\left(K_v \int A(t)dt\right) - V_o \sin\left(\omega_{vco} t\right) \sin\left(K_v \int A(t)dt\right) . \end{aligned} \tag{4.6}$$

Let the phase deviation due to circuit non-idealities, ϕ, be represented as

$$\phi = K_v \int A(t)dt . \tag{4.7}$$

The value of ϕ is very small, therefore Equation 4.6 can be simplified to

$$V_{vco}(t) = V_o \cos\left(\omega_{vco} t\right) - V_o \phi \sin\left(\omega_{vco} t\right) . \tag{4.8}$$

Expand the phase deviation, ϕ, in Equation 4.7, with $A(t)$ as in Equation 4.3, yields

$$\begin{aligned} \phi &= K_v \left(\frac{2\Delta V}{T_{ref}\omega_{ref}}\right) \int \sum_{n\neq 0} \frac{\cos(n\omega_{ref} t)\ \sin(n\omega_{ref}\Delta t)}{n}\, dt , \\ &= \frac{2K_v \Delta V}{T_{ref}\omega_{ref}} \sum_{n\neq 0} \frac{\sin(n\omega_{ref} t)\ \sin(n\omega_{ref}\Delta t)}{n^2 \omega_{ref}} , \\ &= \frac{K_v \Delta V}{T_{ref}\omega_{ref}^2} \sum_{n=0}^{\infty} \frac{\cos(n\omega_{ref}(t-\Delta t)) - \cos(n\omega_{ref}(t+\Delta t))}{n^2} . \end{aligned} \tag{4.9}$$

Substituting Equation 4.9 into Equation 4.8, while considering only the first spur, ($n = 1$), the VCO output is given by

$$V_{\text{vco}}(t) = V_{\text{o}} \cos(\omega_{\text{vco}} t) - \frac{V_{\text{o}} K_{\text{v}} \Delta V}{T_{\text{ref}} \omega_{\text{ref}}^2} \sin(\omega_{\text{vco}} t) \left[\cos(\omega_{\text{ref}}(t - \Delta t)) - \cos(\omega_{\text{ref}}(t + \Delta t))\right] . \tag{4.10}$$

According to the FM theory, the modulation index, β, is

$$\beta = \frac{K_{\text{v}} \Delta V}{T_{\text{ref}} \omega_{\text{ref}}^2} . \tag{4.11}$$

Simplifying this equation by replacing the VCO gain in rad/sV (K_{v}), with VCO gain in Hz/V ($2\pi K_{\text{v}}$), results in

$$\beta = \frac{K_{\text{v}} \Delta V}{\omega_{\text{ref}}} . \tag{4.12}$$

A frequency modulated signal can be expressed by the Bessel function series, as given by

$$J_n(\beta) = \sum_{k=0}^{\infty} \frac{-1^k}{k!\, \Gamma(k + n + 1)} \left(\frac{\beta}{2}\right)^{2k+n} . \tag{4.13}$$

For a small modulation index ($\beta \ll 1$), the carrier amplitude is approximately 1 ($J_0(\beta) \cong 1$), and the first spur amplitude is approximately half of the modulation index ($J_1(\beta \cong \beta/2$), while the rest terms in the series are approximately zero. Therefore, the reference spur magnitude, P_r, in dBc/Hz is

$$P_r = 20 \log \left(\frac{K_{\text{v}} \Delta V}{2\omega_{\text{ref}}}\right) . \tag{4.14}$$

This equation is similar with the equation in Shu and Sinencio (2005), and Manassewitsch (2005), except for the VCO gain in the published work is in rad/sV, while this thesis proves that the VCO gain must be in Hz/sV, which means the reference spur magnitude predicted using the presented analysis is 2π lower compared to the previous analysis. This difference is because the previous work assumes the tuning voltage as a sinusoidal signal, while this work accurately models the tuning voltage using a Fourier series.

Equation 4.14 shows the reference spur magnitude has a linear relations with the VCO gain and the ripple magnitude, while the reference frequency is inversely proportional to the spur magnitude. Therefore, a low VCO gain and a high reference frequency helps to minimise the spur magnitude. Also, a low ΔV, reduces the spur magnitude. A detailed discussion on the ΔV effect on the VCO tuning voltage is presented in the next section.

4.3 VCO Tuning Voltage

As discussed in the previous section, ripples in the VCO tuning voltage (ΔV) are proportional to the reference spur magnitude. These ripples are caused by PFD and charge pump circuit non-idealities. In addition, the loop filter and VCO gain affects the amplitude of ripple voltage. In this section, ΔV amplitude is modelled, hence the reference spur magnitude can be estimated.

The presented analysis only concentrates on the reference spur, therefore the PLL is assumed to be in a locked state. For analysis simplification, the charge sharing and clock feedthrough are not taken into account. In the locked state, a total charge transfer to the loop filter is zero, $Q = 0$. In an ideal circuit, I_{up} and I_{dn} in the charge pump as shown in Figure 4.2 are equal. The charge transfer to the loop filter is given by

$$\begin{aligned} Q &= I_{\text{cp}}\, t_{\text{PFD}}\ , \\ &= (I_{\text{up}} - I_{\text{dn}})\, t_{\text{PFD}}\ , \end{aligned} \tag{4.15}$$

where t_{PFD} is a PFD delay, I_{cp} is the net charge pump current delivered to the loop filter, and I_{up} and I_{dn} are currents that enter and exit the loop filter, respectively. For simplification, at this early stage, the loop filter is considered as a single capacitor, C. A detailed analysis on a second and third order loop filter is discussed in Section 4.3.5.

The charge pump current charges the capacitor resulting in a voltage, which is referred to as a VCO tuning voltage (V_{t}), and is given by

$$V_{\text{t}}(t) = \frac{1}{C} \int I_{\text{cp}}\, dt\ . \tag{4.16}$$

Ideally, the charge pump currents, I_{up} and I_{dn}, are equal, resulting in an equal PFD delay for UP (t_{up}) and DOWN signals (t_{dn}). Therefore, no ripple exists in the VCO tuning

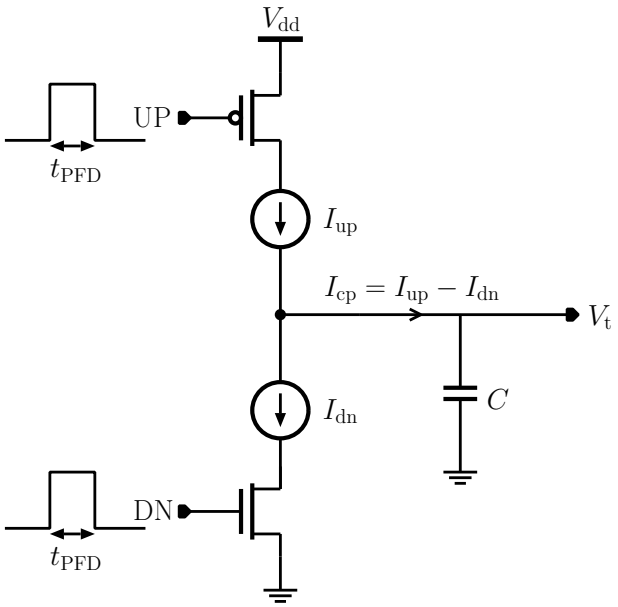


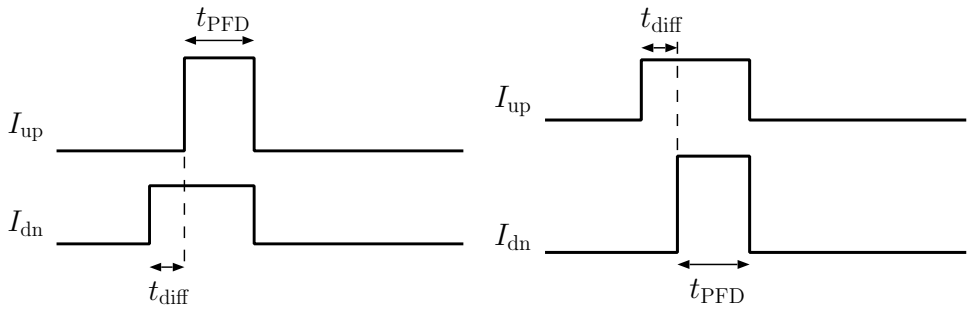
Figure 4.2. A source-switched charge pump circuit. In an ideal circuit, $I_{up} = I_{up}$, and $t_{up} = t_{up}$. Therefore, no ripple exists in the VCO tuning voltage.

voltage ($\Delta V = 0$), hence no reference spur appears on the PLL output. However, in the real implementation, charge pump circuit non-idealities such as current mismatch, current leakage, rise and fall time characteristics, and switching delay cause a ripple in the VCO tuning voltage. This section discusses these non-idealities and effect of a loop filter to the ΔV.

4.3.1 Charge pump current mismatch and PFD delay effect

Due to the channel length modulation and variation of parameters between NMOS and PMOS transistors, I_{up} is not equal to I_{dn} (Mekky and Dessouky 2007). Since the total charge transfer to the loop filter must be zero, the amount of PFD delay either in the UP or DOWN signal has to be adjusted to compensate for the current difference as shown in Figure 4.3. If I_{up} is larger than I_{dn}, t_{dn} must be slightly larger than t_{up}, and vice versa. The current mismatch and differences in the PFD delay results in ripples in the VCO tuning voltage, resulting in reference spurs in the PLL output.

Assuming the I_{up} is larger than I_{dn}, therefore, $t_{dn} = t_{PFD} + t_{diff}$, where t_{diff} is the PFD delay difference between UP and DOWN signal, and $t_{up} = t_{PFD}$ as shown in Figure 4.3(a). Since the total charge transfer is zero when the PLL is in locked state, Equation 4.15 can be rewritten as



(a) I_{up} is larger than I_{dn} (b) I_{dn} is larger than I_{up}

Figure 4.3. Effect of a current mismatch to the PFD delay (t_{PFD}). A charge pump current mismatch resulting in a different PFD delay between UP and DOWN signals.

$$\begin{aligned} I_{up}\, t_{up} - I_{dn}\, t_{dn} &= 0\,, \\ I_{up}\, t_{PFD} &= I_{dn}\, (t_{PFD} + t_{diff})\,, \\ t_{diff} &= t_{PFD} \left(\frac{I_{up}}{I_{dn}} - 1 \right)\,, \end{aligned} \tag{4.17}$$

and the VCO tuning voltage is given by

$$V_t(t) = \begin{cases} -\frac{1}{C} \int I_{dn}\, dt & \text{if } 0 < t < t_{diff} \\ -\frac{I_{dn} t_{diff}}{C} + \frac{1}{C} \int \left(I_{up} - I_{dn} \right)\, dt & \text{if } t_{diff} \leq t \leq (t_{diff} + t_{PFD})\,. \end{cases} \tag{4.18}$$

If the I_{dn} is larger than I_{up}, then $t_{up} = t_{PFD} + t_{diff}$, and $t_{dn} = t_{PFD}$ as shown in Figure 4.3(b), Equations 4.17 and 4.18 can be rewritten as

$$t_{diff} = t_{PFD} \left(\frac{I_{dn}}{I_{up}} - 1 \right)\,, \tag{4.19}$$

$$V_t(t) = \begin{cases} \frac{1}{C} \int I_{up}\, dt & \text{if } 0 < t < t_{diff} \\ \frac{I_{up} t_{diff}}{C} + \frac{1}{C} \int \left(I_{up} - I_{dn} \right)\, dt & \text{if } t_{diff} \leq t \leq (t_{diff} + t_{PFD})\,. \end{cases} \tag{4.20}$$

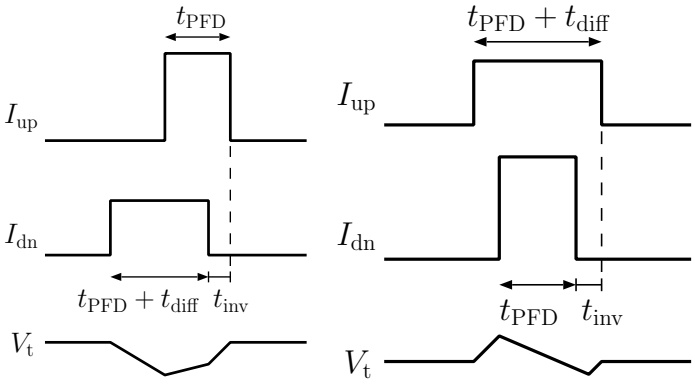
According to Equations 4.17 and 4.19, t_{diff} has a linear relation with both the charge pump current mismatch and PFD delay, and Equations 4.18 and 4.20 show the ripple voltage in the VCO tuning voltage, ΔV, is proportional to t_{diff}. A higher t_{diff} results in a higher ripple amplitude, hence increases the magnitude of the reference spurs. According to Equations 4.18 and 4.20, if I_{up} is larger than I_{dn}, the ripple voltage falls

slightly lower than the tuning voltage, meanwhile if I_{dn} is larger than I_{up}, the ripple voltage rises slightly higher than the tuning voltage. The ripple voltage direction in the tuning voltage is not significant on the reference spur calculation, however, the magnitude has a much greater affect.

4.3.2 Charge pump switching delay effect

As discussed in Section 3.5.4, a switching delay only exists in the charge pump UP switch, which is caused by an added inverter. This delay causes a ripple in the VCO tuning voltage, hence results in reference spurs. The affect of the switching delay on the ripple magnitude depends on the charge pump current, either I_{up} is larger than I_{dn} or vice versa.

The first category is when I_{up} is larger than I_{dn}, where $t_{dn} = t_{PFD} + t_{diff}$, and $t_{up} = t_{PFD}$ as shown in Figure 4.4(a). In this case, the delay caused by the inverter increases the ΔV. The second category is when I_{dn} is larger than I_{up}, where $t_{up} = t_{PFD} + t_{diff}$, and $t_{dn} = t_{PFD}$ as shown in Figure 4.4(b). The delay in UP signal helps to reduce the ripple amplitude in the tuning voltage, hence decreases the reference spur magnitude.



(a) I_{up} is larger than I_{dn} (b) I_{dn} is larger than I_{up}

Figure 4.4. Effect of the UP signal switching delay on the VCO tuning voltage. The switching delay increases the ΔV amplitude when $I_{up} > I_{dn}$, while the delay helps to reduce the ΔV amplitude when $I_{dn} > I_{up}$.

The magnitude of ripple voltage affected by the switching delay is given by

$$\Delta V_{delay} = \frac{1}{C} \int_0^{t_{inv}} I_{cp}\, dt\ . \tag{4.21}$$

4.3.3 Charge pump current rise and fall time characteristics

In addition to the PFD delay and charge pump current mismatch, a charge pump current response also affects the reference spur magnitude. Size of PMOS and NMOS transistors in the charge pump circuit affect the rise and fall times of the I_{up} and I_{dn}. Also, the different type and size of transistors results in an additional differences in the rise and fall times. In addition, a different loop filter also gives a different load to the charge pump, hence affects the rise and fall time characteristics. The difference in the rise and fall times response then produces a small spike in the VCO tuning voltage.

Considering the rise and fall times, the charge pump current, I_{up} and I_{dn}, can be modelled as i_{up} and i_{dn}, respectively, and are given by (Arora *et al.* 2005)

$$i_{up} = \begin{cases} I_{up}\left(1 - \exp^{\left(\frac{-t}{\tau_{rup}}\right)}\right), & \text{if } 0 < t \leq t_{up} \\ K_{up}\exp^{\left(\frac{-t}{\tau_{fup}}\right)}, & \text{if } t_{up} < t \leq t_{ref}\,, \end{cases} \tag{4.22}$$

$$i_{dn} = \begin{cases} I_{dn}\left(1 - \exp^{\left(\frac{-t}{\tau_{rdn}}\right)}\right), & \text{if } 0 < t \leq t_{dn} \\ K_{dn}\exp^{\left(\frac{-t}{\tau_{fdn}}\right)}, & \text{if } t_{dn} < t \leq t_{ref}\,, \end{cases} \tag{4.23}$$

where τ_{rup} and τ_{rdn} are the rise time constants for i_{up} and i_{dn}, respectively, while τ_{fup} and τ_{fdn} are the fall time constants for i_{up} and i_{dn}, respectively. Here, the t_{ref} is the reference clock period, and constants K_{up} and K_{dn} are given by

$$\begin{aligned} K_{up} &= I_{up}\left(1 - \exp^{\left(\frac{-t_{up}}{\tau_{rup}}\right)}\right), \\ K_{dn} &= I_{dn}\left(1 - \exp^{\left(\frac{-t_{up}}{\tau_{rdn}}\right)}\right). \end{aligned} \tag{4.24}$$

The net current flows into the loop filter is given by $i_{up} - i_{dn}$, therefore a different rise and fall times response between i_{up} and i_{dn} causes ripples in the VCO tuning voltage.

4.3.4 Charge pump current leakage

When both UP and DOWN switches are OFF, a small amount of current leaks to and from the loop filter. As explained in Section 3.5.3, the leakage current is due to a subthreshold leakage (Liu and Willson 2010) and a VCO tuning port leakage (Gardner 1980).

For a second order filter, the VCO tuning port shares the same node with the charge pump output. Therefore, the current leakage from the VCO tuning port modulates the charge pump current, hence increases the net current goes to the loop filter. As for a third order loop filter, the VCO tuning port is only connected to the third capacitor in the loop filter (as shown in Figure 4.6). Therefore, the leakage current from the VCO tuning port does not modulates the charge pump current, and does not effect the tuning voltage. Effect of the VCO tuning port leakage current can be seen by performing a transient analysis to the PLL with a Verilog-A behavioural model charge pump is used to replace the charge pump circuit. In the charge pump behavioural model, only the current mismatch effect is included. Results from the simulation show that the tuning voltage is slightly increased, even when both UP and DOWN switches are OFF. Since the behavioural charge pump does not inject any leakage current into the loop filter, so the VCO tuning voltage is only affected by a leakage current from the VCO tuning port that will charge the capacitor in the loop filter.

The current leakage gives a significant effect to the ripple voltage magnitude in a second order loop filter, while only gives a minimum effect to the third order loop filter. A detailed discussion on the effect of loop filter is presented in the next section.

4.3.5 Loop filter order effect

Early in this section, the loop filter is considered as a capacitor. In reality, a second order and third order passive low pass filter are commonly used in the PLL. Here, PLLs with a second and third order low pass filter are referred to as third and fourth order PLL, respectively. A detailed analysis on how these two types of filters affect the VCO tuning voltage is presented in the following paragraphs.

Second order low pass filter

A transfer function of a second order low pass filter as shown in Figure 4.5 is given by

$$F_2(s) = \frac{R_2C_2s + 1}{R_2C_2C_1s^2 + C_1s + C_2s} \,. \tag{4.25}$$

Using Kirchhoff's Current Law , the current that goes through C_1 branch and R_2C_2 branch can be written as

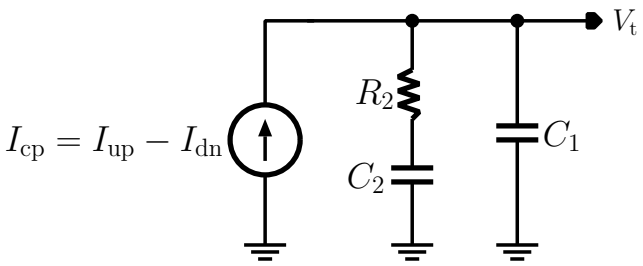


Figure 4.5. Second order low pass filter.

$$I_{C_1}(s) = \frac{I_{cp}}{s} \frac{R_2C_2C_1s + C_1}{R_2C_2C_1s + C_1 + C_2}\,, \tag{4.26}$$

$$I_{R_2C_2}(s) = \frac{I_{cp}}{s} \frac{C_2s}{R_2C_2C_1s + C_1 + C_2}\,. \tag{4.27}$$

Equations 4.26 and 4.27 show that most of charge pump current goes through the C_1 branch. With $R_2C_2C_1s + C_1 \gg C_2s$, we assume that all current goes to C_1. Therefore, the VCO tuning voltage can be represented as

$$V_{t_{fs2}}(t) = \frac{1}{C_1} \int I_{cp}\, dt\,. \tag{4.28}$$

Third order low pass filter

A transfer function of a third order filter as shown in Figure 4.6 is given by

$$F_3(s) = \frac{R_2C_2s + 1}{(R_2C_2C_1s^2 + C_1s + C_2s)(R_3C_3s + 1) + C_3s(R_2C_2s + 1)}\,. \tag{4.29}$$

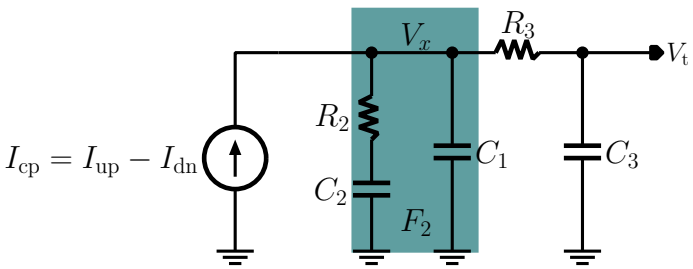


Figure 4.6. Third order low pass filter.

Using Kirchhoff's Current Law, the current that goes through the F_2 branch and R_3C_3 branch can be written as

$$I_{F_2}(s) = \frac{I_{cp}}{s} \frac{(R_2C_2C_1s^2 + C_1s + C_2s)(R_3C_3s + 1)}{(R_2C_2s + 1)C_3s + (R_3C_3s + 1)(R_2C_2C_1s^2 + C_1s + C_2s)} , \tag{4.30}$$

$$I_{R_3C_3}(s) = \frac{I_{cp}}{s} \frac{C_3s(R_2C_2s + 1)}{(R_2C_2s + 1)C_3s + (R_3C_3s + 1)(R_2C_2C_1s^2 + C_1s + C_2s)} . \tag{4.31}$$

Since $(R_2C_2C_1s^2 + C_1s + C_2s)(R_3C_3s + 1) \gg C_3s(R_2C_2s + 1)$, it can be assumed that all the current goes to the F_2 branch. As explained earlier, in F_2 all current is assumed to go through the C_1 branch. Therefore, node V_x in Figure 4.6 can be calculated using Equation 4.28, and current goes through capacitor C_3 is calculated by

$$I_3 = \frac{V_x - V_t}{R_3} . \tag{4.32}$$

The VCO tuning voltage for a third order loop filter can be calculated by

$$V_{t_{fs3}}(t) = \frac{1}{C_3} \int I_3 \, dt . \tag{4.33}$$

4.3.6 Tuning voltage ripple magnitude

A tuning voltage ripple magnitude can be calculated by considering all the circuit non-idealities as explained earlier. The VCO tuning voltage for a PLL with a second ($V_{t_{Fs2}}$) and third order ($V_{t_{Fs3}}$) loop filter is given by

$$V_{t_{Fs2}} = \frac{1}{C_1} \int (i_{up} - i_{dn}) \, dt , \tag{4.34}$$

and

$$V_{t_{Fs3}} = \frac{1}{C_1C_3R_3} \int (i_{up} - i_{dn}) \, dt , \tag{4.35}$$

where i_{up} and i_{dn} are charge pump currents given by Equations 4.22 and 4.23, respectively. The ripple magnitude can be calculated by

$$\Delta V_t = \max(|V_t|) . \tag{4.36}$$

A Matlab script for ΔV calculation is included in Appendix A.1.

4.4 Analysis Verification

For a verification, results from the presented analysis are compared with simulation results using Cadence Spectre tools. Two verifications are conducted, which are a reference spur magnitude based on the analysis in Section 4.2, and a ripple voltage magnitude as discussed in Section 4.3. For the reference spur magnitude verification, ΔV is obtained from a simulation and the reference spur is calculated using Equation 4.14. Meanwhile for the ripple voltage verification, ΔV is obtained based on Section 4.3.6.

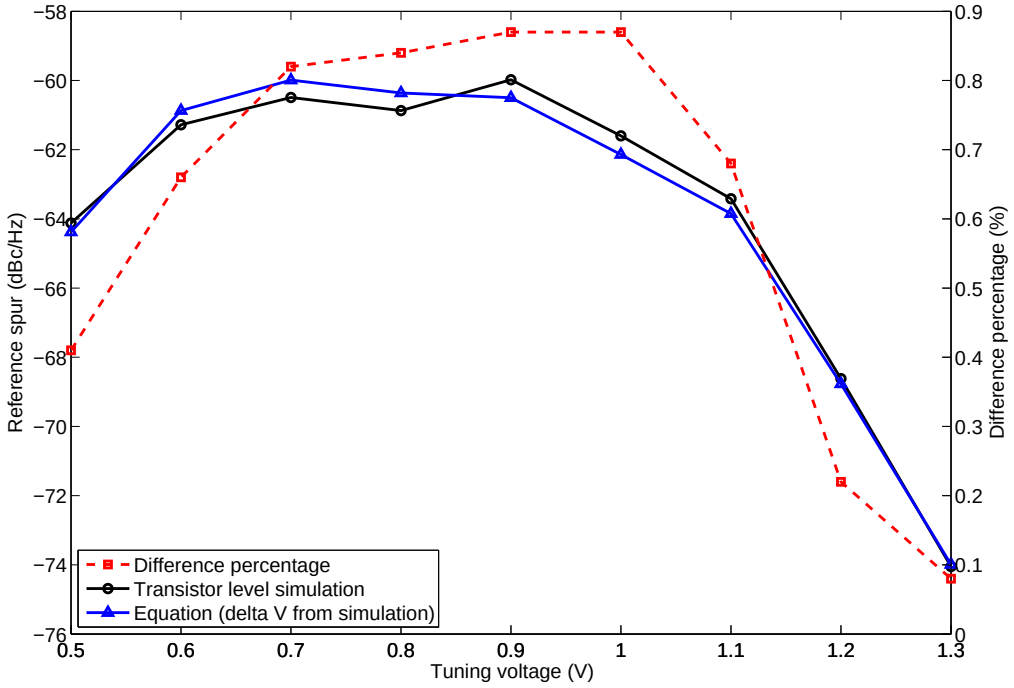
For the Cadence Spectre simulation, a transistor level transient analysis was performed. To obtain a reference spur magnitude, FFT with length of 2^{19} points was applied to the VCO output and the power level difference between the VCO output frequency and the first reference spur were calculated and converted into decibels.

For the spur magnitude verification, ΔV and K_{vco} in the Equation 4.14 are obtained from a transistor level simulation. For ΔV value, the VCO tuning voltage from the transistor level transient analysis is plotted and amplitude of ΔV is obtained. Meanwhile, K_{vco} is attained by plotting the VCO tuning voltage as a function of the VCO output frequency, which is obtained by a Periodic Steady State (PSS) analysis in Cadence SpectreRF. The gradient of the graph at each tuning voltage is K_{vco} for that particular tuning voltage. These values are then applied to Equation 4.14 and the results are plotted on Figures 4.7(a) and 4.7(b), for the third and fourth order PLL, respectively.

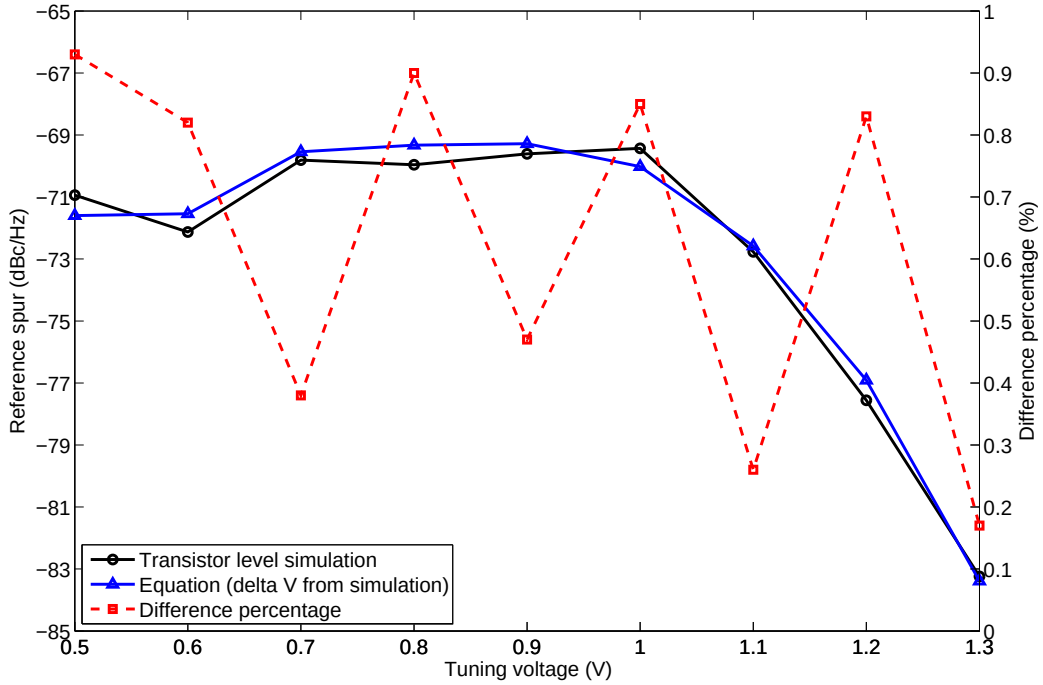
Figures 4.7(a) and 4.7(b) show that the proposed analysis accurately calculates the reference spur magnitude, and is only 1% different to the result obtained by full transistor level simulation. Comparing between these two figures, it shows that with the same loop bandwidth and phase margin, the fourth order PLL (PLL with the third order loop filter) results in reduced reference spurs.

For a ripple voltage verification, ΔV is obtained based on procedures as discussed in Section 4.3.6. Here, K_{vco} is attained by the same means as discussed earlier. Both ΔV and K_{vco} values are then inserted into Equation 4.14 and the results are plotted in Figures 4.8(a) and 4.8(b), for a third and fourth order PLL, respectively.

As shown in Figures 4.8(a) and 4.8(b), a comparison between spur magnitude using the proposed analysis for ΔV estimation, and FFT from transistor level transient analysis gives less than 3% difference.

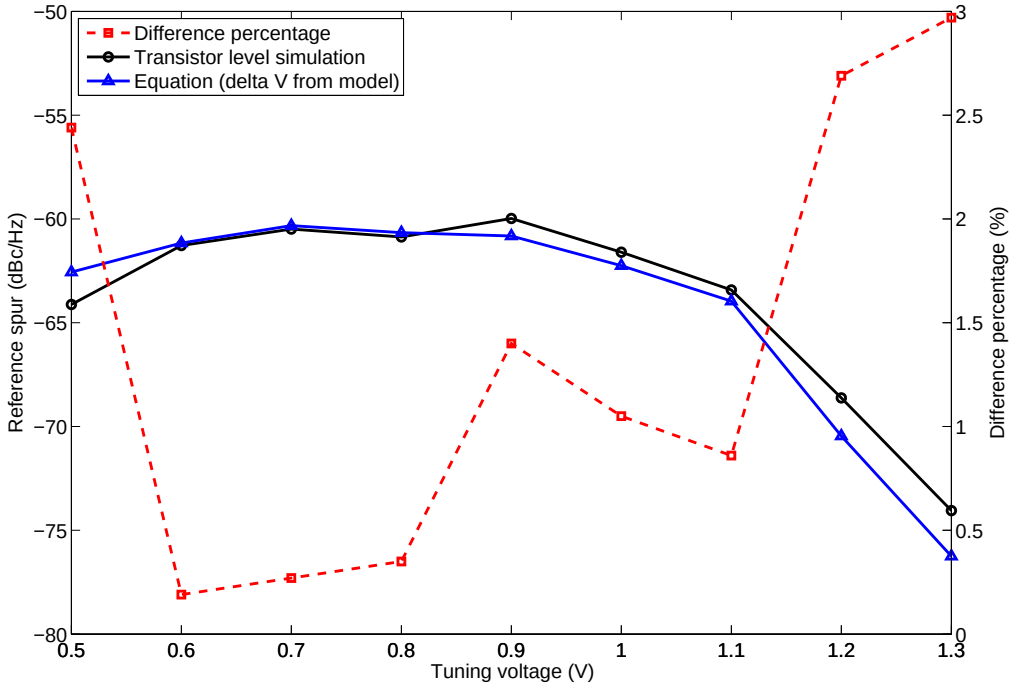


(a) Spur analysis verification for a third order PLL

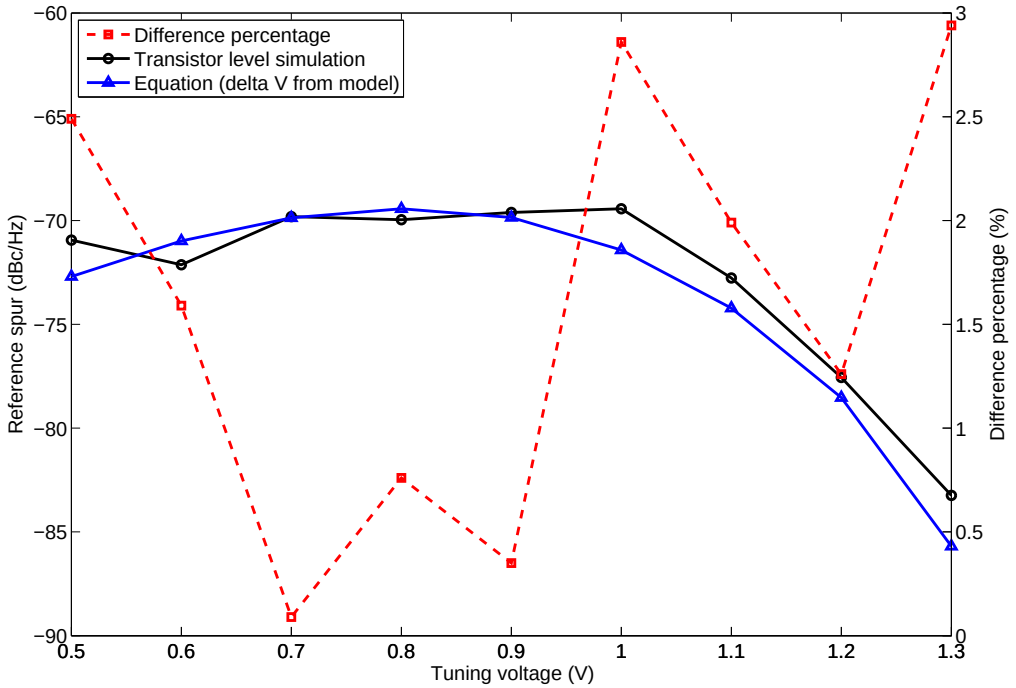


(b) Spur analysis verification for a fourth order PLL

Figure 4.7. Reference spur model verification for a third and fourth order PLL. Reference spur magnitudes are calculated using Equation 4.14 with ΔV value is obtained by a transient analysis at the transistor level simulation. A reference spur magnitude estimation using the proposed analysis in this result is to within 1% of that obtained by full transistor level simulations.



(a) ΔV verification for third order PLL



(b) ΔV verification for fourth order PLL

Figure 4.8. Ripple magnitude (ΔV) model verification for a third and fourth order PLL. Reference spur magnitudes are calculated using Equation 4.14 with ΔV value is obtained by the proposed modelling, and are compared with a transistor level simulation. The differences are less than 3%.

4.5 Effect of Charge Pump Non-idealities

Based on the presented model, effects of charge pump non-idealities on the reference spur magnitude is investigated. As explained in Section 4.3.5, the second order and third order loop filter has a different affect on ΔV. Therefore, a comparison of the affect of charge pump non-idealities between both types of filters is presented. In addition, the affect of the VCO gain on the spur magnitude is also presented, in order to identify the major contributing factor to the reference spurs.

Figures 4.9(a) and 4.9(b) show the effect of VCO gain, charge pump current mismatch and switching delay on the reference spur magnitude for a third and fourth order PLL, respectively. In addition, a current leakage effect is included in the third order PLL (PLL with the second order loop filter). For a current mismatch, two conditions are considered, which are $I_{\text{up}} > I_{\text{dn}}$, and $I_{\text{dn}} > I_{\text{up}}$. For each parameter, the value is increased up to 20%, in steps of 2%.

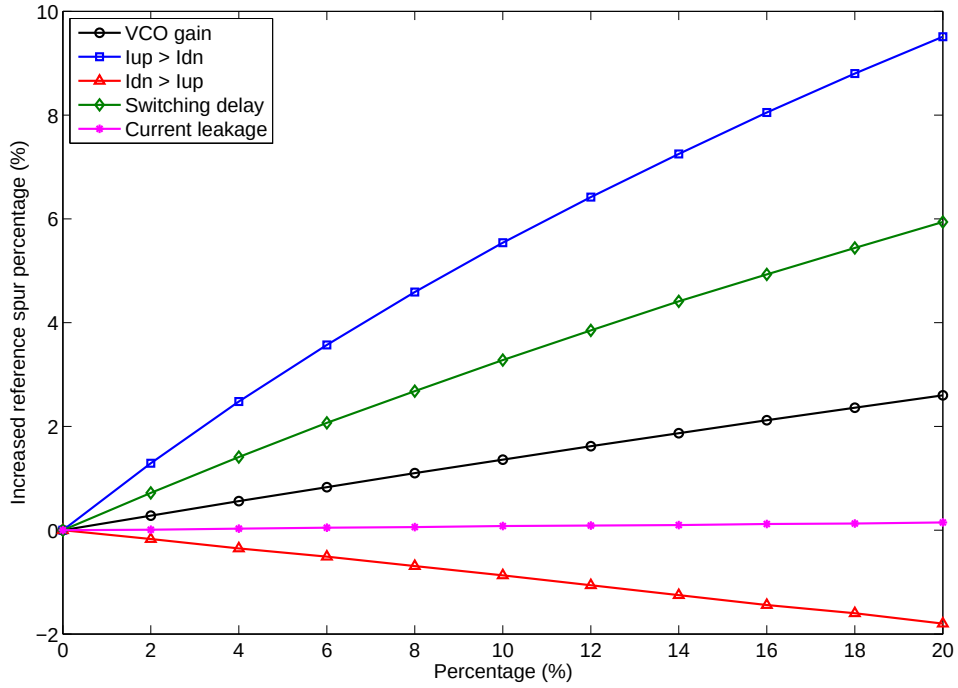
Both Figures 4.9(a) and 4.9(b), clearly show that a current mismatch with $I_{\text{up}} > I_{\text{dn}}$ is the main factor to the reference spur magnitude. On the other hand, $I_{\text{dn}} > I_{\text{up}}$ helps to reduce the spur magnitude.

4.6 Chapter Summary

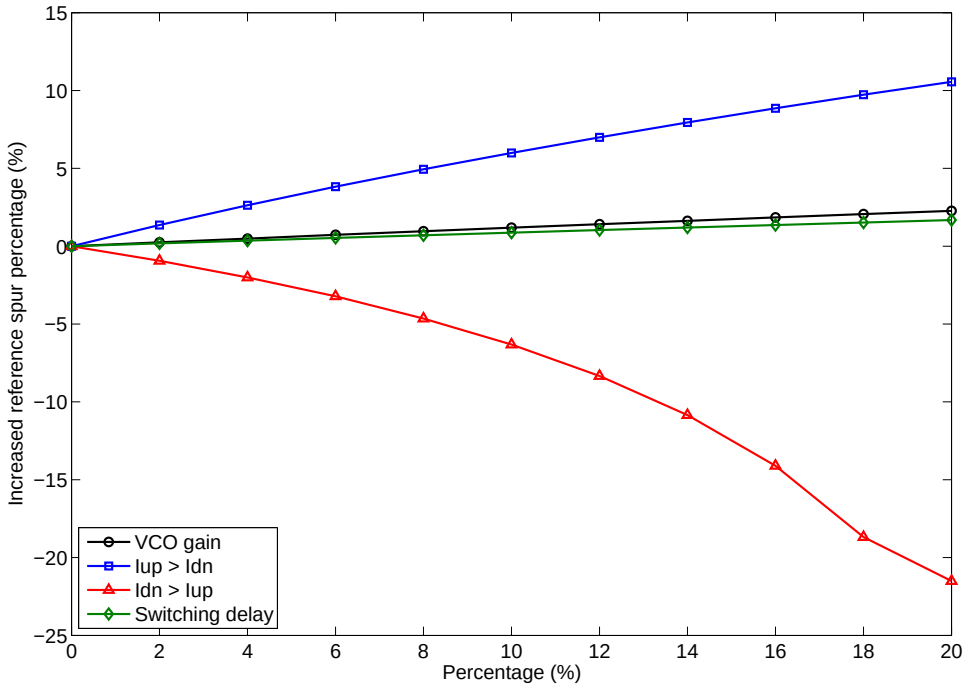
Reference spurs are caused by ripples in the VCO tuning voltage. The ripple voltage is in a form of periodic signal, hence it can be modelled using Fourier series. Employing the frequency modulation theorem, the reference spur is modelled. Analysis in this chapter shows that reference spur has a linear relations with the VCO gain and ripple voltage magnitude, while inversely proportional to the reference frequency. Therefore, a small VCO gain and ripple voltage helps to minimise reference spurs.

Ripples in the VCO tuning voltage are mainly caused by a charge pump current mismatch and switching delay. A slightly larger I_{dn} can improves the spur magnitude, meanwhile the switching delay must be kept as small as possible. In addition, loop filters also affect the reference spur magnitude. A higher order loop filter gives an improved attenuation to the reference spurs.

This chapter presents a comprehensive model for a reference spur in an integer-N PLL. Main causes of the spurs were presented and the affect of each cause on the spur magnitude was investigated. Using the presented analysis, reference spur behavioural



(a) Charge pump non-idealities and the VCO gain effects on a third order PLL



(b) Charge pump non-idealities and the VCO gain effects on a fourth order PLL

Figure 4.9. Effect of VCO gain and charge pump non-idealities on the reference spur magnitude. The current leakage does not effect reference spurs in the fourth order PLL. Here, $I_{\mathrm{up}} > I_{\mathrm{dn}}$ helps to reduce the reference spur magnitude.

modelling can be carried out to achieve an accurate modelling of the spur magnitude before moving to a full transistor level simulation. Therefore, reference spur behavioural modelling is presented in the next chapter.

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Chapter 5

Reference Spur Behavioural Modelling

BEHAVIOURAL modelling helps to estimate PLL performance, dynamic behaviour and stability in a short simulation time before moving to a transistor level design. One of the performance parameters is the PLL reference spur, which can be predicted using a behavioural simulation. For this purpose, all PLL circuit non-idealities that affect the reference spur magnitude need to be included in the behavioural modelling. In this chapter, PLL behavioural modelling for reference spur estimation using Matlab Simulink is presented. The model is designed using the 180 nm SiGe BiCMOS technology. The accuracy of the proposed model is verified by comparing them to a transistor level simulation using a 180 nm SiGe BiCMOS technology.

5.1 Introduction

Simulating PLLs at a transistor level is time consuming, especially when a large dividing ratio is used. A solution to this problem is simulating a PLL at the behavioural level (Rapinoja *et al.* 2006, Mounir *et al.* 2003, Wennan *et al.* 2003). Loop dynamic behaviour, stability, and output performance can be estimated based on the behavioural model simulation result.

Behavioural modelling can be constructed using a top-down or bottom-up design (Demir *et al.* 1994). Top-down design starts the PLL behavioural modelling with a given set of system specifications. Then, the behavioural model determines the PLL architecture and each component specifications in order to achieve the given system specification. In contrast, the bottom-up approach models each PLL component separately, with parameters for each component extracted from transistor level simulation. The components are then combined and simulated together to obtain the PLL performance.

The aim of this work is to estimate reference spurs, dynamic behaviour, and settling time in the PLL output using a behavioural model. As discussed in Chapter 4, the reference spur magnitude is affected by the VCO gain, loop filter, and PFD and charge pump circuit non-idealities, where four different PLL components are involved. Therefore, for a behavioural model verification, the bottom-up design is more suitable at this stage, where each PLL component is modelled separately, and the non-idealities for each component can be included. Then, all the components are combined and simulated together in order to obtain the reference spur magnitude. The spur magnitude can be compared with a transistor level simulation for verifications. The proposed model can also be used for a top-down design, where the designer already sets a targeted reference spur, and fits all the related component parameters to meet the targeted performance.

Much research has been carried out in PLL behavioural modelling (Kuo and Liu 2006, Hanumolu *et al.* 2004, Mao *et al.* 2004, Lagutere *et al.* 2004, Manganaro *et al.* 2003, Kundert 2002, Hinz *et al.* 2000). However, these works concentrate on modelling the PLL phase noise and dynamic behaviour. Only a few works have been reported on modelling the charge pump non-idealities (Rapinoja *et al.* 2006, Mounir *et al.* 2003, Wennan *et al.* 2003, Brigati *et al.* 2001), but the results are not verified. Also, no details are provided on how the non-idealities are modelled.

Behavioural modelling can be implemented in a hardware description language (HDL), such as Verilog-A and VHDL-AMS, or in Matlab Simulink. In HDL, a co-simulation between a behavioural model and the transistor level can be carried out (Yan *et al.* 2009, Hanumolu *et al.* 2004, Mounir *et al.* 2003). The co-simulation gives a better accuracy in predicting phase noise and spurs (Yan *et al.* 2009). However, during circuit designs, several parameters have to be changed before meeting the targeted performance. Changing parameters at the transistor level is not a practical solution as it is time consuming. With a behavioural model, any circuit parameters can be changed easily. Therefore, using a top-down design approach, the proposed behavioural model can assist in identifying and quantifying the circuit parameter that can achieve the targeted reference spur.

The PLL behavioural model starts with a VCO, charge pump, and PFD circuit characterisation in order to identify parameters that affect reference spurs as discussed in Section 5.2. These parameters are then included in the PLL behavioural model in Matlab Simulink as presented in Section 5.3. The behavioural simulation results are compared with a transistor level simulation using Cadence Spectre in Section 5.4. Finally, in Section 5.5 a summary of this approach and its effectiveness is given.

5.2 PLL Behavioural Model Characterisation

Before modelling each component in the PLL, important parameters have to be extracted from the transistor level simulation. For this purpose, Cadence Spectre and SpectreRF simulation tools are used. The components are modelled using a 180 nm SiGe BiCMOS technology provided by Jazz Semiconductor. Methods to extract important parameters from the PFD, charge pump, and VCO that affects the reference spur and PLL settling time from the transistor level simulation are discussed in the following sub-sections.

5.2.1 PFD characterisation

A PFD delay is an important parameter that is included in the behavioural model. The delay is estimated using a transient analysis on the PFD circuit with both input signals have the same phase and frequency as shown in Figure 5.1. The simulation result shows both PFD outputs have a similar signal with a short logic HIGH as shown in

Figure 5.2. This delay is required to eliminate the dead zone effect. The duration of this HIGH signal represents the amount of delay in the PFD circuit.

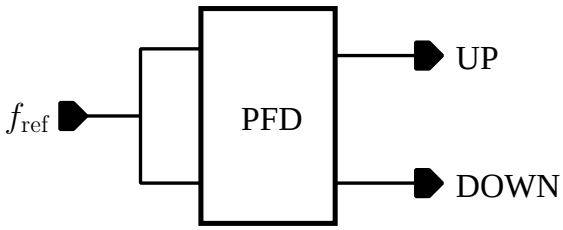


Figure 5.1. PFD simulation setup. This setup is for a PFD delay characterisation. Both PFD inputs are connected to the similar input signal. The PFD outputs, UP and DOWN, have a similar signal with a short logic HIGH.

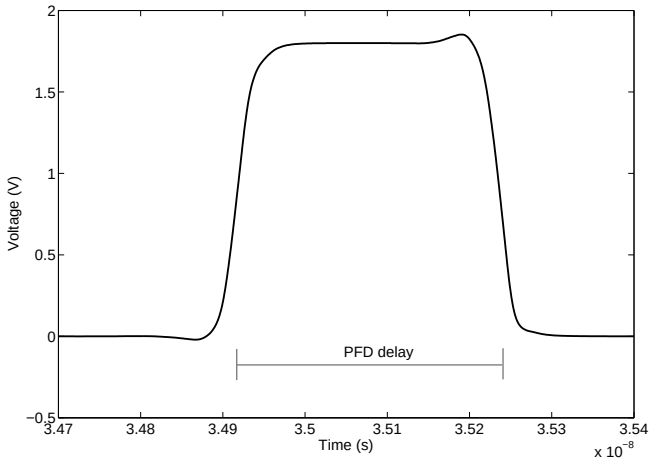


Figure 5.2. PFD timing diagram. A period when both PFD output signals (UP and DOWN) are HIGH simultaneously is referred to as a PFD delay.

5.2.2 Charge pump characterisation

In the charge pump circuit, four parameters are identified to be included in the behavioural model, namely, current leakage, current mismatch between I_{up} and I_{dn}, switching delay, and rise and fall time characteristics of the charge pump current. Characterisation of these parameters is discussed in the following sub-sections.

Charge pump current leakage

A charge pump current leakage can be obtained from a transient analysis on the charge pump circuit. The simulation setup is shown in Figure 5.3, where a PFD is connected to the charge pump input, and a loop filter is connected to the charge pump output. For

the PFD, both inputs are connected to a single reference frequency. The charge pump output current that enters the loop filter is plotted. The leakage current is the current that enters or exits the loop filter when both UP and DOWN charge pump switches are OFF.

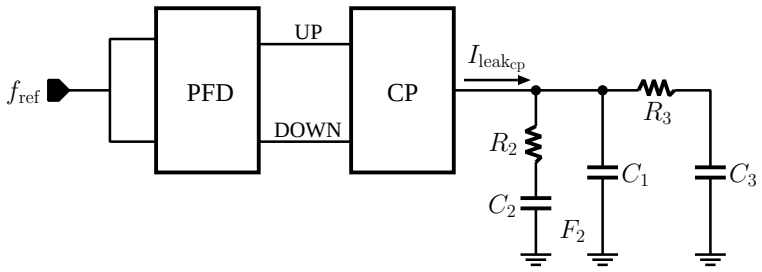


Figure 5.3. Charge pump current leakage simulation setup for a fourth order PLL. The PFD inputs are connected to a similar signal, and the charge pump output is connected to a third order low pass filter. The current leakage is the current that enters or exits the loop filter when both UP and DOWN switches are OFF. For a third order PLL, the loop filter is replaced by a second order low pass filter.

As discussed in Section 4.3.4, a third order PLL (PLL with a second order loop filter) is also affected by a leakage current from the VCO tuning port. The amount of leakage current can be estimated by performing a transient analysis to the VCO with its input connected to the second order loop filter as shown in Figure 5.4. The leakage current charges the capacitor in the loop filter, hence increases the tuning voltage.

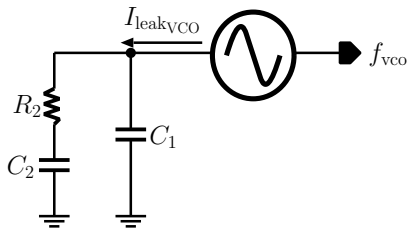


Figure 5.4. A VCO tuning port current leakage simulation setup. A VCO is connected to a low pass filter. Leakage current from the VCO tuning port charges capacitors in the filter.

Charge pump current mismatch

The charge pump current mismatch can be obtained from a DC analysis. For this analysis, both UP and DOWN switches are ON, and the output node is connected to a DC voltage with an initial value at zero. The DC voltage value is then swept up to the

circuit supply voltage, in 50 mV steps. Then both I_{up} and I_{dn} currents are plotted as shown in Figure 5.5.

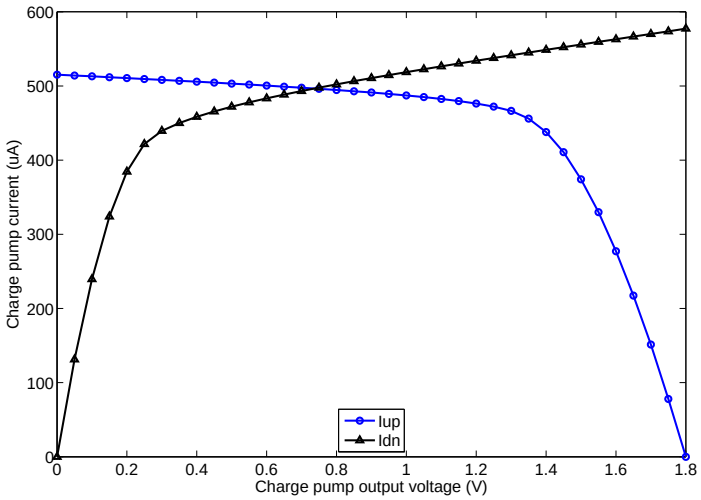


Figure 5.5. Charge pump mismatch current. Here, the I_{up} and I_{dn} values vary depending on the charge pump output voltage.

Switching delay

The delay in UP switch is due to the inverter needed to invert the PFD output signal as explained in Chapter 4. The delay value is estimated from a transient analysis simulation of the inverter.

Charge pump current rise and fall time characteristics

Effect of rising and falling times are modelled as Equations 4.22 and 4.23 in Chapter 4. Rise and fall time constants in the equations can be obtained from a transient analysis, where the rise time constant is the time it takes for the current to reach $1 - e^{-1}$ (63.21%) of its final value, and the fall time constant is the time it takes for the current to decay to e^{-1}(36.79%) of its final value as shown in Figure 5.6. A second order and third order loop filter gives a different time constant, due to a different impedance as seen from the charge pump.

5.2.3 VCO characterisation

The VCO gain (K_{vco}) plays an important role on judging the spur magnitude and settling time. Input to the VCO is a filtered tuning voltage, V_{tune}, and the output is a

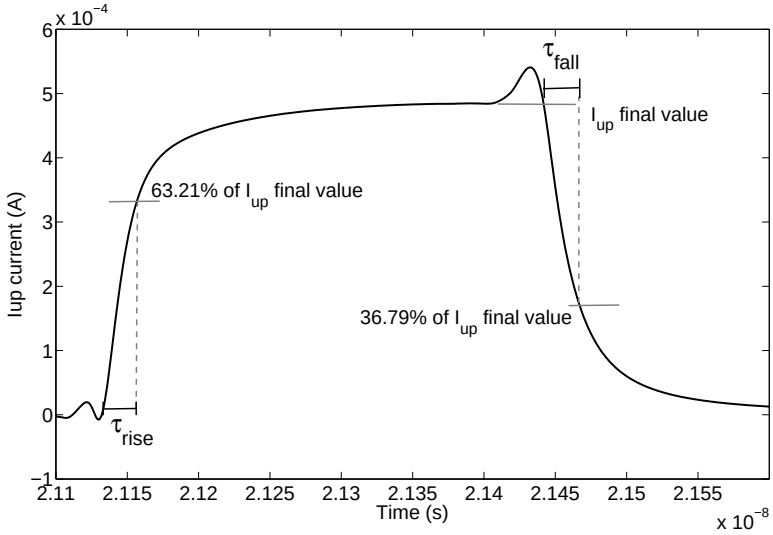


Figure 5.6. Rise and fall time characteristics of I_{up} current. Rise time constant (τ_{rise}) is the time for I_{up} to reach 63.21% of its final value, and fall time constant (τ_{fall}) is the time for I_{up} to reach 36.79% of its final value. The same method is used in the I_{dn} current to determine the rise and fall time constants. The spike on the signal is due to charge injection from switching events (Charles and Allstot 2008), which is not included in the modelling.

sinusoidal signal with frequency f_{o}. The output frequency depends on the tuning voltage and the VCO gain, K_{vco}. Ideally, the relationship between the input tuning voltage and the output frequency is linear, resulting in a constant K_{vco}. Unfortunately, in the real implementation, K_{vco} is only constant in the middle tuning voltage range, while varies at both, low and high tuning voltage as shown in Figure 5.7. The inclusion on this non-linearity in the behavioural model is critical to accurately estimate reference spurs and predicting its settling time. As such variation in the K_{vco} causes a different spur magnitude at different tuning voltages.

The VCO output frequency as a function of the oscillator input tuning voltage as shown in Figure 5.7 is obtained using Periodic Steady-State (PSS) analysis in Cadence. For this simulation, the tuning voltage is changed from 0 to supply voltage (1.8 V), in 50 mV steps.

5.3 Simulink Behavioural Modelling

A third and fourth order PLL behavioural modelling in Matlab Simulink are shown in Figures 5.8(a) and 5.8(b), respectively. The presented model is only applicable to the

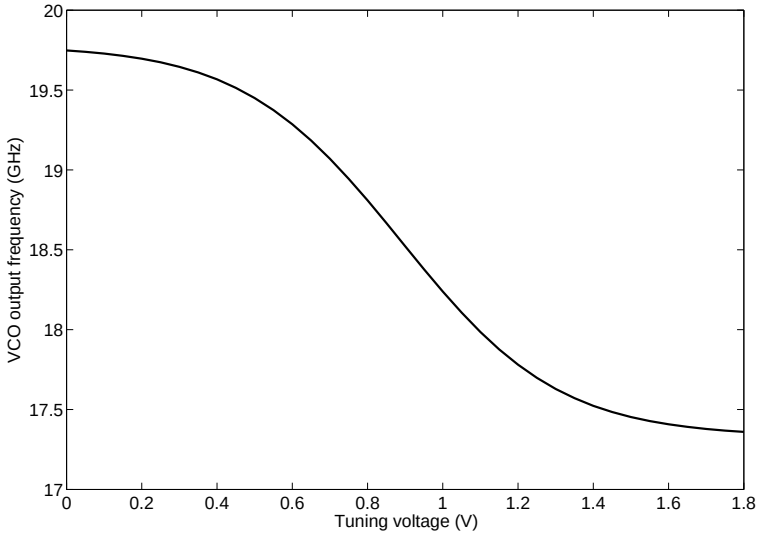


Figure 5.7. VCO output frequency (f_o) as a function of tuning voltage (V_{tune}). The graph slope is the VCO gain (K_{vco}). Here, K_{vco} is only constant in the middle range of tuning voltage, but varied at the low and high tuning voltage.

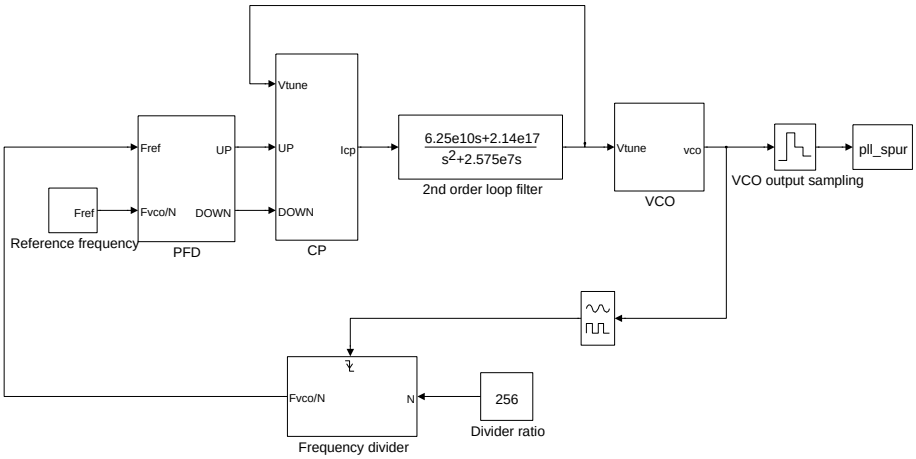
design using the 180 nm SiGe BiCMOS technology, as this technology is used in the PLL components characterisation. However, this modelling can be used for different technology, by using the dedicated technology in the PLL components characterisation. Each component in the PLL is modelled separately, and is discussed in the following sub-sections. For the fourth order PLL model as shown in Figure 5.8(b), the charge pump output voltage, V_x, is different with the VCO tuning voltage. Therefore, a charge pump output voltage transfer function is added to the fourth order PLL modelling. The output of V_x transfer function is fed back into the charge pump module for the charge pump current determination.

5.3.1 PFD Simulink

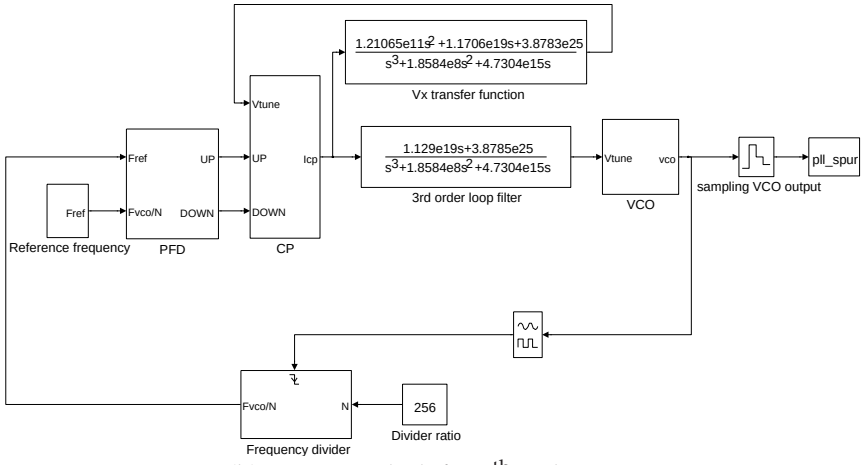
The PFD is constructed by two D flip-flops and a NAND logic gate from the Simulink library as shown in Figure 5.9. A transport delay is used to represent a PFD delay.

5.3.2 Charge pump Simulink

Charge pump currents can be dealt with by an interpolation or curve fitting. For the interpolation method, the tuning voltage and its corresponding current value from a transistor level simulation are stored in a two column array. This array is referred to in



(a) PLL Simulink for 3rd order PLL



(b) PLL Simulink for 4th order PLL

Figure 5.8. PLL Simulink model for a third and fourth order PLL. The PFD and charge pump circuit non-idealities are included in the modelling for reference spur estimation. An extra transfer function, V_X, representing the charge pump output voltage, is required in the fourth order PLL in order to determine the charge pump current. For the third order PLL, the charge pump output and the VCO tuning voltage is similar.

the behavioural model simulation whenever a charge pump current value is needed. If an exact value is not available in the array, an interpolation between two adjacent points is performed. In Simulink, a lookup-table can be used for this method.

For the second method, a curve fitting technique is used to obtain a polynomial equation that relates the tuning voltage and charge pump currents (Rapinoja *et al.* 2006). The polynomial order depends on the non-linearity between the tuning voltage and the current.

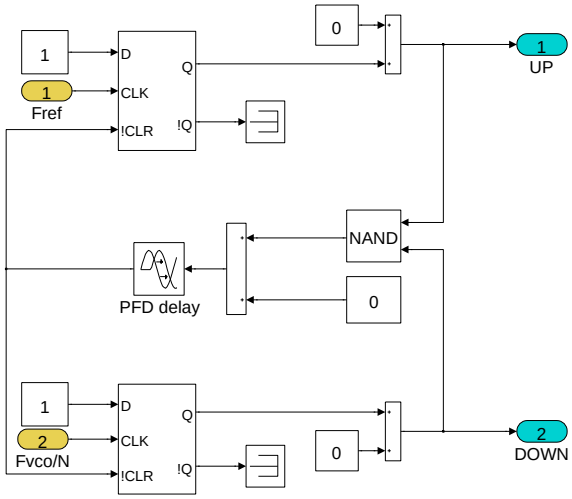


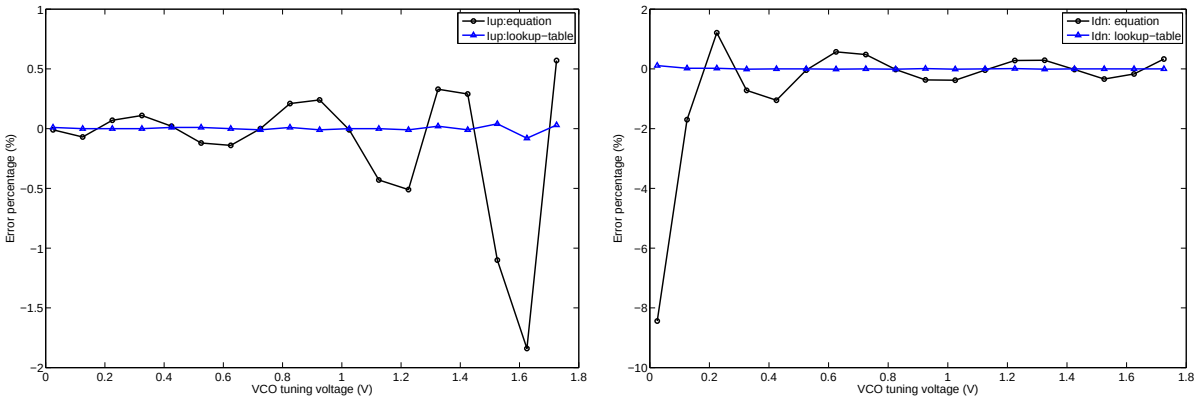
Figure 5.9. PFD Simulink model. Two D flip-flops and a NAND gate are used to model the PFD. A transport delay is used to represent the PFD delay.

Figure 5.10 shows a comparison between the interpolation and curve fitting method for I_{up} and I_{dn} current modelling, respectively. For the lookup table, charge pump current values corresponding to the tuning voltage between 0 and 1.8 V, in 50 mV steps are generated. Meanwhile, in the curve fitting method, an 8^{th} order polynomial is required. It must be mentioned that the order of the polynomial is circuit and technology dependent. Then, the percentage difference between the interpolation and curve fitting method when compared to transistor level simulations are plotted in Figure 5.10.

Figure 5.10 shows that the interpolation method gives a better accuracy when compared to the curve fitting method, with a difference percentage of less than 0.15%. Therefore, a lookup table is chosen for the Simulink model.

Figure 5.11 shows the charge pump Simulink behavioural model. The model has three input ports, namely, V_{tune}, UP and DOWN. Here, V_{tune} is from charge pump output voltage, which is also the VCO tuning voltage if a second order loop filter is used, and UP and DOWN are from PFD outputs. Meanwhile, the V_{tune} port is coupled into two lookup tables, in order to determine I_{up} and I_{dn} values.

For the UP port, a transport delay is inserted to represent the switching delay. The DOWN and delayed UP signals are connected to a sub-system as shown in Figure 5.12 to insert rise and fall time characteristics. As given in Equations 4.22 and 4.23, both the delayed UP and DOWN signals are divided into two parts, where the first part starts at the rising edge until the falling edge, and the second part starts at the falling edge until the next rising edge. The first part is for the rise time insertion, and is



(a) I_{up} (b) I_{dn}

Figure 5.10. Charge pump current: a comparison between interpolation and curve fitting methods. The interpolation method is implemented using a lookup-table, and for the curve fitting, an 8^{th} polynomial equation is used to represent the charge pump current. It is clearly shown in the both graphs that the interpolation method has a lower difference percentage when compared to the curve fitting method. Therefore, a lookup-table is used in the charge pump Simulink model.

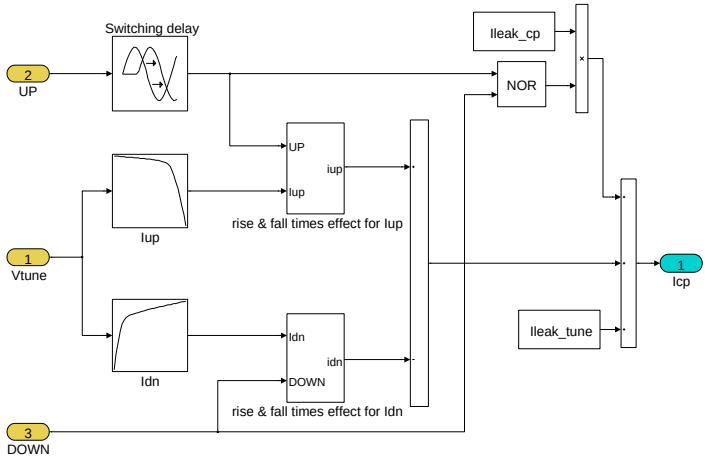


Figure 5.11. Charge pump Simulink model. Charge pump non-idealities, namely, current mismatch, switching delay, and rise and fall time characteristics are included in this behavioural model. The switching delay is represented by a transport delay, and a constant named I_{leak}_cp is added to the charge pump output to represent the current leakage. Meanwhile, the rise and fall time characteristics are modelled in a sub-system as shown in Figure 5.12.

given by $1 - e^{(-t/\tau)}$, while the second part is the fall time insertion, and is given by $e^{(-t/\tau)}$, where t is obtained by the integrators, and τ are attained by charge pump characterisations, as explained in Section 5.2.2. These signals are then combined by using a switch.

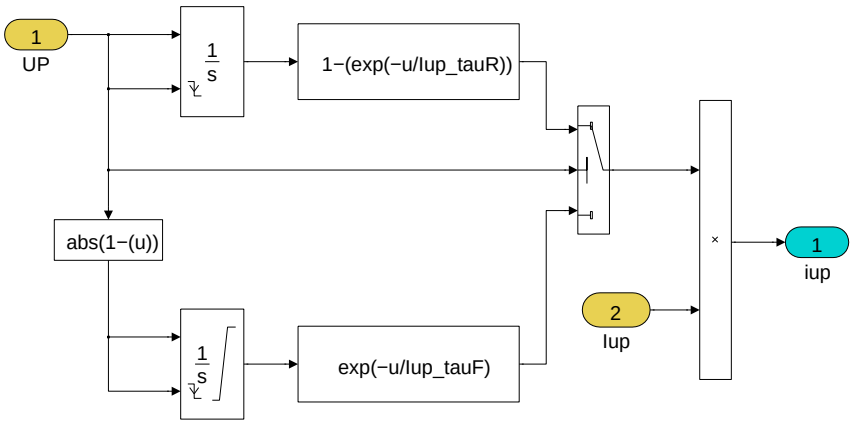


Figure 5.12. Rise and fall time characteristics sub-system. This model inserts the affect of rise and fall time characteristics on the charge pump currents. The UP port is connected to the delayed UP signal, and I_{up} port is connected to I_{up}, which is given by a lookup-table in the Simulink charge pump model.

The UP and DOWN signals with the rise and fall time effects are multiplied with I_{up} and I_{dn} from the lookup-table, respectively. Then, $I_{up} - I_{dn}$ is obtained to represent the current component that either enters or exits from the loop filter.

A charge pump current leakage is also included in the Simulink model. The leakage current value can be obtained from a transistor level simulation as explained in Section 5.2.2. The leakage current only exists when both UP and DOWN switches are OFF. For the third order PLL model, the VCO tuning port current leakage is also included.

This charge pump model helps to accurately simulate the PLL settling time, since the charge pump current non-linearity is taken into account. As shown on Figure 5.10, when the tuning voltage close to 0 V or the supply voltage (1.8 V in this case), I_{up} and I_{dn} values are very different, and present a significant influence on the PLL settling behaviour. Using the presented model, such effects can be modelled and quantified.

5.3.3 Loop filter Simulink

The loop filter is modelled by a transfer function in the Simulink library. The transfer function of a second and third order loop filter is given in Equations 4.25 and 4.29, respectively.

For the third order loop filter as shown in Figure 4.6 in Chapter 4, V_x is the charge pump output voltage, and its value is needed to be fed back into the charge pump model in order to determine the charge pump current. The value of V_x can be obtained by its transfer function, as given by

$$\frac{V_x(s)}{I_{cp}(s)} = \frac{(R_2C_2s+1)(R_3C_3s+1)}{(R_2C_1C_2s^2+C_1s+C_2s)(R_3C_3s+1)+C_3s(R_2C_2s+1)} . \tag{5.1}$$

5.3.4 VCO Simulink

Much research has been published on the VCO behavioural modelling (Centurelli *et al.* 2004, Buonomo and Schiavo 2004, Costantini *et al.* 2002). However, the focus on these publications is on modelling the VCO phase noise. By contrast, this work only focuses on the PLL reference spur modelling. Therefore, for simplicity, phase noise modelling is not included in this VCO and due to the fact that phase noise study of PLLs is already well covered in the literature.

Similar to the approach presented for the charge pump, the VCO behavioural model can also be implemented using an interpolation (Harasymiv *et al.* 2010), or a curve fitting (Mounir *et al.* 2003, Wennan *et al.* 2003) method. As explained in Section 5.3.2 a lookup table is used for the interpolation technique, while a polynomial equation is used for the curve fitting method. The VCO output frequency as a function of tuning voltage from 0 to 1.8 V, in 50 mV steps, is also obtained from a transistor level simulation, and a lookup table is generated. Meanwhile, for the curve fitting method, a 7^{th} order polynomial is used. Difference frequencies for these two methods when compared to VCO frequencies, obtained from the PSS analysis in Cadence SpectreRF, are shown in Figure 5.13. The figure shows that the interpolation approach gives improved accuracy, with a maximum frequency difference of less than 2 MHz. The accuracy can be improved by expanding the lookup-table data.

A VCO phase model is used for the VCO Simulink behavioural model as shown in Figure 5.14. The input port named V_{tune} is from the tuning voltage given by the loop

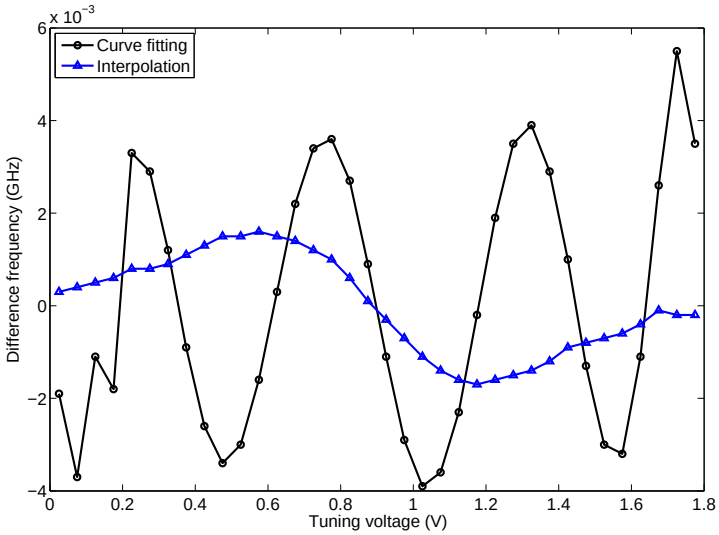


Figure 5.13. VCO frequency: a comparison between the interpolation and curve fitting method. The interpolation method gives a better accuracy with a maximum frequency difference of less than 2 MHz. Similar to the charge pump model, the interpolation method is implemented using a lookup-table, and for the curve fitting, a 7^{th} polynomial equation is used to represent the VCO frequency.

filter transfer function. This port is connected to the lookup table in order to determine the VCO output frequency. Then, the VCO phase is calculated by

$$\theta_{\text{vco}} = 2\pi \int f_{\text{vco}}\, dt \tag{5.2}$$

The VCO signal is attained by applying a cosine function to the phase, θ_{vco}.

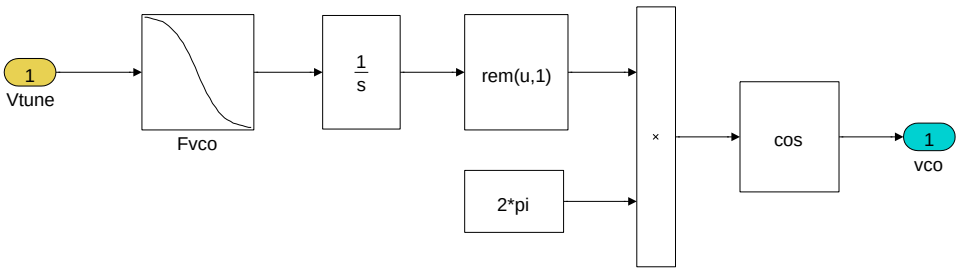


Figure 5.14. VCO Simulink model. A lookup-table from Simulink library is used to determine the VCO frequency according to its V_{tune} input port. The rem$(u,1)$ function is to ensure the VCO phase is bounded between zero and 2π.

Similar to the charge pump current issue, when the tuning voltage around 0 V and the supply voltage (1.8 V in this case), the VCO gain is much lower when compared to the value at the middle range tuning voltage. Therefore, the PLL tracking is much slower

around these regions. This effect can be simulated using this VCO model, hence an accurate settling time for the PLL can be predicted.

5.3.5 Frequency divider Simulink

A frequency divider can be modelled using a triggered subsystem as shown in Figure 5.15. Inputs of the model are a dividing ratio and a VCO signal, which is used as a clock to the subsystem. Output of the model is a square wave signal with a frequency that given by f_{vco}/N, where f_{vco} is the VCO signal frequency, and N is the division ratio.

In each clock cycle, a variable (initial value is zero) is increments by 1, and the resulting value is divided by the division ratio. The remainder of the division is compared to the half of dividing ratio. If the value is less than $N/2$, then the output signal is at logic HIGH, and vice versa. This comparison is utilised to produce an output signal with a 50% duty cycle.

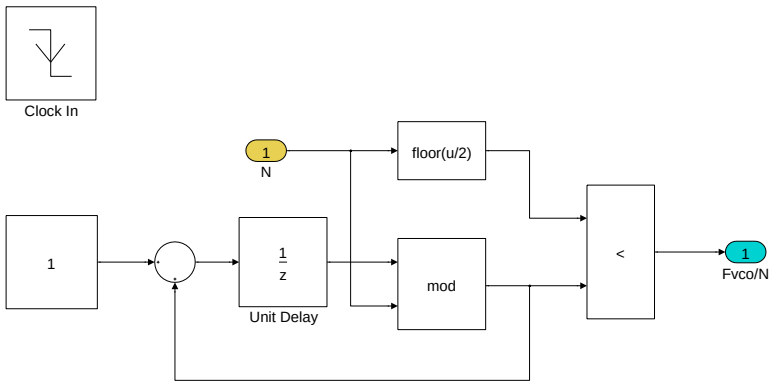


Figure 5.15. Frequency divider Simulink model. Here, N is the division ratio. The system is clocked by the VCO output.

5.4 PLL Behavioural Modelling Result

The proposed model is aimed for a reference spur and settling time estimation. A comparison between results obtained from the Simulink model and transistor level simulation is presented in the following sub-sections.

5.4.1 Reference spur

Reference spurs can be obtained from the proposed Simulink model by calculating Power Spectral Density (PSD) of the VCO output. The first offset reference spur for nine different VCO output frequencies are obtained. These data are then compared with reference spur magnitudes from a transistor level simulation as shown in Figures 5.16(a) and 5.16(b), for a third and fourth order PLL, respectively. In these figures, the reference spur magnitude is only less than 3% and 4%, for the third and fourth order PLL, respectively, different to the result obtained by full transistor level simulation.

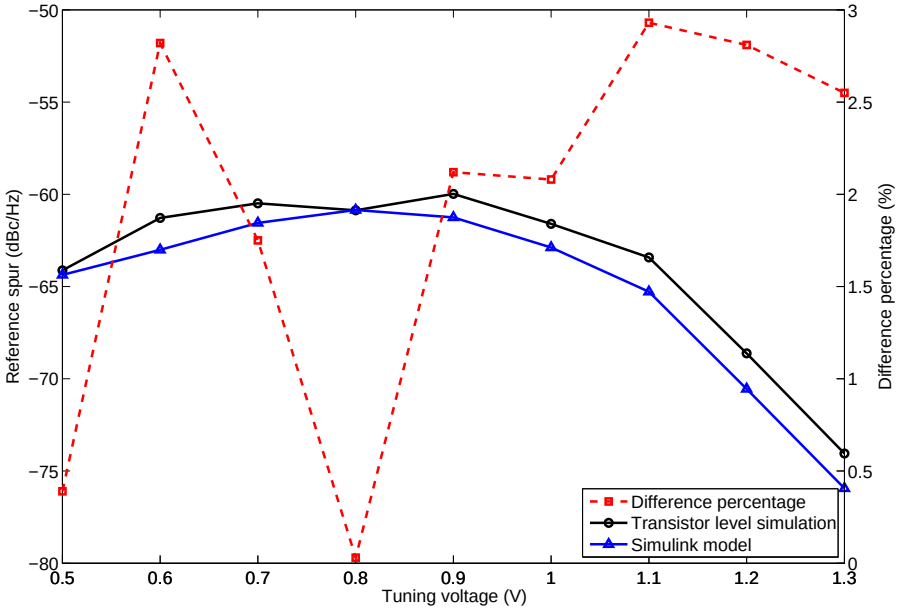
5.4.2 PLL settling time

Non-idealities in the PFD, charge pump and VCO circuit are included in the proposed Simulink model, resulting in an accurate settling time simulation. Figures 5.17(a) and 5.17(b) show a comparison in PLL settling time between the Simulink model proposed in this work and a transistor level simulation, for a third and fourth order PLL, respectively. Using this proposed Simulink model, a dramatic reduction in simulation time is achieved without compromising the performance estimation accuracy.

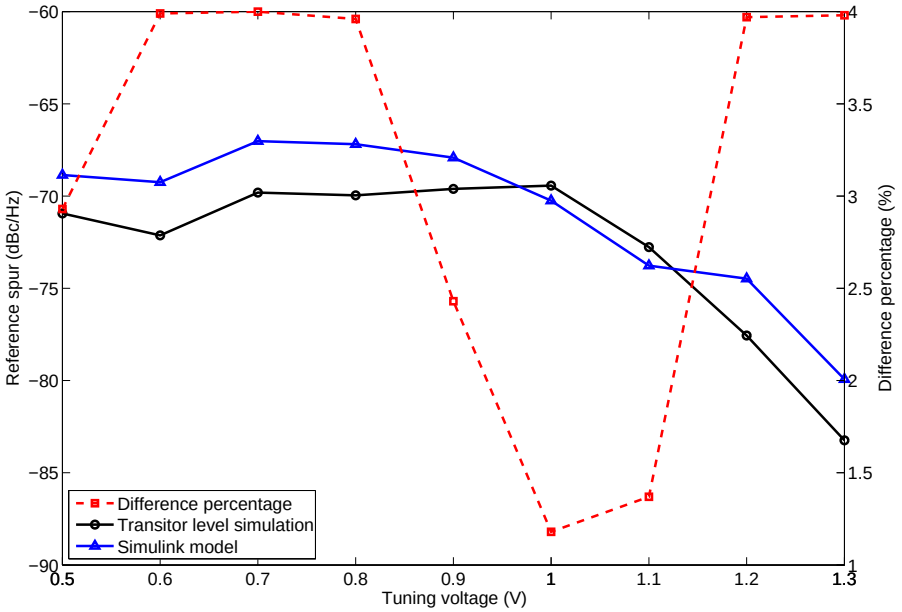
5.5 Chapter Summary

A PLL behavioural model has been developed in Matlab Simulink. A bottom-up approach is used, where each PLL component is modelled separately, and are combined together for the simulation. The Simulink model includes PFD and charge pump non-idealities, in order to accurately estimate the reference spur magnitude and settling time. For a model verification, reference spurs and tuning voltages from the Simulink model are compared with results from a transistor level simulation. The reference spur comparison results in less than 3% and 4% for the third and fourth order PLL, respectively. The tuning voltage response for both, the third and fourth order PLL is also similar to the transistor level simulation.

Having investigated the PLL reference spur behavioural modelling in this chapter, it is now raises the question of how to suppress the reference spur, and therefore this is what we now discuss in the next chapter.

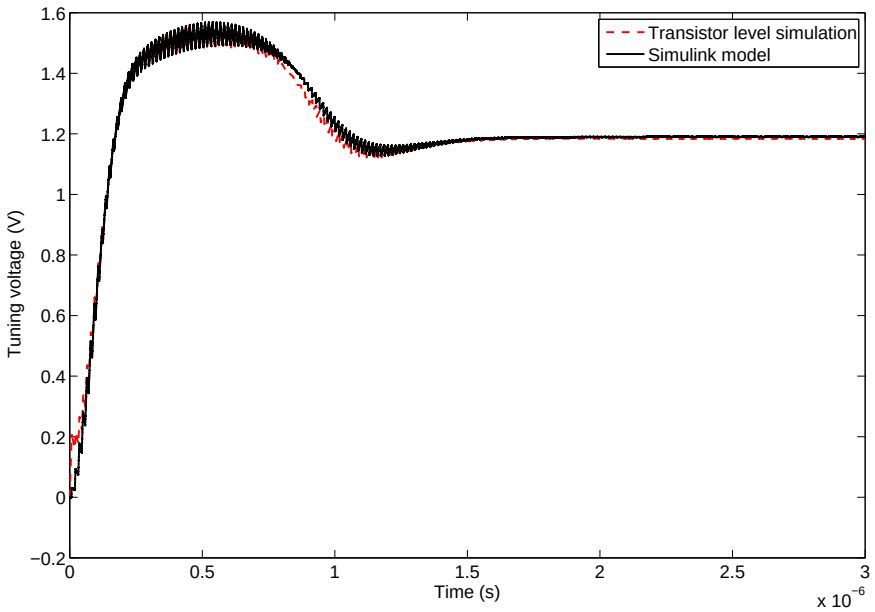


(a) Reference spur comparison for a third order PLL

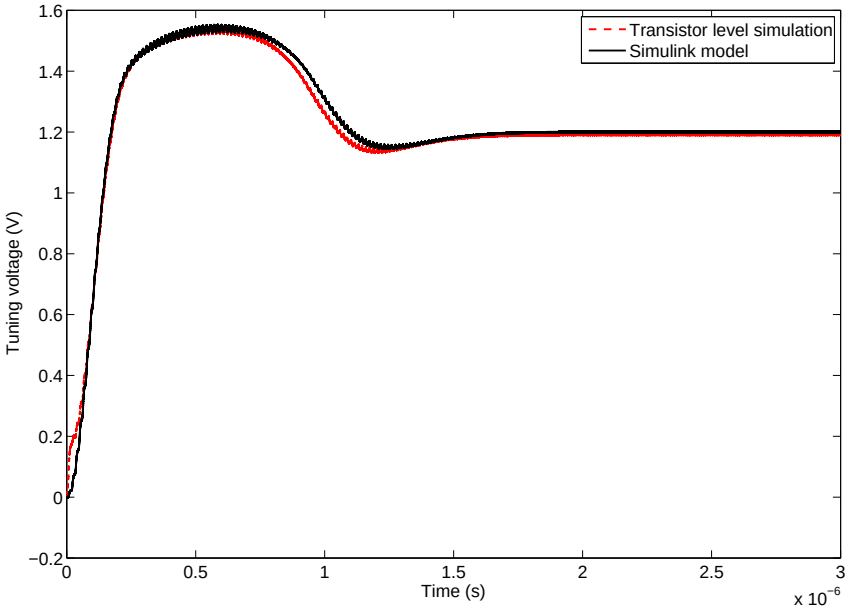


(b) Reference spur comparison for a fourth order PLL

Figure 5.16. Reference spur magnitude comparison between transistor level simulation and Simulink model for a third and fourth order PLL. The percentage difference for the third order PLL is less than 3%, while for the fourth order PLL, the difference percentage is less than 4%.



(a) Tuning voltage comparison for a third order PLL



(b) Tuning voltage comparison for a fourth order PLL

Figure 5.17. VCO tuning voltage comparison between a transistor level simulation and Simulink model for a third and fourth order PLL. The settling time for both, the transistor level simulation and Simulink model are about the same. The tuning voltage response of the third order PLL is similar to the fourth order PLL, therefore the settling time also is almost similar. This is because, the loop filter design for both PLLs have the same loop bandwidth and phase margin.

Chapter 6

Spur Suppression Design Technique

REFERENCE spurs in the PLL output can be minimised by lowering the VCO gain and ripple voltage or increasing the reference frequency. A crystal oscillator is normally used as the reference frequencies, thus the choice of frequency is limited to the crystal oscillator frequencies available on the market. Lowering the VCO gain and voltage ripple can be implemented by several design techniques. This chapter reviews several techniques to minimise reference spurs in the PLL. In addition, a new technique to improve reference spur performance is presented. The technique uses a ratioed current charge pump, which is designed so that I_{dn} is larger than I_{up} at an optimum ratio. A method to calculate the optimum charge pump current is presented in this chapter. For performance evaluation, the reference spur magnitude for the new technique is compared to a conventional PLL.

6.1 Introduction

Reference spurs in a PLL cannot be completely eliminated, but can be minimised. Several approaches have been carried out to suppress reference spurs. Some of these approaches concentrate on redesign of the circuitry that affects the reference spur magnitude, such as the VCO, PFD, and charge pump. Meanwhile, several other approaches push the spur offset frequency to a higher frequency than the reference frequency. These reference spur suppression design techniques are reviewed in the following section.

From the analysis in Chapter 4, current mismatch significantly affects the reference spur magnitude, and a slightly I_{dn} larger than I_{up} helps to reduce the spur magnitude. An optimum I_{dn} to I_{up} ratio is important to obtain the minimum reference spur magnitude. This current ratio can be implemented in the charge pump circuit by resizing transistors in the current mirror circuit. A detailed discussion on how to determine the optimum ratio and its implementation in the charge pump is presented in this chapter.

A review of reference spur suppression techniques is presented in Section 6.2. Then, a low reference spur technique, namely, a ratioed current charge pump, is discussed in Section 6.3. Next, Section 6.4 presents a reference spur magnitude comparison between the PLL with a ratioed current charge pump and a conventional PLL. Finally, this chapter is summarised in Section 6.5.

6.2 Reference Spur Suppression Technique Reviews

A low reference spur is one of the main challenges in PLL design, especially in present technology where a low supply voltage is commonly used due to voltage scaling. The low supply voltage helps to reduce power consumption, however it causes a large VCO gain to be used to cover a wide VCO tuning range, hence increasing the reference spur.

Many approaches have been carried out for reference spur suppression. One of these techniques is by lowering the VCO gain, while maintaining a wide VCO output frequency range (Cho *et al.* 2010, Kim *et al.* 2008, Kuo and Liu 2006). Another method to suppress the reference spur magnitude is by minimising the ripple voltage on the VCO tuning voltage. This can be achieved by reducing current mismatch and current leakage in the charge pump. In this section, several reference spur suppression design techniques are reviewed.

6.2.1 Low VCO gain

As discussed in Chapter 4, the VCO gain, K_v, is proportional to reference spur magnitude. Therefore, a low VCO gain is required to obtain low reference spur and phase noise. However, with a low supply voltage, normally a high VCO gain is used to provide a wide tuning range, as required by the system specification.

One technique to achieve a wide tuning range while maintaining a small VCO gain is by using a VCO with two or more control ports. This technique can be implemented in several ways. One way is by using a switched-capacitor VCO, where an array of switched capacitors are connected in parallel to the varactor as shown in Figure 2.21 (Lou *et al.* 2011, Nariman *et al.* 2010, Shu *et al.* 2010, Deng and Kiang 2009, Berny *et al.* 2005). The varactor is tuned by a voltage from the loop filter, and each capacitor is controlled by a switch, where digital signals are required to control these switches. When the switch is ON, the capacitor and varactor are in parallel, resulting in a higher capacitance, hence a lower VCO frequency is obtained. When all the switches are OFF, the capacitance is only given by the varactor, and results in the maximum VCO frequency. Therefore, the digital signals that control the capacitor switches determine the VCO frequency band.

The switched capacitor VCO enable a small varactor to be used in a wide tuning range VCO. The small varactor provides a small VCO gain, hence produce a small reference spur. However, the switched capacitor increases the VCO design complexity. The varactor size and number of capacitors have to be chosen properly in order to meet the system requirement. In addition, the switch on-resistance reduce the overall tank quality factor, hence excessive number of switched capacitor can worse phase noise (Deng and Kiang 2009, Stagni *et al.* 2008). Also, the switch parasitic capacitance reduces the tuning range (Stagni *et al.* 2008).

Another technique to implement a low VCO gain is by using a dual loop PLL, where two loops, namely, coarse tuning and fine tuning loop control the varactors (Cho *et al.* 2010, Herzel *et al.* 2008b, Kuo *et al.* 2006, Glisic and Winkler 2006, Winkler *et al.* 2005). The coarse tuning loop contains a large varactor to cover a wide tuning range, while the fine tuning loop couples into a small varactor. The dual loop PLL requires two charge pumps and two loop filters. The coarse tuning loop is coupled into a large capacitor to suppress reference spur caused by the large VCO gain from the large varactor (Herzel *et al.* 2003). Therefore, the reference spur is mainly contributed by the fine

tuning loop. A low reference spur is expected because the fine tuning loop consists of a small varactor with a low VCO gain.

6.2.2 Improved charge pump circuit

Minimising the charge pump current mismatch helps to improve reference spur performance. The current mismatch can be reduced by using a high output impedance for the charge pump, and this can be implemented by using a cascode current source topology (Rhee *et al.* 2000, Lee *et al.* 1999). However, the cascode topology increases the voltage headroom, hence limits the VCO tuning voltage, which is not appropriate for a low supply voltage circuit. This limitation is addressed by using a gain boosting circuit to increase the charge pump output impedance without increasing the voltage headroom (Mekky and Dessouky 2007, Choi and Han 2006).

Another current matching technique is by using a current compensation circuit, where either I_{up} or I_{dn} is unchanged, while the other current is increased or decreased to match the unchange current value. For example, for fixed I_{up}, a current compensation circuit is implemented in the I_{dn} current source, so that I_{dn} is matched with I_{up}. Current compensation can be implemented by using a digitally controlled bias generator (Liang *et al.* 2008, Huh *et al.* 2005) or an error amplifier (Hwang *et al.* 2009, Lee and Hajimiri 2000). The bias generator consists of an array of current sources. Each generator is controlled by an array of switch as shown in Figure 6.1. A control circuit is required to provide the digital signals to control the switches and sets the bias current value, which is must be matched to the other current.

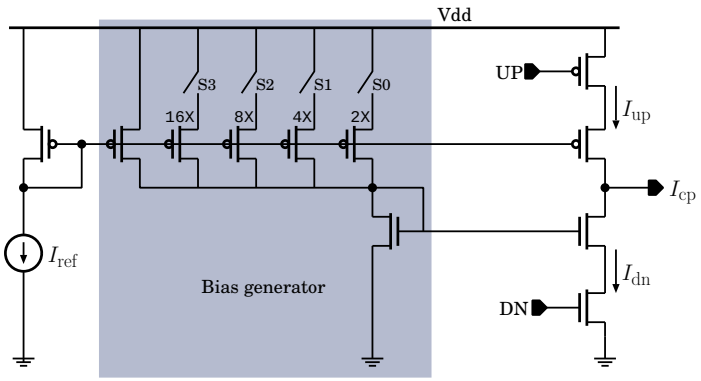


Figure 6.1. Charge pump with bias generator circuit. Here, the I_{up} is fixed, while I_{dn} is set to match I_{up}. Combination switches S0, S1, S2, and S3 are used to obtain the I_{dn}.

The current compensation circuit also can be implemented by using an error amplifier to compare charge pump output voltage at node A with a reference voltage at node B (Huan *et al.* 2011, Hwang *et al.* 2009, Lee and Hajimiri 2000) as shown in Figure 6.2. The difference voltage adjusts the current bias voltage, so that the voltage at node A equals to node B, hence I_{up} equals to I_{dn}.

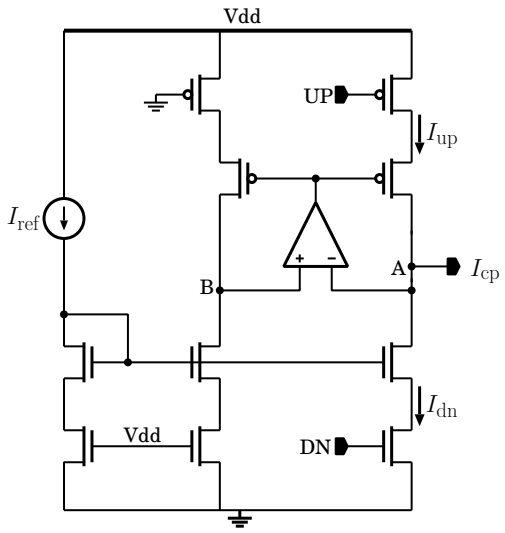


Figure 6.2. Charge pump error amplifier compensation circuit. An error amplifier is used to compare V_{cp} at node A with V_{ref} at node B. Output of the amplifier adjusts the I_{up} current mirror bias voltage according to the difference voltage between node A and B, results in a matching current between I_{up} and I_{dn}.

A charge pump current also can be matched by using a sub-sampling phase detector (SSPD) together with amplitude controlled charge pump (Gao *et al.* 2010). The SSPD directly samples the high frequency VCO signal with a low frequency reference signal. The phase difference between these signals is converted into a sampled voltage difference, which is then used to control I_{up} and I_{dn}. The charge pump current values will be dependent on the sampled voltage difference. Here, I_{up} and I_{dn} are switched ON and OFF simultaneously by a pulse generator circuit. Both I_{up} and I_{dn} have a similar constant ON time, which is determined by the pulse generator, with the different current values depends on the phase difference between VCO and the reference signal. Therefore, no ripple on the tuning voltage exists as the switching occurs simultaneously and the current values are matched by the SSPD and amplitude controlled charge pump.

Another factor causing reference spurs is the charge pump current leakage. The leakage current problem can be solved by a leakage current compensation circuit (Chuang and Liu 2006, Xiaozhou *et al.* 2009). In Chuang and Liu (2006), a replica charge pump

and operational amplifier are used to determine the amount of leakage current, and a leakage current generator circuit is designed to compensate the leakage current. Meanwhile, in Xiaozhou *et al.* (2009) an auxiliary tuning loop, which consists of a PFD, voltage integrators, and voltage controlled current source (VCCS), is used to compensate for the amount of leakage current. The auxiliary tuning loop is only active after the PLL is locked.

6.2.3 Other methods

Besides a low VCO gain and low charge pump current mismatch and leakage, there are several other techniques utilised to improve the reference spur performance. One of the techniques is by using a charge-distribution mechanism, where the comparison between VCO and reference signals are distributed into several consecutive times (Choi *et al.* 2012, Lee and Lee 2006, Park and Mori 1991). This can be implemented by using multiple pairs of PFD and charge pump (Lee and Lee 2006, Park and Mori 1991) or inserts an edge-interpolator circuit before the charge pump circuit (Choi *et al.* 2012). As the phase and frequency comparison between the VCO and reference signal occurs n times higher when compared to a conventional PLL, the charge pump current has to be $1/n$. This technique pushes the reference frequency offset far away from the output frequency (Choi *et al.* 2012).

Another method to push the offset frequency much higher than the reference frequency is by using a frequency booster circuit before the charge pump (Elsayed *et al.* 2011). Therefore, the PFD output frequency is higher than the reference frequency. In Liang *et al.* (2007), a two-path switched capacitor network is included between the charge pump and the loop filter to double the spur frequency. The capacitor switching are designed to redistribute the ripple voltage twice to the loop filter in a reference cycle period. Therefore, the spur frequency offset is double of reference frequency. The drawback of this design is that the charge injection and clock feedthrough from the switches introduce an additional ripple voltage, hence increase the spur magnitude (Liang *et al.* 2007). Alternatively, a double sampling phase detector is used in Huang *et al.* (2008) to push the spur frequency to twice the reference frequency.

The reference spur magnitude also can be minimised by randomising the ripple on the tuning voltage (Liang *et al.* 2007). A switched capacitor is placed between the charge pump and loop filter as shown in Figure 6.3. The ϕ_2 switch, as shown in the figure, is

controlled by a pseudo-random-bit-string (PBRS), to randomise the switching events, so that the ripple voltages are randomly transfered to the loop filter.

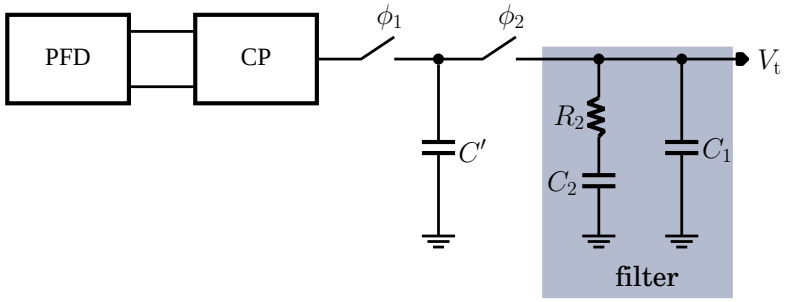


Figure 6.3. Randomised ripple on the tuning voltage. Here, the ϕ_2 is switching randomly so that the ripple voltages are randomly transfered to the VCO.

Another method to reduce reference spurs is by properly designing the delay in the PFD. The PFD delay is required to eliminate the dead zone. However, if the delay is larger than necessary, it increases the reference spur. Therefore, a calibrated PFD is introduced in Charles and Allstot (2006), where a feedback is used to maintain the minimum PFD delay to avoid dead zone.

6.2.4 Spur suppression technique comparisons

Table 6.1 presents performance of several spur suppression techniques, where f_{out} is the PLL output frequency, f_{ref} is reference frequency, and the loop bandwidth ratio is the percentage of loop bandwidth to the reference frequency ratio. It is unfair to compare the technique performances by its spur magnitude, because the magnitude is affected by the VCO gain and loop bandwidth (Elsayed *et al.* 2011). Each PLL uses different VCO gain and loop bandwidth. Smaller VCO gain helps to reduce the spur magnitude, meanwhile larger loop bandwidth is good for the spur performance.

6.3 Ratioed Current Charge Pump

Several spur suppression design techniques are reviewed in the previous section and one of them is achieved by charge pump current matching. Although I_{up} and I_{dn} are matched, reference spurs still exist due to other circuit non-idealities such as switching delay. According to the reference spur analysis in Section 4.3.2, a slightly larger I_{dn} than I_{up} helps to reduce reference spur magnitude. Therefore, the charge pump current

Table 6.1. Spur suppression technique comparison. Performance summary of several spur suppression techniques.

Reference	Technique	f_{out} (GHz)	Tuning range (GHz)	f_{ref} (MHz)	Loop bandwidth ratio (%)	Spur (dBc/Hz)
(Gao *et al.* 2010)	Sub-sampling phase detection	2.21	N/A	55.25	5%	-80
(Xiaozhou *et al.* 2009)	Current leakage compensation	1.21	0.43	1	10%	-52.1
(Liang *et al.* 2008)	Current mismatch compensation	5.22	0.36	10	2%	-69.25
(Choi *et al.* 2012)	Charge distribution	0.897	0.35	13	2.3%	-66
(Liang *et al.* 2007)	Charge distribution	1.8-3.4	1.6	8	1.5%	-68
(Lee and Lee 2006)	Distributed PFD/CP	4.8	N/A	1	N/A	-55
(Deng and Kiang 2009)	Low K_{vco}	5.15-5.35	0.2	4	5%	-40
(Glisic and Winkler 2006)	Low K_{vco}	55.14-58.7	3.56	218.75	2.06%	-64
(Kuo and Liu 2006)	Low K_{vco}	5.23-6.16	0.93	20	0.3%	-74

N/A : Not available

source is designed so that the I_{dn} slightly larger than I_{up}. Before implementing the design, an optimum I_{dn} to I_{up} ratio has to be determined.

When I_{dn} is larger than I_{up}, the I_{up} current switch ON longer than I_{dn}, so that the total charge transfer to the loop filter is zero. Figure 6.4 show timing diagrams for I_{up}, I_{dn}, and resulting in charge pump current, I_{cp}, when $I_{dn} > I_{up}$. The I_{up} is delayed by the switching delay of the UP switch, t_{inv}.

The optimum ripple amplitude in the VCO tuning voltage, ΔV, is achieved when $\Delta V_{top} = \Delta V_{bottom}$, and this can be attained if the I_{up} duration has $2t_{inv}$ longer than I_{dn}. Therefore, the difference duration between I_{up} and I_{dn} is given by

$$t_{diff} = 2t_{inv} \ . \tag{6.1}$$

Substituting this into Equation 4.19 results in

$$t_{PFD}\left(\frac{I_{dn}}{I_{up}} - 1\right) = 2t_{inv} \ ,$$
$$\frac{I_{dn}}{I_{up}} = \left(\frac{2t_{inv}}{t_{PFD}} + 1\right). \tag{6.2}$$

This equation gives the I_{dn} to I_{up} ratio in terms of switching delay (t_{inv}), and PFD delay (t_{PFD}). Parameters t_{inv} and t_{PFD} can be extracted from a transistor level simulation.

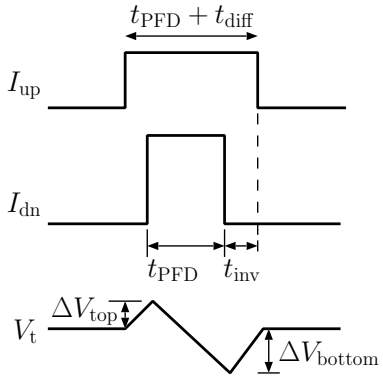


Figure 6.4. Timing diagram for charge pump current when $I_{dn} > I_{up}$. A minimum ripple voltage amplitude, ΔV_{top} and ΔV_{bottom}, is required to obtain a minimum reference spur.

The charge pump current is provided by a current mirror circuit as shown in Figure 6.5. The size of N_3 and N_5 is similar to N_1, while N_4 and N_6 is similar to N_2. Also, the size of P_3 and P_5 is similar to P_1. Initially, neglecting the channel length modulation effect, the charge pump current, I_{up} and I_{dn}, is equals to I_{ref} ($I_{up} = I_{dn} = I_{ref}$), and is given by

$$I_{ref} = \frac{1}{2}\mu_N C_{ox}\left(\frac{W}{L}\right)_{N_5}(V_{GS_{N_5}} - V_{th_{N_5}})^2 , \tag{6.3}$$

$$= \frac{1}{2}\mu_P C_{ox}\left(\frac{W}{L}\right)_{P_3}(|V_{GS_{P_3}}| - |V_{th_{P_3}}|)^2 , \tag{6.4}$$

$$I_{up} = \frac{1}{2}\mu_P C_{ox}\left(\frac{W}{L}\right)_{P_1}(|V_{GS_{P_1}}| - |V_{th_{P_1}}|)^2 , \tag{6.5}$$

$$I_{dn} = \frac{1}{2}\mu_N C_{ox}\left(\frac{W}{L}\right)_{N_1}(V_{GS_{N_1}} - V_{th_{N_1}})^2 , \tag{6.6}$$

where μ_P and μ_N are the charge carrier mobility for PMOS and NMOS, respectively, and C_{ox} is the gate oxide capacitance per unit area.

Ideally, $V_{GS_{N_1}} = V_{GS_{N_5}}$, yields (assuming N_2, N_4, and N_6 sizes are similar)

$$\frac{I_{dn}}{I_{ref}} = \frac{(W/L)_{N_1}}{(W/L)_{N_5}} . \tag{6.7}$$

As $I_{up} = I_{dn} = I_{ref}$, and for a minimum ripple amplitude in the VCO tuning voltage, the I_{dn} has to be $(2t_{inv}/t_{PFD}) + 1$ larger than I_{up}, therefore,

$$\frac{I_{dn}}{I_{up}} = \frac{(W/L)_{N_1}}{(W/L)_{N_3}} = \left(\frac{2t_{inv}}{t_{PFD}} + 1\right) . \tag{6.8}$$

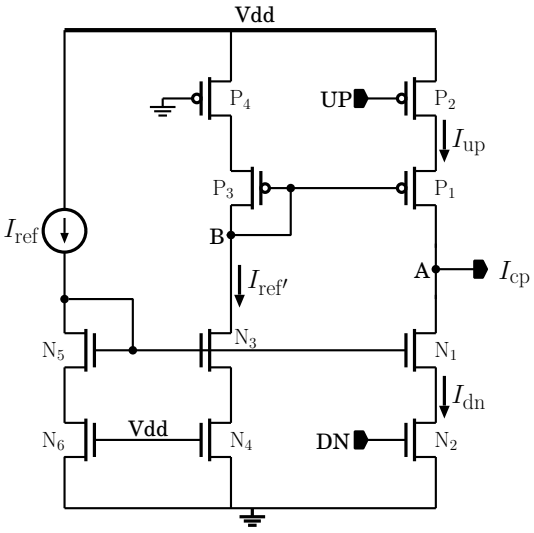


Figure 6.5. Charge pump circuit. Transistors N_1, N_3, N_5, P_1, and P_3 construct current sources for I_{up} and I_{dn} generation.

Considering the length of N_1 is similar to N_3 ($L_{N_1} = L_{N_3}$), therefore the width of N_1 is given by

$$W_{N_1} = \left(\frac{2t_{inv}}{t_{PFD}} + 1\right) W_{N_3} \,. \tag{6.9}$$

However, Equation 6.9 is only valid for an ideal case, and inappropriate to be used in the real implementation. In reality, the channel length modulation effect has to be considered, where I_{up} and I_{dn} changes according to the charge pump output voltage. Considering the channel modulation effect, I_{up} and I_{dn} is given by

$$I_{up} = \frac{1}{2}\mu_P C_{ox} \left(\frac{W}{L}\right)_{P_1} (|V_{GS_{P_1}}| - |V_{th_{P_1}}|)^2 (1 + \lambda_P |V_{DS_{P_1}}|) \,, \tag{6.10}$$

$$I_{dn} = \frac{1}{2}\mu_N C_{ox} \left(\frac{W}{L}\right)_{N_1} (V_{GS_{N_1}} - V_{th_{N_1}})^2 (1 + \lambda_N V_{DS_{N_1}}) \,, \tag{6.11}$$

where λ_P and λ_N are the channel length modulation effect parameters for PMOS and NMOS, respectively.

Referring to Figure 6.5, I_{up} to $I_{ref'}$ ratio is given by

$$\frac{I_{up}}{I_{ref'}} = \frac{\left(\frac{W}{L}\right)_{P_1} (|V_{GS_{P_1}}| - |V_{th_P}|)^2 (1 + \lambda_P |V_{DS_{P_1}}|)}{\left(\frac{W}{L}\right)_{P_3} (|V_{GS_{P_3}}| - |V_{th_P}|)^2 (1 + \lambda_P |V_{DS_{P_3}}|)} \,, \tag{6.12}$$

and

$$\frac{I_{\text{ref}'}}{I_{\text{ref}}} = \frac{\left(\frac{W}{L}\right)_{N_3}(V_{GS_{N_3}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_3}})}{\left(\frac{W}{L}\right)_{N_5}(V_{GS_{N_5}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_5}})}. \tag{6.13}$$

Therefore, I_{up} to I_{ref} ratio is given by

$$\frac{I_{\text{up}}}{I_{\text{ref}}} = \frac{\left(\frac{W}{L}\right)_{P_1}(|V_{GS_{P_1}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_1}}|)}{\left(\frac{W}{L}\right)_{P_3}(|V_{GS_{P_3}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_3}}|)} \frac{\left(\frac{W}{L}\right)_{N_3}(V_{GS_{N_3}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_3}})}{\left(\frac{W}{L}\right)_{N_5}(V_{GS_{N_5}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_5}})}. \tag{6.14}$$

Further, I_{dn} to I_{ref} ratio can be calculated by

$$\frac{I_{\text{dn}}}{I_{\text{ref}}} = \frac{\left(\frac{W}{L}\right)_{N_1}(V_{GS_{N_1}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_1}})}{\left(\frac{W}{L}\right)_{N_5}(V_{GS_{N_5}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_5}})}. \tag{6.15}$$

From Equations 6.14 and 6.15, I_{dn} to I_{up} ratio can be calculated by

$$\frac{I_{\text{dn}}}{I_{\text{up}}} = \frac{\left(\frac{W}{L}\right)_{P_3}(|V_{GS_{P_3}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_3}}|)}{\left(\frac{W}{L}\right)_{P_1}(|V_{GS_{P_1}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_1}}|)} \frac{\left(\frac{W}{L}\right)_{N_1}(V_{GS_{N_1}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_1}})}{\left(\frac{W}{L}\right)_{N_3}(V_{GS_{N_3}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_3}})}. \tag{6.16}$$

As the size of PMOS P_1 and P_3 are similar, hence $\left(\frac{W}{L}\right)_{P_1} = \left(\frac{W}{L}\right)_{P_3}$, and the length of NMOS N_1 is similar with N_3, therefore Equation 6.16 can be simplified to

$$\frac{I_{\text{dn}}}{I_{\text{up}}} = \frac{(|V_{GS_{P_3}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_3}}|)}{(|V_{GS_{P_1}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_1}}|)} \frac{W_{N_1}(V_{GS_{N_1}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_1}})}{W_{N_3}(V_{GS_{N_3}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_3}})}. \tag{6.17}$$

For a minimum ripple voltage magnitude, I_{dn} has to be larger than I_{up} by a ratio that is given by Equation 6.2. Substituting this equation into Equation 6.17, results in N_1 to N_3 width ratio as

$$\frac{W_{N_1}}{W_{N_3}} = \left(\frac{2t_{\text{inv}}}{t_{\text{PFD}}} + 1\right) \frac{(|V_{GS_{P_1}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_1}}|)}{(|V_{GS_{P_3}}| - |V_{th_P}|)^2(1+\lambda_P|V_{DS_{P_3}}|)} \frac{(V_{GS_{N_1}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_1}})}{(V_{GS_{N_3}} - V_{th_N})^2(1+\lambda_N V_{DS_{N_3}})}. \tag{6.18}$$

Due to the channel length modulation, $V_{DS_{P_1}}$, $V_{GS_{P_1}}$, $V_{DS_{N_1}}$, and $V_{GS_{N_1}}$ vary according to the charge pump output voltage, therefore the W_{N_1} to W_{N_3} ratio is also varies. For an optimum reference spur, only the VCO tuning voltage at the centre of VCO tuning frequency is considered. This is because, the centre frequency has the maximum VCO gain, resulting in a maximum reference spur, at that point. Therefore, for the W_{N_1} to W_{N_3} ratio calculation, we consider the charge pump output voltage similar to the VCO tuning voltage at the centre of tuning frequency.

The varying current ratio along the charge pump output voltage can be eliminated by implementing a current matching topology together with the ratioed current charge pump. The combination circuit is named ratioed with matched current charge pump, and further discussion on this circuit is available in the next section.

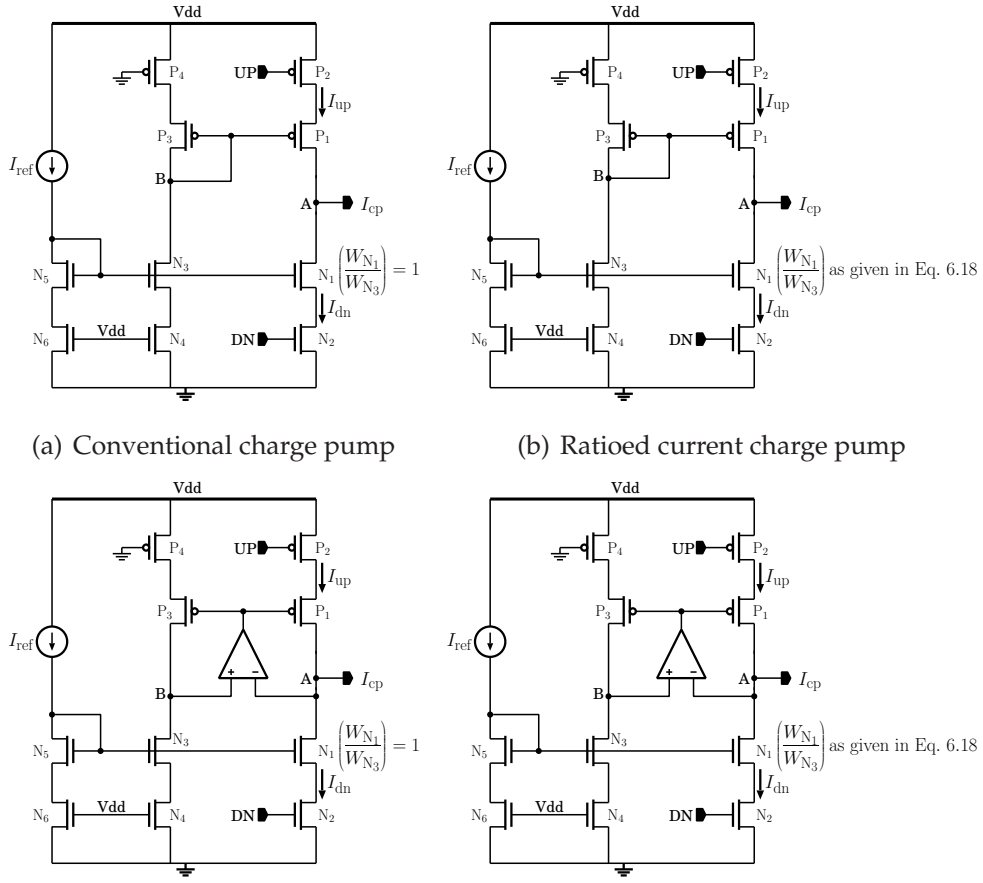
6.4 Reference Spur Suppression Performance Estimation

In order to estimate performance of the ratioed current charge pump spur suppression technique, PLLs with four different charge pump topologies are implemented, namely, conventional, ratioed current, matched current, and ratioed with matched current charge pump as shown in Figures 6.6(a), 6.6(b), 6.6(c), and 6.6(d), respectively.

The matched current charge pump circuit is taken from Lee and Hajimiri (2000). For the ratioed and ratioed with matched current charge pump circuit as shown in Figures 6.6(b) and 6.6(d), respectively, width of NMOS N_1 for both charge pumps are chosen so that the I_{dn} to I_{up} ratio is $(2t_{inv}/t_{PFD}) + 1$.

Figures 6.7(a), 6.7(b), 6.7(c), and 6.7(d) show the charge pump current, I_{up} and I_{dn}, for a conventional, ratioed current, matched current, and ratioed with matched current charge pump, respectively. For the conventional and ratioed current charge pumps, I_{dn} to I_{up} ratio varies with the charge pump output voltage. Meanwhile, for the matched current and ratioed with matched current charge pumps, the current ratio are constant in the middle of charge pump output voltage range.

Using the presented analysis in Chapter 4, reference spur magnitude for PLL with these four different charge pumps were obtained. Figure 6.8(a) shows the reference spur magnitude, while Figure 6.8(b) presents reference spur performance in percentage for the matched current, ratioed current, and ratioed with matched current charge pump PLL when compared to the conventional charge pump PLL.



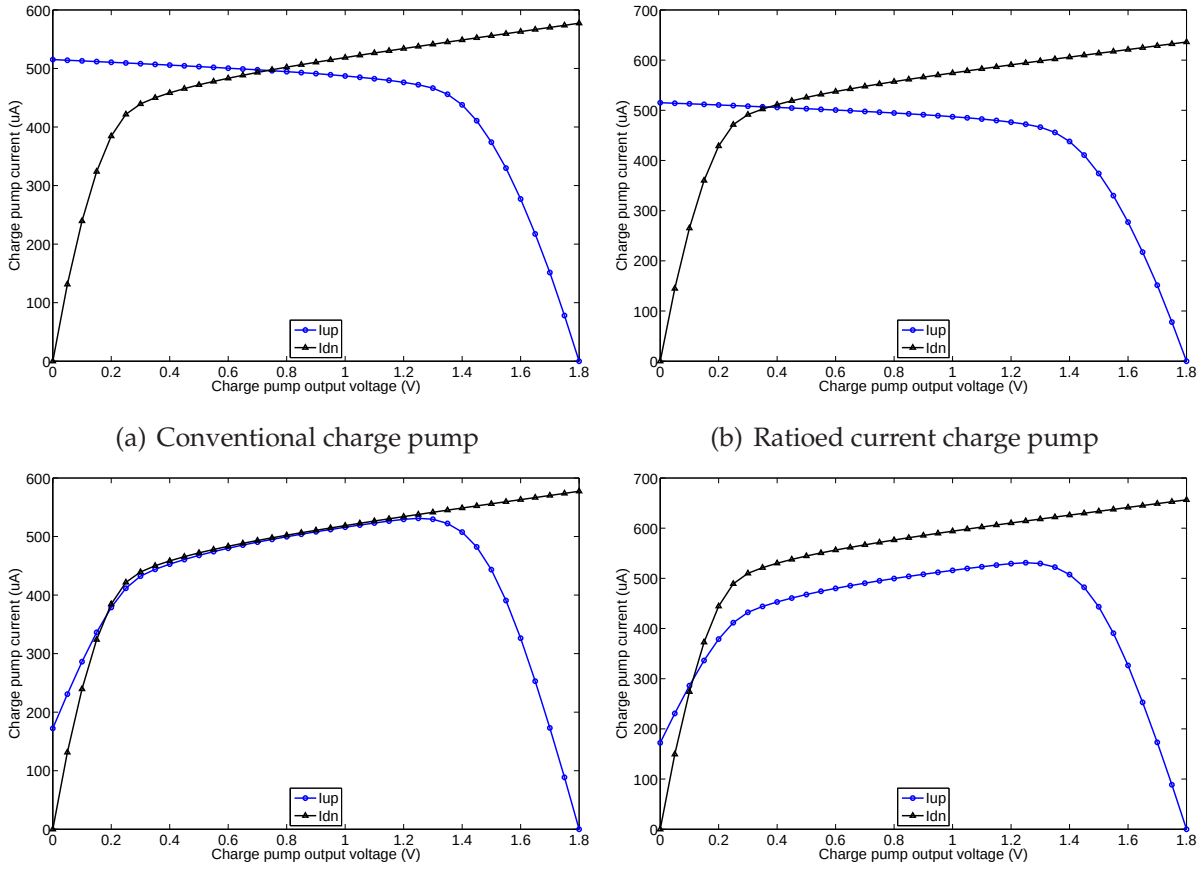
(a) Conventional charge pump (b) Ratioed current charge pump

(c) Matched current charge pump (d) Ratioed with matched current charge pump

Figure 6.6. Four different charge pump circuits. Reference spur magnitude of PLLs with these four different charge pumps are simulated to compare the performance.

The comparison graph shows that the charge pump with ratioed current improves reference spur performance. For the ratioed current charge pump topology, the spur performance decreases when the tuning voltage larger than 1 V. This is due to the channel length modulation, where I_{dn} to I_{up} ratio varies across the charge pump output voltage. Therefore, when ratioed I_{dn} to I_{up} too large and exceeds the optimum value, the spur magnitude starts to increase. This situation can be eliminated by using a current matching topology. As the I_{up} is designed to track the I_{dn}, the I_{dn} to I_{up} ratio is almost constant across the charge pump output voltage. In this case, the varying reference spur magnitude is caused by the varying VCO gain.

Reference spur improvement depends on I_{dn} to I_{up} ratio in the proposed charge pump when compared to the current ratio in the conventional charge pump. As shown in Figure 6.7(a), I_{dn} to I_{up} ratio in the conventional charge pump is increasing with the charge pump output voltage, nearly meet the optimum current ratio. Therefore, the



(a) Conventional charge pump

(b) Ratioed current charge pump

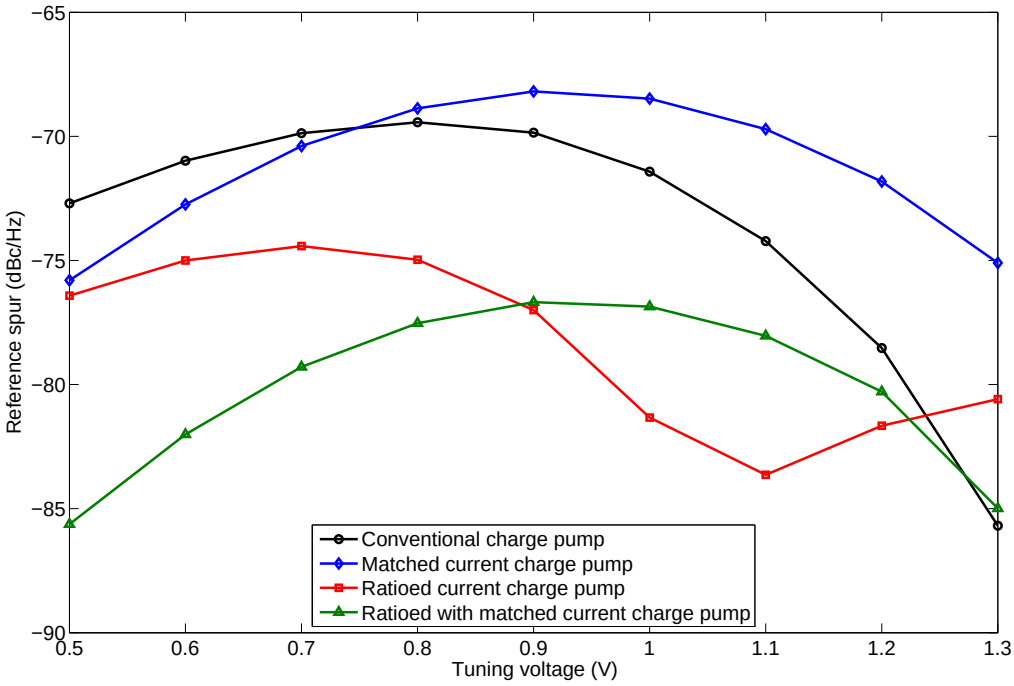
(c) Matched current charge pump

(d) Ratioed with matched current charge pump

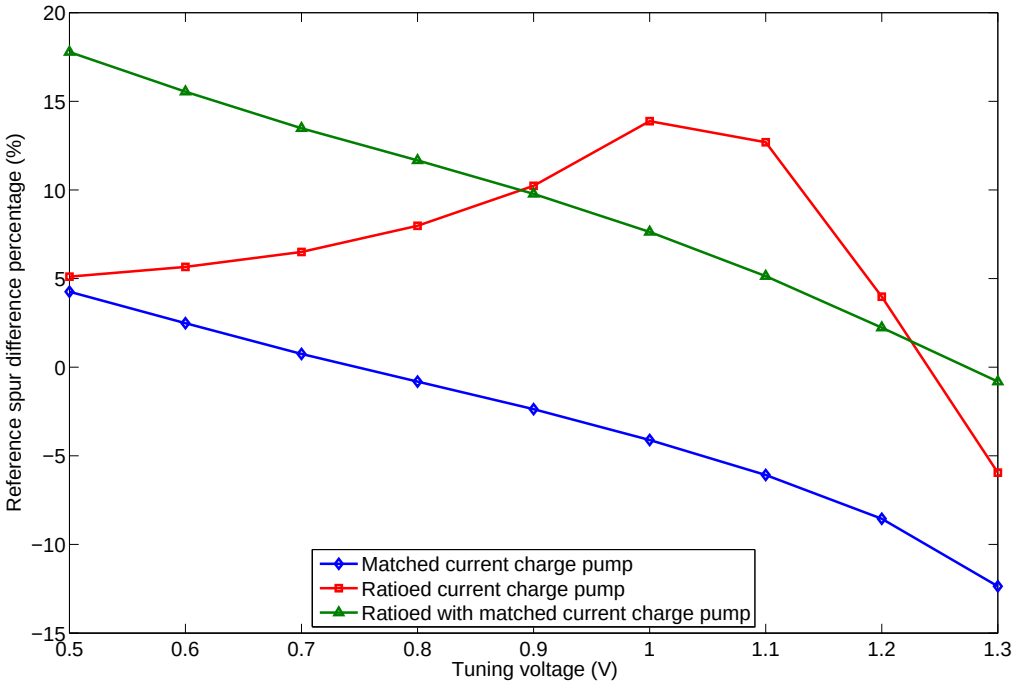
Figure 6.7. Charge pump current, I_{up} and I_{dn}, for four charge pump topologies. The charge pump currents are obtained from a dc analysis at the transistor level simulation. For the matched current and ratioed with matched current charge pump, the current ratio is constant in the middle of charge pump output voltage range, while the ratio increases with the tuning voltage for the conventional and ratioed current charge pump.

spur improvement is decreasing with the tuning voltage as shown in the matched current, and ratioed with matched current charge pump in Figure 6.8(b).

The matched current charge pump is expected to improve the reference spur performance, however the results in Figure 6.8 show an improvement is only achieved when the tuning voltage is less than 0.7 V. When the tuning voltage is higher than 0.7 V, the reference spur magnitude is higher than the conventional PLL. This is because when the charge pump current is matched, the ON period for I_{up} and I_{dn} is similar, but the I_{up} is delayed by a switching delay, hence produces a mismatch between these two signals. As shown in Figure 6.7(c), increasing the charge pump output voltage also



(a) Reference spur magnitude



(b) Reference spur difference percentage

Figure 6.8. Reference spur magnitude comparison. Reference spurs for the ratioed current, matched current, and ratioed with matched current charge pump PLL are compared to reference spur magnitude of a conventional charge pump. The reference spur magnitude is calculated using the mathematical analysis as presented in Chapter 4.

increases the I_{up} and I_{dn}, hence increasing the ripple voltage amplitude and reference spur.

Further, a VCO tuning voltage response for the ratioed current charge pump PLL is investigated. Using Simulink behavioural modelling as presented in Chapter 5, the VCO tuning voltage response for the ratioed current and ratioed with matched current charge pump PLL is obtained. These voltage responses are compared to a conventional charge pump PLL, and is presented in Figure 6.9. The ratioed current charge pump has a similar tuning voltage response as the conventional charge pump, while the ratioed with matched current charge pump has a slightly different response at the early stage. However, the proposed ratioed current and ratioed with matched current charge pump does not affect the PLL settling time.

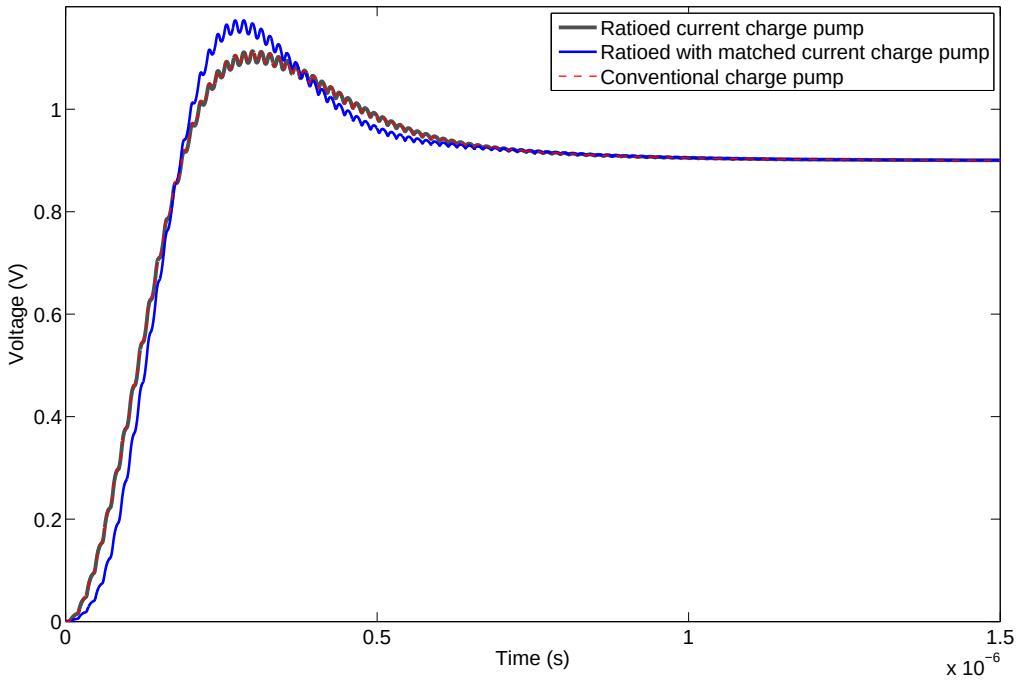


Figure 6.9. VCO tuning voltage comparison. A VCO tuning voltage for the proposed ratioed current and ratioed with matched current charge pump is compared with the tuning voltage of a conventional charge pump PLL. These VCO tuning voltages are obtained from a simulation at the behavioural level. The graph shows the ratioed current charge pump has a similar tuning voltage response as the conventional charge pump, while the ratioed with matched current charge pump has a slightly different response at the early stage.

6.5 Chapter Summary

In this chapter, a method to calculate an optimum charge pump current ratio to minimise ripples in the VCO tuning voltage, caused by the charge pump current mismatch and switching delay, is presented. The technique aims to set the charge pump current, I_{dn}, slightly larger than I_{up} at an optimum ratio to compensate the switching delay in the charge pump UP switch. This can be implemented by only resizing transistors in the charge pump current source circuit. Two charge pumps are designed to estimate the performance, where the first charge pump only implements the ratioed current, and the second charge pump combines the ratioed current and current matching topology. Using the mathematical analysis presented in Chapter 4, reference spur of the ratioed current and ratioed with matched current charge pump PLLs is calculated. These reference spur magnitudes are then compared to the spur magnitude from a conventional and matched current charge pump PLL, showing an improvement.

Having investigated the reference spur suppression technique in this chapter, it now raises the question of how much improvement the proposed technique can achieve when it is implemented at the transistor level, and therefore this is what we now discuss in the next chapter. A PLL design with the proposed ratioed current charge pump at a transistor level is presented in the next chapter.

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Chapter 7

PLL Circuit Design

EFFECTIVENESS of the ratioed current charge pump and ratioed current with matched current charge pump techniques are demonstrated through the design of PLL using a 180 nm SiGe BiCMOS technology provided by Jazz Semiconductor. Reference spur performance for the PLL with ratioed current and ratioed with matched current charge pumps are compared to a conventional charge pump PLL.

7.1 Introduction

In Chapter 6, the ratioed current charge pump is proposed to decrease ripple magnitude in the VCO tuning voltage, hence improves reference spur performance in the PLL output. Based on the reference spur mathematical analysis and behavioural modelling in Chapters 4 and 5, respectively, performance of the ratioed current charge pump is estimated. The results show that the proposed technique helps to reduce reference spur magnitude in the PLL output.

In this chapter, transistor level design of a PLL system that employs the ratioed current charge pump and ratioed with matched current charge pump circuits are presented. Reference spur magnitude of the proposed techniques are compared to a conventional charge pump PLL. Each of the PLL components is designed separately, before it is combined to form a PLL system. Frequency divider and prescaler test circuits have been fabricated, and the measurement results are presented in this chapter. Meanwhile, other circuit results are based on simulation using Spectre and SpectreRF in Cadence.

The PLL component design circuits are presented in Section 7.2. Then, these components are combined to form a PLL system. Phase noise and reference spur of the PLL are presented in Section 7.3. Finally, Section 7.4 summarises this chapter.

7.2 PLL Component Design

Two PLLs that employ the ratioed current charge pump and ratioed with matched current charge pump are designed to validate the spur suppression concept. The PLL frequency planning is as presented in Table 2.1. All the PLL component circuit designs are presented in the next sub-sections, and the PLL system integration and performance evaluation are presented in Section 7.3. This work only concentrates on the reference spur suppression technique, and all the circuit designs do not take low power consumption into consideration.

7.2.1 Charge pump

The ratioed current and ratioed with matched current charge pump circuits are shown in Figures 6.6(b) and 6.6(d). Here, NMOS N_1 in the both charge pump circuits is chosen

so that the ratio I_{dn} to I_{up} is optimum, where the optimum current ratio can be calculated based on Equation 6.2. The error amplifier in the ratioed with matched current charge pump is implemented using a rail-to-rail amplifier as shown in Figure 7.1.

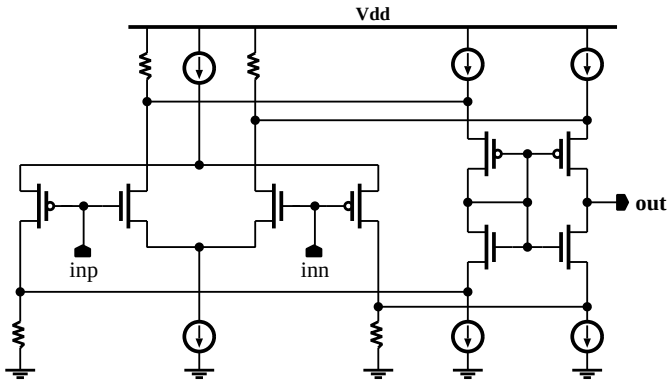


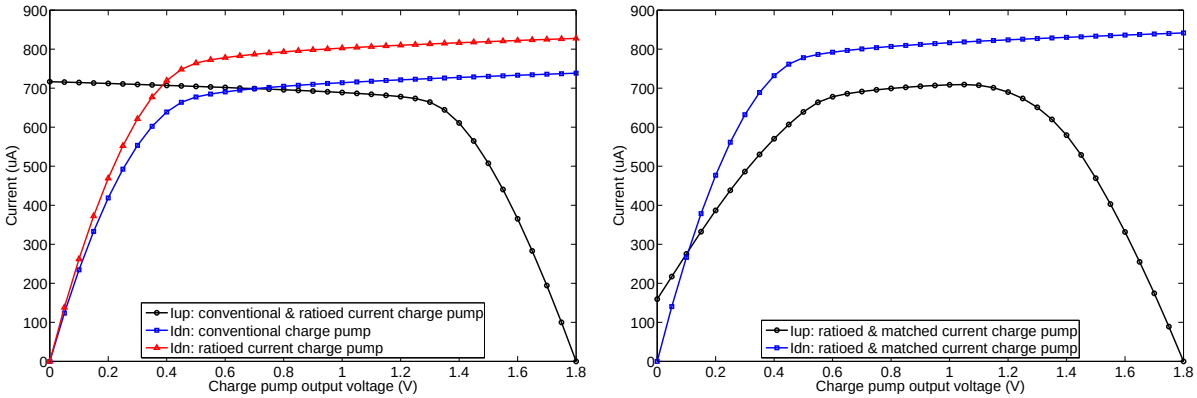
Figure 7.1. Rail-to-rail amplifier. This rail-to-rail amplifier is used as an error amplifier in the ratioed with matched current charge pump.

In addition, a conventional charge pump PLL is also implemented. Charge pump current, I_{up} and I_{dn}, for the three charge pump topologies are shown in Figures 7.2. Reference spur level for the PLL with ratioed current and ratioed with matched current charge pumps are compared to the conventional charge pump PLL in Section 7.3.2.

Figure 7.3 shows the ratioed current charge pump layout. The circuit occupies 50 μm $\times$ 50 μm silicon area.

Charge pump noise

Charge pump phase noise is simulated using PSS and Pnoise analysis in Cadence SpectreRF. For the simulation setup, the PFD and charge pump is connected together. A reference signal is connected to the both PFD inputs, and noise is taken from the charge pump output current. Figure 7.4 shows the open loop noise for the conventional, ratioed current, and ratioed with matched current charge pumps, and the closed-loop noise for the ratioed with matched current charge pump. The flicker noise ($1/f$ noise) for the three charge pumps are very close in value, but white noise for the ratioed with matched current charge pump is higher when compared to the other two charge pumps. The extra amplifier in this type of charge pump contributes to the higher noise.



(a) Conventional and ratioed current charge pumps

(b) Ratioed with matched current charge pump

Figure 7.2. Charge pump current, I_{up} and I_{dn}, for three different charge pump topologies. Charge pump currents are obtained from a dc analysis at the transistor level simulation. Here, I_{up} for the conventional and ratioed current charge pumps are similar, while the I_{dn} for the ratioed current charge pump is $(2t_{\mathrm{inv}}/t_{\mathrm{PFD}})+1$ larger than I_{dn} for the conventional charge pump.

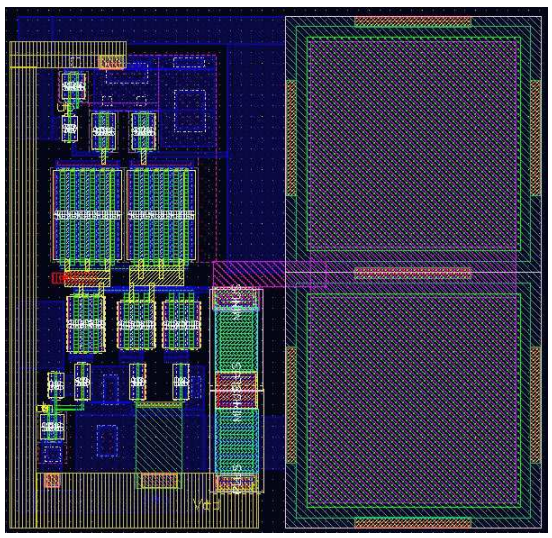


Figure 7.3. Ratioed current charge pump layout. The circuit occupies 50 μm $\times$ 50 μm silicon area.

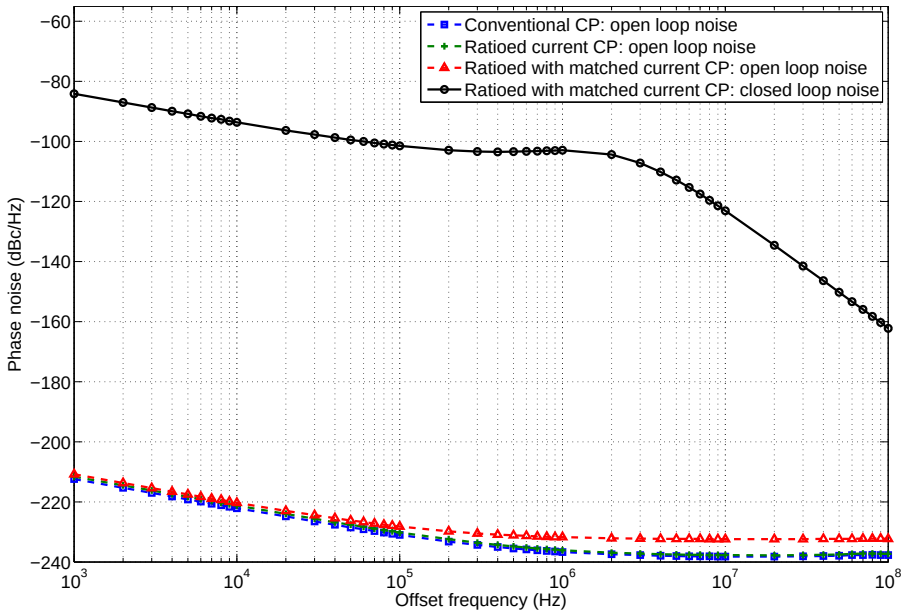


Figure 7.4. Open and closed-loop charge pump current noise for the conventional, ratioed current, and ratioed with matched current charge pumps. The charge pump open loop noise is obtained from a PSS and Pnoise analysis in Cadence Spectre. Flicker noise for these three charge pumps are not much different, but the white noise for ratioed with matched current charge pump is higher when compared to the other two charge pumps, due to the extra amplifier circuit.

7.2.2 VCO

An LC cross-coupled differential VCO as shown in Figure 7.5 is designed. A large accumulation mode MOS varactors are used to cover a wide tuning range from 15.86 GHz to 18.38 GHz. According to the frequency planning in Table 2.1, the PLL output frequency range is from 16.286 GHz to 18.286 GHz. The VCO is designed so that these PLL frequencies are located along the charge pump current (I_{up} and I_{dn}) linear region, where in this design the tuning voltage, V_{tune}, is in between 0.3 V to 1.3 V. Using a large varactor to cover the wide tuning range within a small tuning voltage range results in a large VCO gain, where the maximum value in this design is about 3 GHz/V.

As shown in Figure 7.5, a bias voltage, V_b, is connected to the varactors through inductors, L_2 and L_3. The bias voltage is used to shift the linear region of the VCO gain to be located at the centre of the tuning voltage. Capacitors, C_1 and C_2, are used to block the DC voltage components of the VCO output signal from the varactor. These capacitors

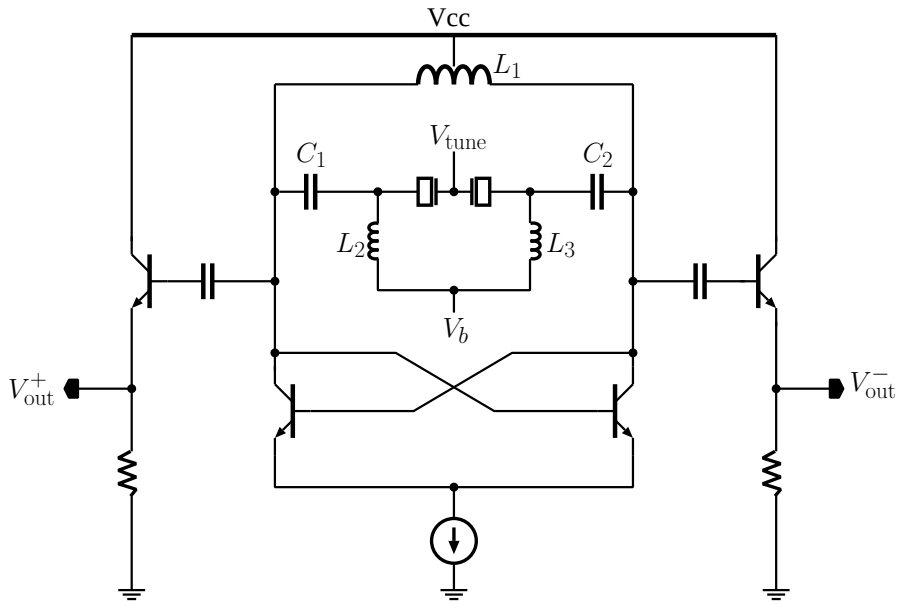


Figure 7.5. LC cross-coupled differential VCO schematic. The VCO outputs are connected to BJT voltage followers, which are used as a buffer. A bias voltage, V_b, is connected to the varactors through inductors, L_2 and L_3, to ensure the linear region of the VCO gain is located at the centre of the tuning voltage.

are connected in series with the varactors, hence affect the tank's capacitance. Considering these capacitance (C_1 and C_2), the total capacitance, C_{total}, in the LC tank is given by

$$C_{\text{total}} = \frac{C_{\text{var}} C_1}{C_{\text{var}} + C_1}\,, \tag{7.1}$$

where C_{var} is the varactor capacitance, and C_1 & C_2 are set to be equal. Choosing C_1 much larger than C_{var} results in $C_{\text{total}} \approx C_{\text{var}}$. Therefore, a large C_1 & C_2 are important to minimise their capacitance effect to the tank capacitance.

The VCO layout is shown in Figure 7.6. The circuit occupies 460 μm $\times$ 400 μm area including the buffers. A post-layout simulation with resistor and coupling capacitor extraction is performed in order to accurately simulates the output frequency and phase noise. Figure 7.7 shows the VCO output frequency as a function of its tuning voltage.

VCO noise

The VCO phase noise is simulated using PSS and Pnoise analysis in Cadence SpectreRF. Along the tuning range, the worse VCO phase noise is -101.1 dBc/Hz at 1 MHz offset. Figure 7.8 shows the open loop and closed-loop VCO phase noise.

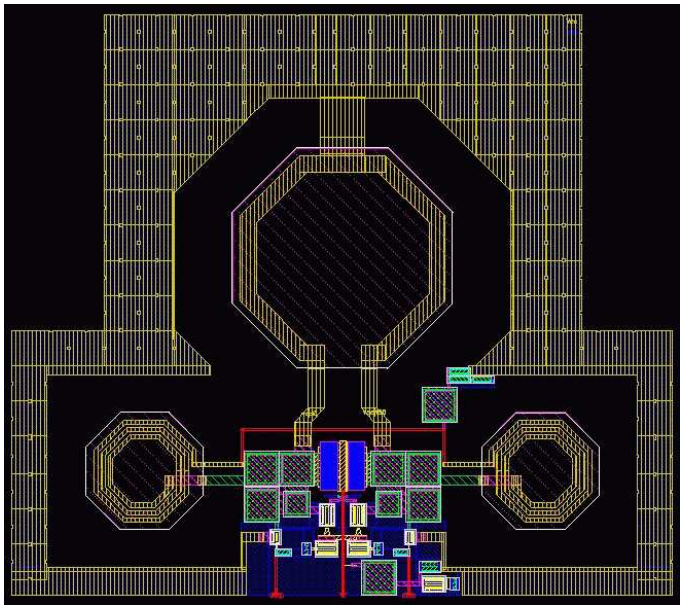


Figure 7.6. VCO layout. The circuit occupies $460\ \mu\mathrm{m} \times 400\ \mu\mathrm{m}$ area including buffers.

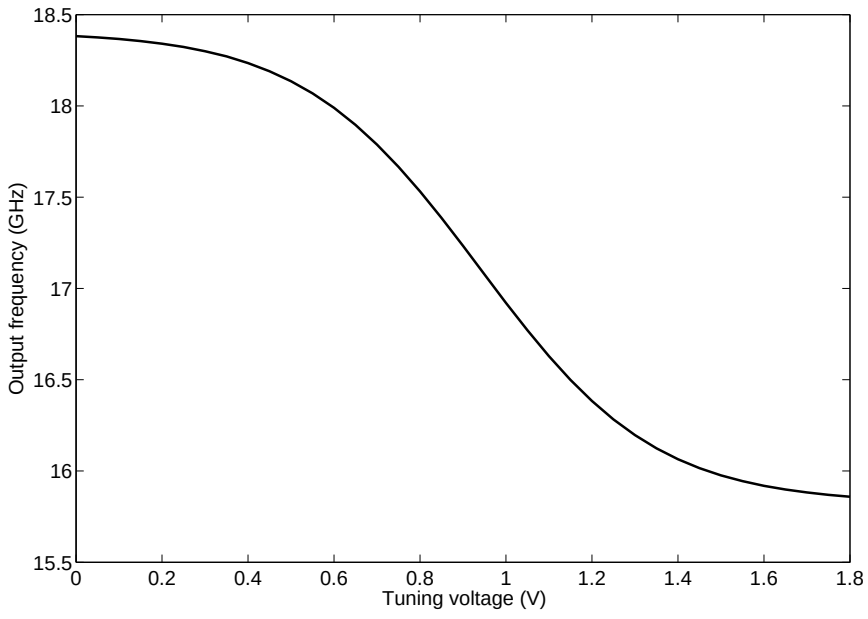


Figure 7.7. VCO output frequency as a function of tuning voltage. The VCO output frequency is obtained from a post-layout simulation using PSS analysis in Cadence Spectre. The maximum voltage gain (the graph slope) is about 3 GHz/V located at the centre of tuning voltage.

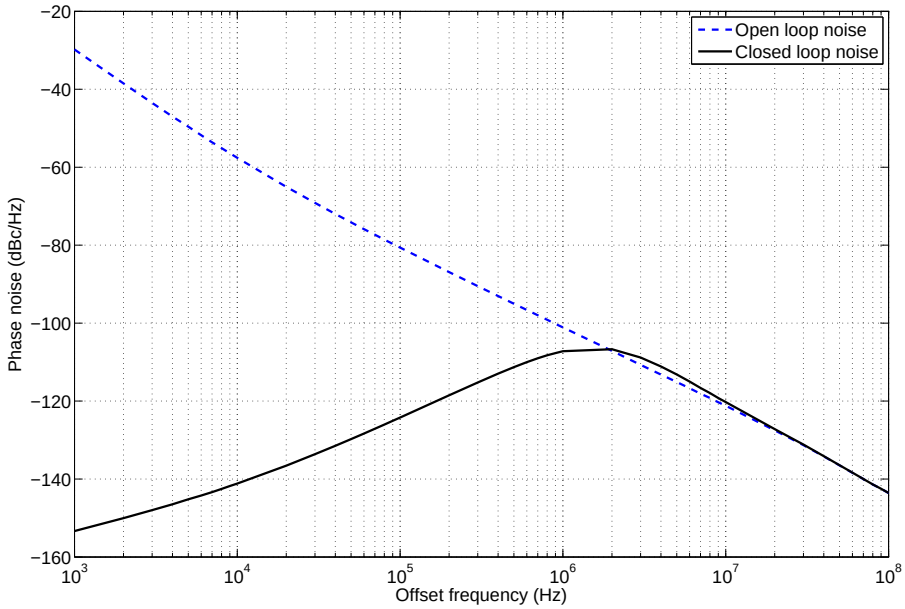


Figure 7.8. The VCO open loop and closed-loop noise. The VCO open loop noise is obtained from a post-layout simulation using PSS and Pnoise analysis in Cadence SpectreRF. Meanwhile, the VCO closed-loop noise is calculated using Equation 3.14. The VCO noise is filtered at low offset frequencies, but is passed to the PLL output when the offset frequency is outside the loop bandwidth.

Normally VCO performance is compared with other designs by using Figure-Of-Merit (FOM) (Liu and Lin 2007, Jang and Lee 2007, Luo *et al.* 2005), which is defined by

$$\mathrm{FOM_{vco}} = \mathcal{L}(f_{\mathrm{offset}}) - 20\log\left(\frac{f_o}{f_{\mathrm{offset}}}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right) , \tag{7.2}$$

where $\mathcal{L}(f_{\mathrm{offset}})$ is the single sideband phase noise measured at frequency offset, f_{offset}, from the output frequency, f_o, and P_{DC} is the DC power consumption in mW. This FOM ignores the VCO frequency tuning range factor. Another FOM that include the tuning range (Kim *et al.* 2003) is given by

$$\mathrm{FOM_{t_{vco}}} = \mathcal{L}(f_{\mathrm{offset}}) - 20\log\left(\frac{f_o}{f_{\mathrm{offset}}}\right) - 20\log\left(\frac{\mathrm{FTR}}{10}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right) , \tag{7.3}$$

where FTR is the frequency tuning range percentage, which is given by

$$\mathrm{FTR} = \frac{(f_{o_{\max}} - f_{o_{\min}})}{f_o} 100\ [\%] . \tag{7.4}$$

Based on both FOMs, the VCO in this work is compared to other published designs as presented in Table 7.1. Lower FOM indicates a better performance, however FOM_{vco} and $FOM_{t_{vco}}$ in this work is higher compared to other designs. This is because designs in Nagarajan *et al.* (2011), and Floyd (2008) employ a switched capacitor VCO to lower the VCO gain, hence improves phase noise and tuning range, while VCOs presented in Li *et al.* (2008), and Kuo *et al.* (2009) use a transformer based topology to obtain an improved phase noise and a larger tuning range. As this work gives the priority for reference spur issues, a conventional VCO with a large varactor to achieve a wide tuning range, is used. A large VCO gain from the large varactor limits the phase noise performance.

Table 7.1. VCO performance comparison.

Reference	Centre freq. (GHz)	Phase noise (dBc/Hz)	Tuning range	Power (mW)	Process	FOM_{vco}	$FOM_{t_{vco}}$
This work#	17.1	-101.1@1MHz	14.7%	10	0.18μm SiGe BiCMOS	-175.8	-179.2
(Nagarajan *et al.* 2011)*	25.1	-100.7@1MHz	17%	12.6	0.18μm SiGe BiCMOS	-180.3	-184.9
(Floyd 2008)*	17.4	-125@10MHz	16.5%	23.1	0.13μm SiGe BiCMOS	-176.8	-181.2
(Li *et al.* 2008)*	21.4	-105.9@1MHz	3%	9.6	0.18μm CMOS	-182.8	-171.6
(Kuo *et al.* 2009)*	24.5	-95@1MHz	15.5%	1.7	0.18μm CMOS	-179.8	-183.6

Simulation result

* Measurement result

7.2.3 Frequency divider

A master slave frequency divider as shown in Figure 2.18 is designed. For a high operating frequency, the divider is implemented using an emitter coupled logic (ECL) D flip-flop as shown in Figure 7.9. The divider output is buffered before being used to drive other circuits. The output buffer consists of a pair of emitter followers and a differential amplifier.

The master-slave divider consists of two D flip-flops. Output of the first D flip-flop must be able to drive the input of second D flip-flop. Normally, emitter follower circuits are added in between the D flip-flops to provide a voltage level shifting to drive the next stage (Wang *et al.* 2006, Rylyakov and Zwick 2003). The divider circuit in this thesis employs a direct coupling structure, where the circuit is designed so that the emitter follower in between the D flip-flops can be eliminated. This is achieved by properly choosing resistors and the amount of current so that the first D flip-flop output level is able to drive the second flip-flop at an appropriate level.

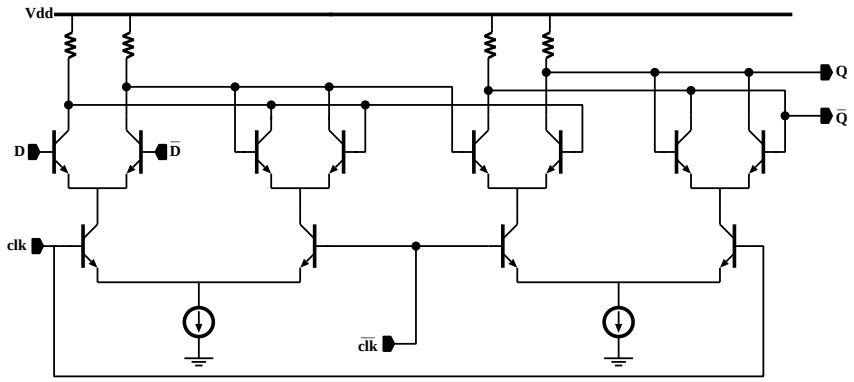


Figure 7.9. Master-slave frequency divider schematic. The divider consists of two D flip-flops, which is implemented in an ECL topology. Output of the first D flip-flop is designed to drive input of the second D flip-flop without a voltage level shifter.

Figure 7.10 shows two cascaded master-slave divider layout results in a divide-by-4 circuit, and Figure 7.11 shows a divide-by-2 master-slave frequency divider micrograph. The layout is designed to be symmetrical to ensure the same delay for the differential signal. Tracks from input to output are designed to be as short as possible to reduce the propagation delay. The circuit occupies 0.6 mm $\times$ 0.6 mm silicon area including the pads.

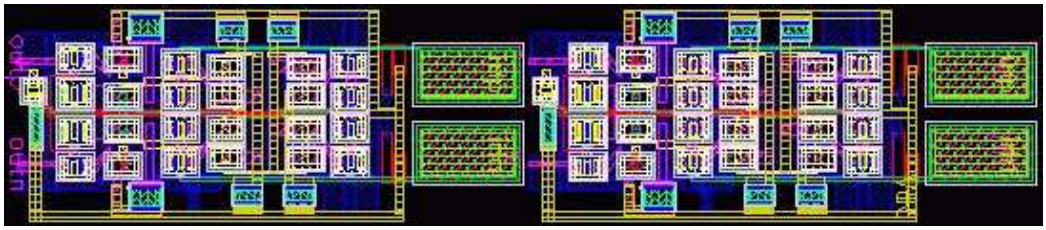


Figure 7.10. Master-slave frequency divider layout. The layout shows two cascaded master-slave frequency dividers, resulting in a divide-by-four circuit. The circuit occupies 62 μm $\times$ 296 μm area.

The master-slave divider including the buffer consumes 54 mW from a 1.8 V supply voltage. The maximum operation frequency is 30 GHz. Figure 7.12 shows a measurement result of the master slave divider at 24 GHz input frequency.

7.2.4 Prescaler

The dual modulus prescaler consists of a dual modulus divider (divide-by-7 and 8), two counters (named as P and S counters), and an ECL-to-CMOS converter as shown

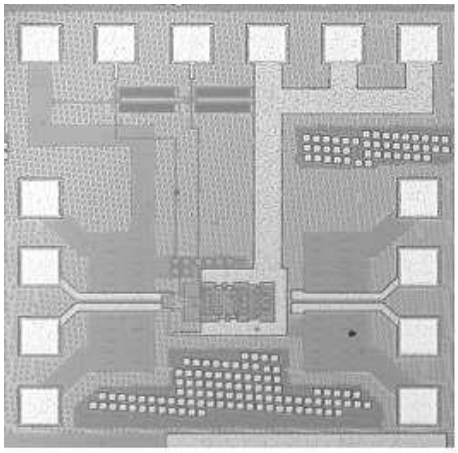


Figure 7.11. Master-slave frequency divider micrograph. A divide-by-two circuit, which is implemented in a master-slave topology.

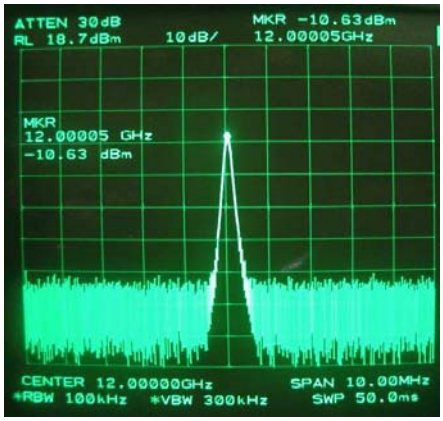


Figure 7.12. Master-slave frequency divider measurement result. This spectrum shows a measurement result of a divide-by-two master-slave divider, where the input frequency is at 24 GHz and the output frequency is 12 GHz.

in Figure 7.13. The prescaler total division ratio, M, can be calculated by Equation 2.8. Each circuit block is discussed in the following sub-sections.

Dual modulus divider

The dual-modulus divider consists of two stages, where the first stage is divide-by-3 and 4, and the second stage is divide-by-2 as shown in Figure 7.14 (Lee *et al.* 1997).

The dual-modulus divider is implemented by three D flip-flops, two OR gates, and one NAND gate. These circuits are implemented using an emitter-coupled logic (ECL) circuit topology, as it can handle a high operating frequency but at the cost of higher power consumption. Figure 7.15(a) and 7.15(b) show the ECL topology for OR and

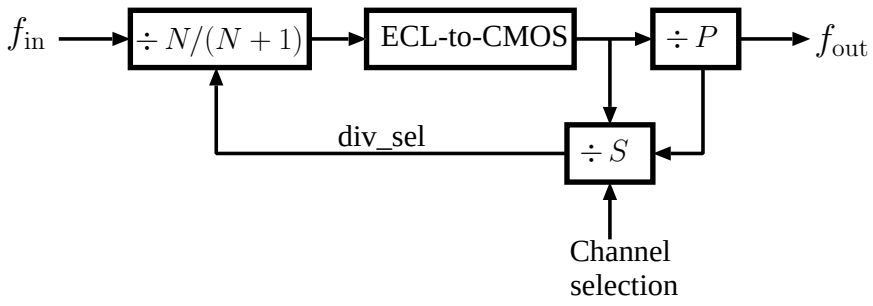


Figure 7.13. Prescaler. Consist of a dual-modulus divider, an ECL-to-CMOS converter, and two counters, namely, P and S. Channel selection is connected to a digital signal that represent the channel number. This digital signal determine the prescaler dividing ratio.

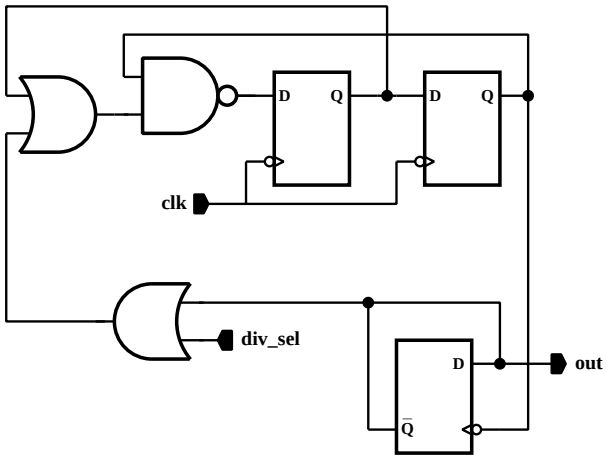


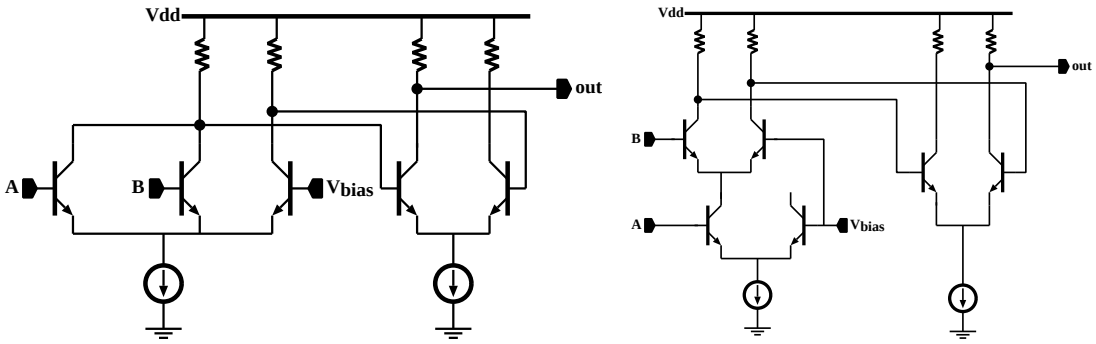
Figure 7.14. Dual modulus divider. The top D flip-flops construct a divide-by-three or four circuit, and the bottom D flip-flop construct a divide-by-two circuit. The `div_sel` signal determines the division ratio, either seven or eight.

NAND gates, respectively. The ECL D flip-flop circuit is similar to the D flip-flop as used in master slave frequency divider as shown in Figure 7.9

The dual-modulus divider has two division ratios, which is seven and eight. The division ratio is controlled by an input signal named `div_sel`, which is provided by the S counter. If `div_sel` is HIGH, the division ratio is 8, while if `div_sel` is LOW, the division ratio is seven.

P counter

The P counter is a 3-bit synchronous binary down counter. The counter is built from full adders and D flip-flops as shown in Figure 7.16.



(a) An ECL OR gate (b) An ECL AND gate

Figure 7.15. OR and AND gates implementation in an ECL topology. The ECL topology enables the circuit to operate at higher operating frequency compared to conventional digital circuit implementation. However, ECL topology increases the power consumption.

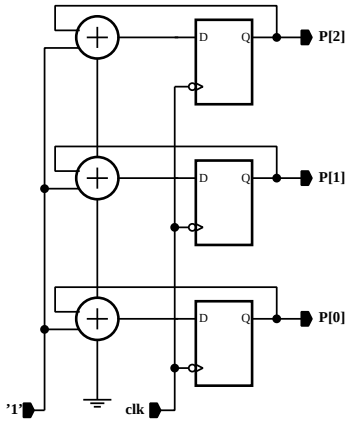


Figure 7.16. P counter. The P Counter is a 3-bit synchronous binary down counter.

The P counter is clocked by the dual-modulus divider output. The Most Significant Bit (MSB) of the counter output is taken as the prescaler output. This counter also provides a signal named `load` that coupled into S counter. The `load` signal is only HIGH when all the P counter output are zeros.

S counter

The S counter is also using a 3-bit synchronous binary down counter. In addition, a multiplexer is included in between full adders and D flip-flops as shown in Figure 7.17. The multiplexer determines the S counter output, either from the adder or from the digital input signals, which is also the channel number. The multiplexer is controlled by a signal named `load`.

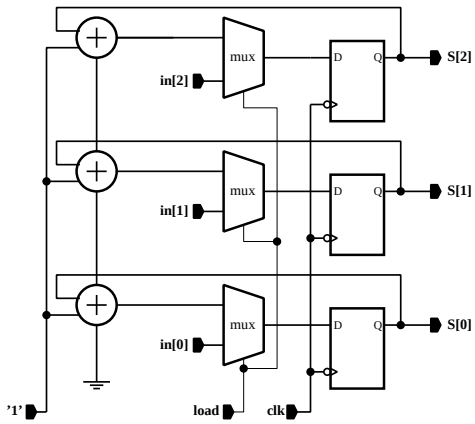


Figure 7.17. S counter. The S Counter is a 3-bit synchronous binary down counter with an extra signal named `load` to control multiplexers.

The clock signal is provided by the dual-modulus divider output, and the `load` signal is from the P counter. The 3 bits digital input signal is user-defined, and it determines the prescaler division ratio. The prescaler can handles eight different digital inputs from 000 to 111. This will give eight different division ratios, which are 57, 58, 59, 60, 61, 62, 63, and 64. The S counter has an output signal named `div_sel`, which is fed back to the dual-modulus divider.

When the `load` signal is HIGH, the S counter loads the digital input to the output, and starts count down from that binary input value. The S counter outputs maintain zeros until the next `load` signal is HIGH. When all the S counter output are zeros, `div_sel` signal is LOW.

ECL-to-CMOS

The P and S counters are clocked by the dual-modulus divider output. As the divider uses an ECL topology, the output voltage is a sinusoidal voltage with amplitude of a few hundreds mV. The counters are implemented in digital, thus digital signals are required. Therefore, an ECL-to-CMOS circuit is used to match the logic level between the dual-modulus divider and the counters. Figure 7.18 shows the ECL-to-CMOS circuit.

The ECL-to-CMOS circuit is implemented using a differential amplifier with an active load, PMOS. The active load is used to provide a high output conductance, r_o, hence a higher gain can be achieved. Two stages of inverter is connected to the differential amplifier as buffers to ensure a rail-to-rail voltage swing can be obtained.

Figure 7.19 shows the prescaler layout. The circuit occupies 340 μm $\times$ 100 μm silicon area.

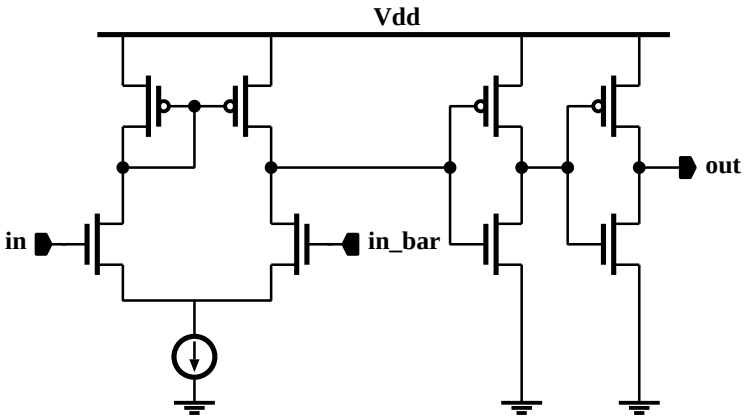


Figure 7.18. ECL-to-CMOS converter. This circuit is required to convert a sinusoidal signal from the dual-modulus divider to a digital signal for P and S counters.

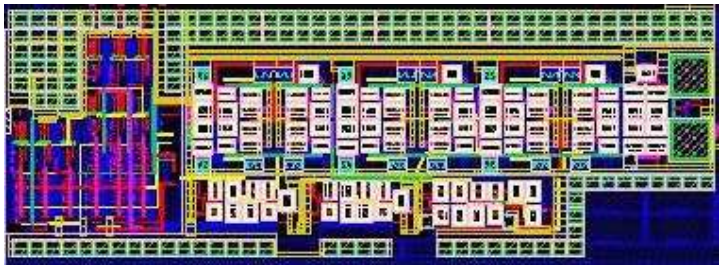


Figure 7.19. Prescaler layout. The circuit occupies 340 μm $\times$ 100 μm silicon area.

Prescaler results

Figure 7.20 shows the dual modulus divider simulation results when the digital input is set to 001, with input frequency at 5 GHz. The input signal is AC coupled and DC biased before it goes to the dual-modulus divider. Note that the output swing is not a full digital swing and the ECL-to-CMOS converter is used to ensure a rail-to-rail voltage swing.

Figure 7.21 shows the prescaler simulation results for four selected digital inputs, namely, 000, 011, 101, and 111, which are also represent four channels. These four digital inputs provide four different division ratios, which is 57, 60, 62, and 64, respectively. The operating frequency is 5 GHz.

Figure 7.22 shows the prescaler measurement results for six different division ratios, which is 59, 60, 61, 62, 63, and 64. The operating frequency is at 4.4 GHz. The limitation of the operating frequency comes from the delay $\texttt{div}_{\texttt{sel}}$ signal. This signal is generated by S counter, and the counter is clocked by the dual modulus divider output. As the counter is a digital circuit, while the dual modulus divider is an ECL

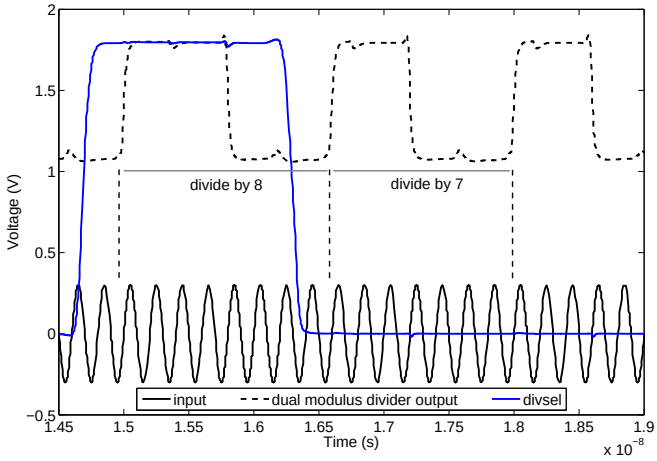


Figure 7.20. Dual modulus divider simulation result. When the `div_sel` signal is HIGH, the input signal is divided by 8. The division ratio is changed to 7 when the `div_sel` signal is LOW. The output swing is not a full digital swing, hence an ECL-to-CMOS is used to convert this signal to a rail-to-rail voltage swing.

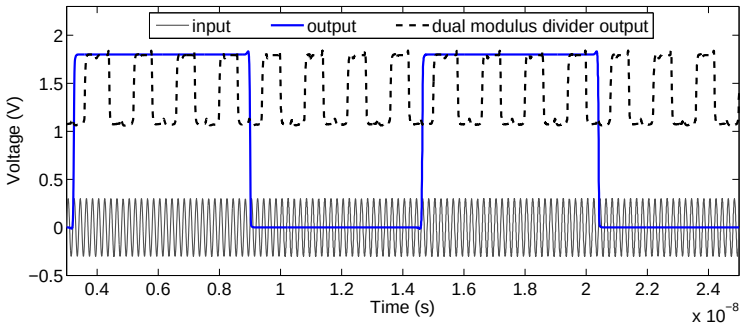
circuit, hence ECL-to-CMOS is used to convert the dual modulus divider output into a digital logic signal. Unfortunately, the ECL-to-CMOS delays the clock signal for the S counter, hence delays the $\texttt{div}_{\texttt{sel}}$ signal. Therefore, the delay is improved by resizing the transistors in ECL-to-CMOS and $\texttt{div}_{\texttt{sel}}$ signal generation circuits. According to simulation results, the improved prescaler circuit can operates at higher than 5 GHz input frequency.

Prescaler and divider noise

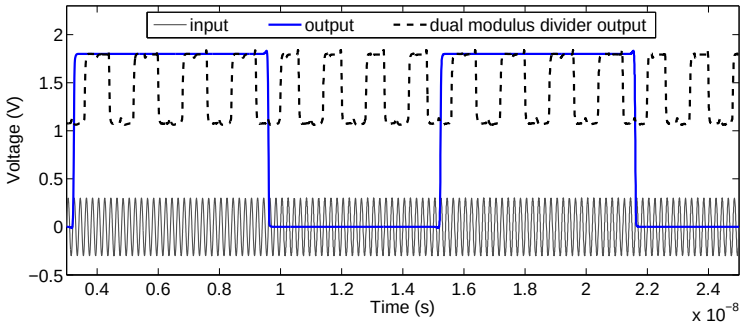
Frequency divider and prescaler phase noise are simulated together using PSS and Pnoise analysis and the results are shown in Figure 7.23. The division ratio, N, increases the phase noise by $20\log(N)$. The noise is filtered out when the offset frequency is outside the loop bandwidth.

7.2.5 PFD

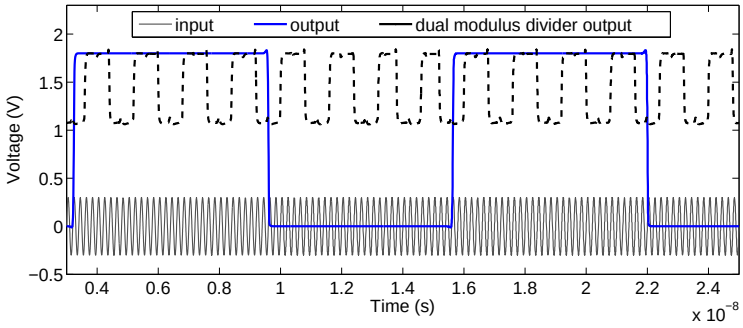
A PFD circuit as shown in Figure 7.24 consist of two D flip-flops, a NAND gate, and a few inverters. Three inverters after the NAND gate is for a PFD delay to eliminate the dead zone, while inverters at the PFD inputs and outputs are functioned as buffers. Each D flip-flops is constructed by four OR gates as shown in Figure 7.25. The PFD layout occupies 30 μm $\times$ 30 μm die area as shown in Figure 7.26.



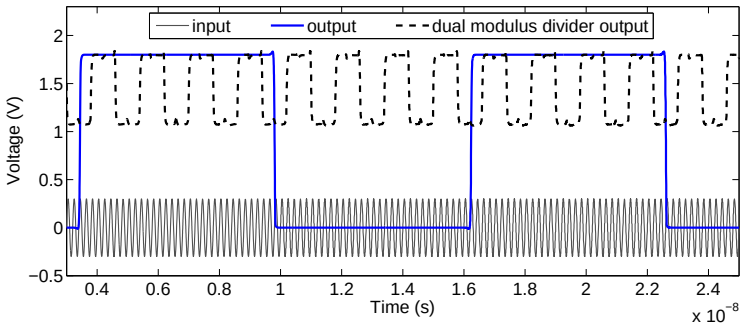
(a) Channel 0, digital input = 000, division ratio = 57



(b) Channel 3, digital input = 011, division ratio = 60

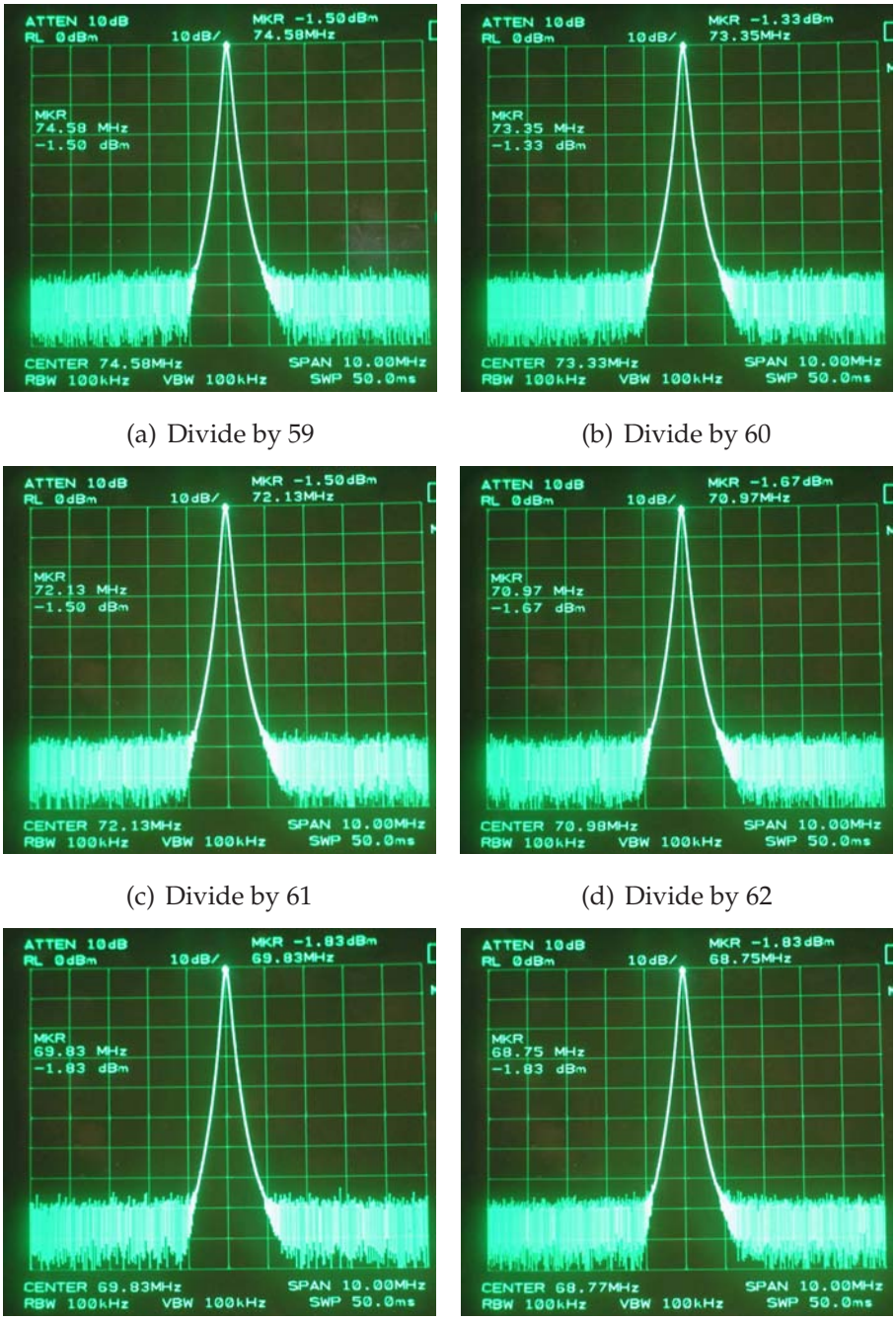


(c) Channel 5, digital input = 101, division ratio = 62



(d) Channel 7, digital input = 111, division ratio = 64

Figure 7.21. Prescaler simulation results for four different digital inputs. The input frequency is at 5 GHz. The prescaler output is taken from the MSB of P counter output.



(a) Divide by 59 (b) Divide by 60

(c) Divide by 61 (d) Divide by 62

(e) Divide by 63 (f) Divide by 64

Figure 7.22. Prescaler measurement results. The spectrum show measurement results for a prescaler with six different dividing ratio, which is 59, 60, 61, 62, 63, and 64. The input frequency is at 4.4 GHz.

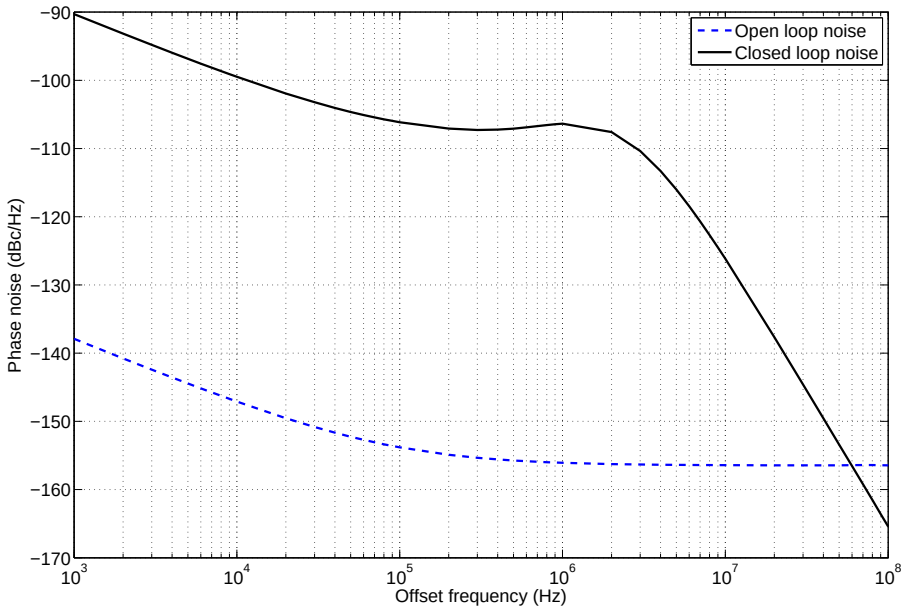


Figure 7.23. Frequency divider and prescaler phase noise. The divider and prescaler open loop noise is obtained from a simulation using PSS and Pnoise analysis in Cadence SpectreRF. Meanwhile, the closed-loop noise is calculated using Equation 3.15. The division ratio, N, increases the prescaler and divider noise by $20\log(N)$. The noise is filtered out when the offset frequency is outside the loop bandwidth.

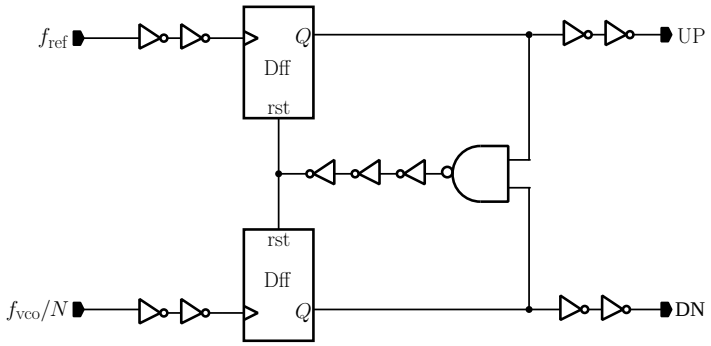


Figure 7.24. PFD circuit. The PFD is constructed by two D flip-flops and a NAND gate together with three inverters as the PFD delay. Inverters at the D flip-flop inputs and outputs are functioned as buffers.

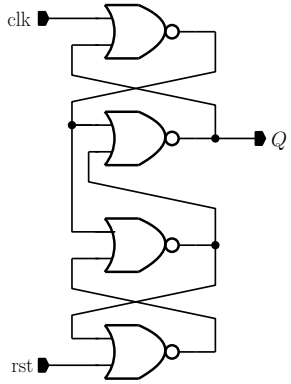


Figure 7.25. D flip-flop circuit. The D flip-flops in the PFD is constructed by four OR gates.

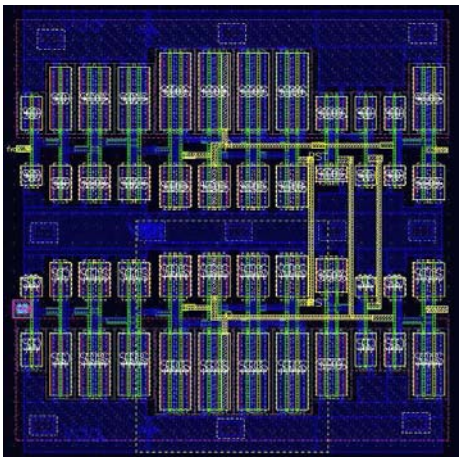


Figure 7.26. PFD layout. The circuit consumes 30 μm $\times$ 30 μm die area.

7.2.6 Loop filter

Resistors and capacitors in the loop filter are chosen according to loop bandwidth and phase margin of the PLL. The resistors and capacitors value were calculated based on Thompson and Brennan (2005). The simplest loop filter is a second order low pass filter with a transfer function is given by

$$F_2(s) = \frac{1}{s\tau_0}\frac{(1+s\tau_1)}{(1+s\tau_2)}, \tag{7.5}$$

where τ_0 is the low frequency filter gain, and τ_1 and τ_2 are the time constants. Equating this equation with a second order low pass filter transfer function as given in Equation 4.25, yields

$$\tau_0 = C_1 + C_2 \,, \tag{7.6}$$

$$\tau_1 = R_2 C_2 \,, \tag{7.7}$$

$$\tau_2 = \frac{R_2 C_1 C_2}{C_1 + C_2} \,, = \frac{\tau_1 C_1}{\tau_0} \,. \tag{7.8}$$

Relationship between the PLL phase margin and the loop filter can be derived from an open loop transfer function as given in Equation 3.8, where $F(s)$ in the equation is replaced by Equation 4.25. The transfer function is rewritten as

$$H_{\text{ol}}(s) = \frac{K_{\text{pd}} K_{\text{vco}}}{Ns} \frac{1}{s\tau_0} \frac{(1 + s\tau_1)}{(1 + s\tau_2)} \,. \tag{7.9}$$

Phase of the open loop transfer function ($\angle H_{\text{ol}}$) is given by

$$\angle H_{\text{ol}}(s) = -\pi + \arctan\left(\frac{\omega(\tau_1 - \tau 2)}{1 + \omega^2 \tau_1 \tau_2}\right) \,, \tag{7.10}$$

where the phase margin (PM) is

$$\text{PM} = \arctan\left(\frac{\omega(\tau_1 - \tau 2)}{1 + \omega^2 \tau_1 \tau_2}\right) \,, \tag{7.11}$$

$$= \arctan(\omega\tau_1) - \arctan(\omega\tau_2) \,. \tag{7.12}$$

As seen in Equations 7.11 and 7.12, the phase margin contains a frequency dependent phase value. Apply differentiation to the arctan argument in Equation 7.11 with respect to frequency, ω, yields the phase changing rate with respect to frequency and is given by

$$\frac{d}{d\omega}\left(\frac{\omega(\tau_1 - \tau 2)}{1 + \omega^2 \tau_1 \tau_2}\right) = \frac{(1 + \omega^2 \tau_1 \tau_2)(\tau_1 - \tau_2) - \omega(\tau_1 - \tau_2)(2\omega\tau_1\tau_2)}{1 + \omega^2 \tau_1 \tau_2} \,. \tag{7.13}$$

Equating this equation to zero results in a phase turning frequency and is given by

$$\omega = \frac{1}{\sqrt{\tau_1 \tau_2}} \,. \tag{7.14}$$

Rearrange this equation yields

$$\tau_2 = \frac{1}{\tau_1 \omega^2} \, . \tag{7.15}$$

Substituting this equation into Equation 7.11, and choose the loop natural frequency, ω_n, equals to the phase turning frequency, results in a quadratic function (Thompson and Brennan 2005), and is given by

$$\tau_1{}^2 - \frac{2\tau_1}{\omega_n} \tan(\text{PM}) - \frac{1}{\omega_n{}^2} = 0 \, . \tag{7.16}$$

The positive real root for this quadratic equation gives τ_1 in terms of phase margin (PM) and loop natural frequency (ω_n), as given by

$$\tau_1 = \frac{\tan(\text{PM}) + \sec(\text{PM})}{\omega_n} \, . \tag{7.17}$$

Substituting Equation 7.17 into Equation 7.15 gives τ_2 in terms of PM and ω_n, as given by

$$\tau_2 = \frac{1}{\omega_n [\tan(\text{PM}) + \sec(\text{PM})]} \, . \tag{7.18}$$

Here, the τ_0 in terms of PM and ω_n can be obtained by equating the magnitude of open loop transfer function in Equation 7.9 to one, resulting in

$$\tau_0 = \frac{K_{\text{pd}} K_{\text{vco}}}{N \omega_n{}^2} \left(\tan(\text{PM}) + \sec(\text{PM})\right) \, . \tag{7.19}$$

Substituting τ_1, τ_2, and τ_0 in Equations 7.19, 7.17 and 7.18 into Equations 7.6, 7.7, and 7.8 give the resistors and capacitors value for the second order loop filter.

As discussed in Chapters 4 and 5, a third order loop filter is commonly used as it gives a better attenuation for the reference spur. The third order low pass filter transfer function is given by

$$F_3(s) = \frac{1}{s\tau_3} \frac{(1 + s\tau_4)}{(1 + s\tau_5)(1 + s\tau_6)} \, . \tag{7.20}$$

Equating this equation to the third order loop filter transfer function in Equation 4.29 results in

$$\tau_4 = R_2 C_2 \,, \tag{7.21}$$

$$\tau_3 \tau_5 \tau_6 = C_1 C_2 C_3 R_2 R_3 \,, \tag{7.22}$$

$$\tau_3(\tau_5 + \tau_6) = R_2 C_2 (C_1 + C_2) + R_3 C_3 (C_1 + C_2) \,, \tag{7.23}$$

$$\tau_3 = C_1 + C_2 + C_3 \,. \tag{7.24}$$

The extra attenuation that is given by the extra pole (τ_6) in the third order loop filter is given by

$$\text{Attenuation} = 20 \log \left(\sqrt{1 + {\omega_s}^2 {\tau_6}^2} \right) \ (\text{dB}) \,, \tag{7.25}$$

where ω_s is the sampling frequency. However, the extra pole in the third order loop filter degrades the phase margin of the system. The phase margin for the third order filter is given by

$$\text{PM}_{\text{F}_3} = \arctan(\omega\tau_4) - \arctan(\omega\tau_5) - \arctan(\omega\tau_6) \,. \tag{7.26}$$

Comparing this equation to Equation 7.12, it is clearly shows the extra pole decreases the phase margin, hence affect the stability of the system.

Considering the same phase margin and loop natural frequency as in the second order filter, capacitors and resistors value in the third order filter can be calculated (Thompson and Brennan 2005). This can be carried out by equating the magnitude and phase of the third order filter transfer function to the second order filter transfer function, as given in Equations 7.27 and 7.28, respectively.

$$\frac{1 + {\omega_n}^2 {\tau_4}^2}{{\omega_n}^2 {\tau_3}^2 (1 + {\omega_n}^2 {\tau_5}^2)(1 + {\omega_n}^2 {\tau_6}^2)} = \frac{1 + {\omega_n}^2 {\tau_1}^2}{{\omega_n}^2 {\tau_0}^2 (1 + {\omega_n}^2 {\tau_2}^2)} \,, \tag{7.27}$$

$$\frac{\omega_n[-\tau_4 + \tau_5 + \tau_6 + \omega_n^2(\tau_4\tau_5\tau_6)]}{1 + \omega_n^2(\tau_4\tau_5 + \tau_4\tau_6 - \tau_5\tau_6)} = \frac{\omega_n(\tau_2 - \tau_1)}{1 + \omega_n^2 \tau_1 \tau_2} \,. \tag{7.28}$$

Based on Equations 7.27 and 7.28, the τ_3, τ_4, τ_5, and τ_6 in terms of τ_0, τ_1, and τ_2 are obtained. Further, using Equations 7.17, 7.18, 7.19, and 7.25, τ_3, τ_4, τ_5, and τ_6 in terms of phase margin, loop natural frequency, and attenuation magnitude can be attained. Eventually, resistors and capacitors in the third order filter can be calculated based on

Equations 7.21, 7.22, 7.23, and 7.24. All the equations for resistors and capacitors value calculation are presented in Matlab script in Appendix A.3.

As 74.14 MHz reference frequency is chosen for the PLL, the maximum loop bandwidth can be used is about 7 MHz. For this PLL design, a 3 MHz loop bandwidth with a 55° phase margin is chosen.

Loop filter noise

The loop filter noise can be modelled by a noise current in parallel with a noiseless admittance (Herzel *et al.* 2010, Osmany *et al.* 2007). Thermal noise from the filter can be calculated by

$$S_{\mathrm{f_{ol_i}}} = 4kT\mathcal{R}\mathrm{e}(Y(s)) \,, \tag{7.29}$$

where $Y(s)$ is the complex admittance of the filter as seen from the charge pump to ground. For a third order low pass filter, $Y(s)$ in Equation 3.17 is given by

$$Y(s) = \frac{1}{Z_1} + \frac{1}{Z_2} \,, \tag{7.30}$$

where Z_1 and Z_2 are shown in Figure 7.27 (Herzel *et al.* 2010, Osmany *et al.* 2007), and are given by

$$Z_1(s) = \frac{R_2C_2s + 1}{R_2C_1C_2s^2 + C_1s + C_2s} \,, \tag{7.31}$$

$$Z_2(s) = \frac{R_3C_3s + 1}{C_3s} \,. \tag{7.32}$$

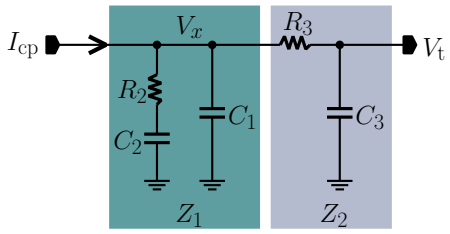


Figure 7.27. Third order low pass filter. Transfer functions of Z_1 and Z_2 is given by Equations 7.31 and 7.32, respectively.

The output to loop filter noise transfer function as given in Equation 3.11 use a voltage noise as the input. Therefore, the thermal noise (from noise current) in Equation 7.29 is modified to

$$S_{f_{olv}}(f) = S_{f_{oli}}(f) \left|F_2(s)\right|^2 . \tag{7.33}$$

Therefore, closed-loop filter noise at the PLL output is given by

$$S_{f_{cl}}(f) = S_{f_{oli}}(f) \left|F_2(s)\right|^2 \left|\frac{\theta_o}{v_f}\right|^2 , \tag{7.34}$$

where $\left|\frac{\theta_o}{v_f}\right|$ is the output to loop filter noise transfer function as given in Equation 3.11. Open loop noise in the noise current and noise voltage models, and closed-loop noise that contributes by the filter are shown in Figure 7.28.

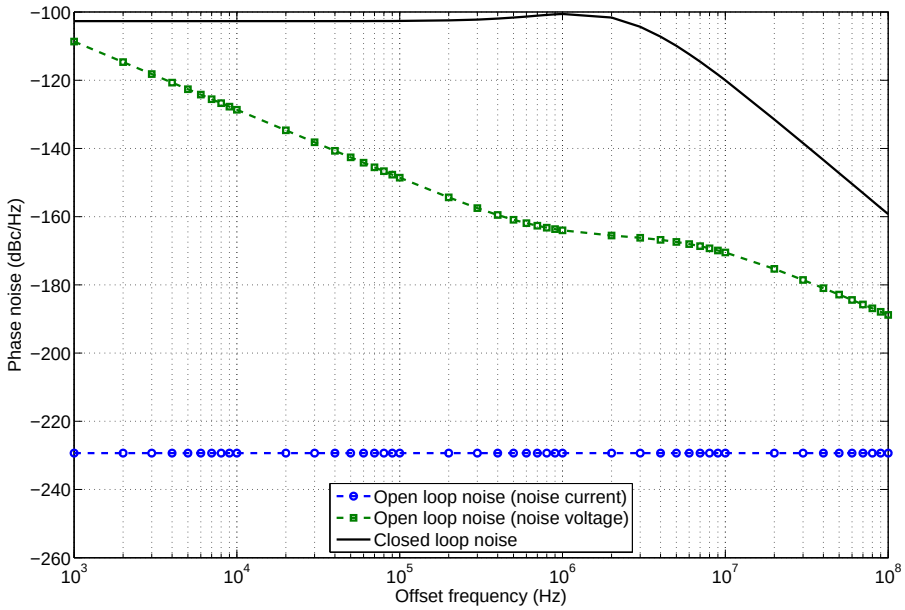


Figure 7.28. Third order loop filter noise spectrum. Thermal noise of the filter is obtained by using a noise current model, which is given by Equations 7.29, 7.30, 7.31, and 7.32. Then, this input noise is converted into voltage noise using Equation 7.33, before the closed-loop noise can be calculated using Equation 7.34.

7.3 PLL Performance

The PFD, charge pump, low pass filter, VCO, frequency divider, and prescaler are connected together to build a PLL system. The PLL layout is shown in Figure 7.29. The

circuit occupies 1.2 mm $\times$ 0.55 mm die area. A separate supply voltages are used for the digital (PFD, charge pump, frequency divider, and prescaler), and analog (VCO) circuits, to minimise the strong digital signal coupling into the VCO output, hence affect the reference spur magnitude. In addition, guide-rings around the digital circuit are made to isolate the digital circuit from the analog circuit.

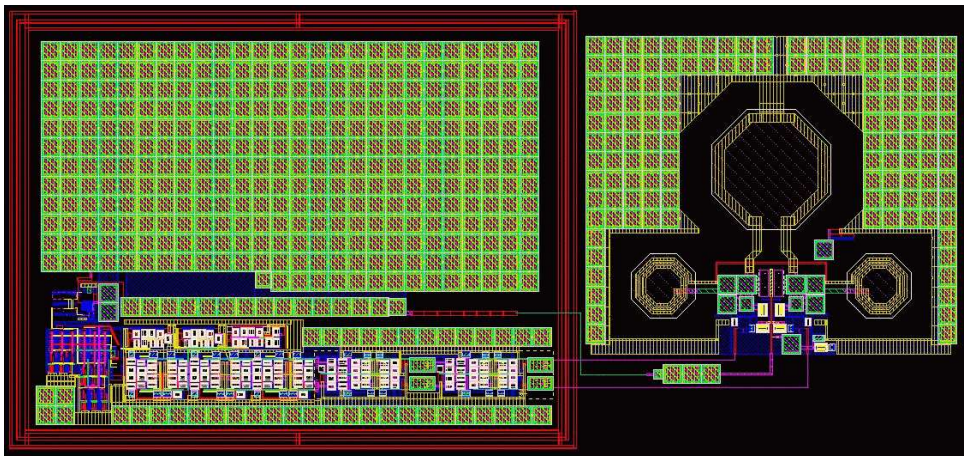


Figure 7.29. PLL layout. The circuit occupies 1.2 mm $\times$ 0.55 mm area.

7.3.1 PLL phase noise

PLL phase noise can be estimated by the technique discussed in Section 3.4.1. Noise from VCO, charge pump, low pass filter, and frequency divider & prescaler, and the total phase noise at the PLL output are shown in Figure 7.30. The close-in phase noise is dominated by the charge pump noise and is expected to be -97.0 dBc/Hz at 1 MHz offset. Meanwhile, VCO noise dominates the PLL phase noise at the outside of the loop bandwidth (which is 3 MHz in this case). At lower bound offset frequency (less than 1 kHz), PLL phase noise is dominated by reference frequency noise. In this work, a low noise crystal oscillator is assumed to be used as the reference signal. As the crystal oscillator noise is very low when compared to circuit noise from PLL components, effect of reference noise is not considered.

7.3.2 PLL reference spur

Reference spur for three different PLLs are compared as shown in Figure 7.31. The first PLL employs a conventional charge pump, and the spur level is at -62.8 dBc/Hz

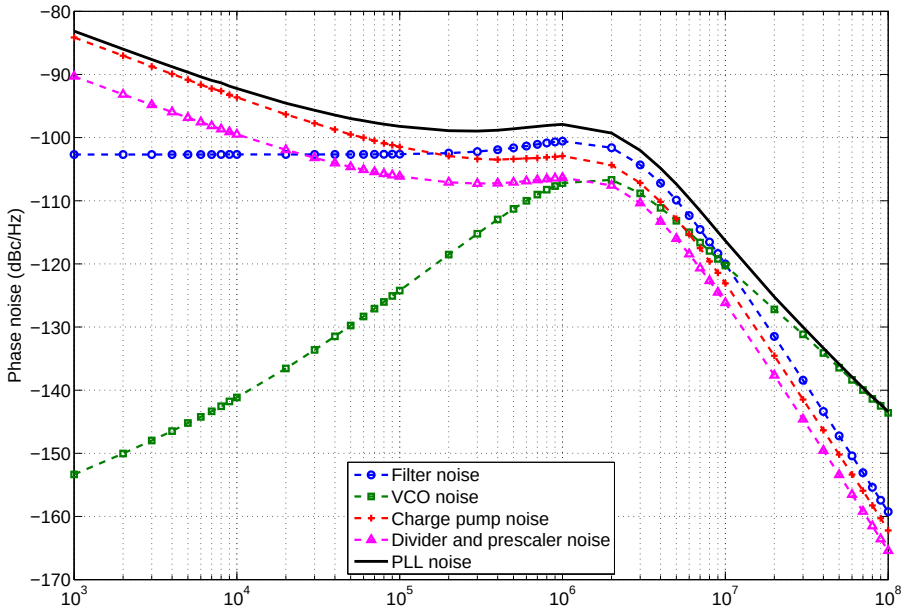


Figure 7.30. PLL phase noise. Here, PLL phase noise is obtained by adding all the closed-loop noise magnitude from the PFD, charge pump, filter, and prescaler and divider, which is obtained by simulation and calculation as discussed in the text. As shown in the spectrum, the PLL close-in phase noise is dominated by charge pump, while the VCO noise dominates the PLL phase noise at the outside of loop bandwidth.

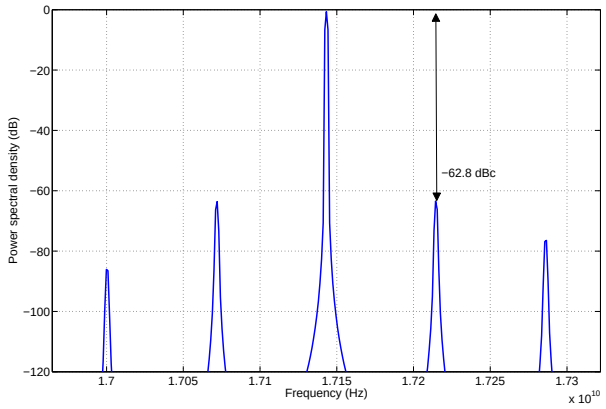
as shown in Figure 7.31(a). The second and third PLLs employ the proposed ratioed current and ratioed with matched current charge pumps, where the spur level is at -66.7 dBc/Hz and -67.2 dBc/Hz, respectively.

Results from the transistor level simulation proves the proposed ratioed current and ratioed with matched current charge pump helps to decrease the reference spur magnitude. As the proposed technique can be implemented only by resizing transistors in the charge pump, the technique can be easily combined with other spur suppression technique such as low VCO gain, current leakage compensation or charge distributed techniques, to further decrease reference spur magnitude.

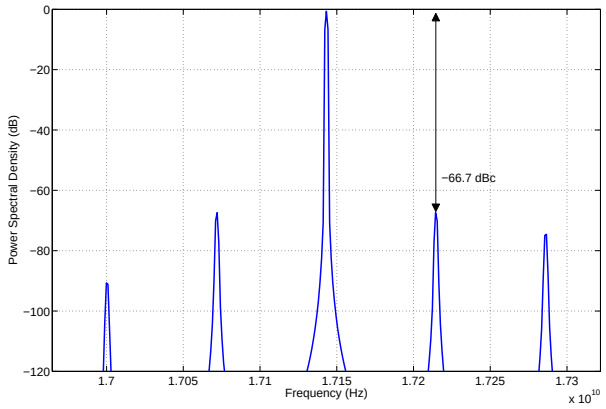
Table 7.2 summarises the ratioed with matched current charge pump PLL performance.

7.4 Chapter Summary

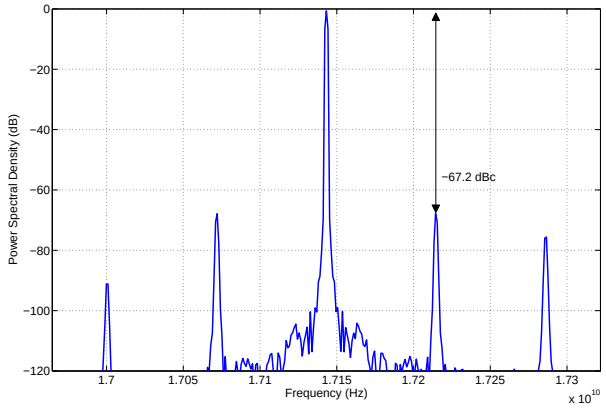
In this chapter, PLLs with the ratioed current and ratioed with matched current charge pumps are implemented at the transistor level using 180 nm SiGe BiCMOS technology. Each PLL component circuit design is discussed. All the PLL component designs are



(a) Conventional charge pump



(b) Ratioed current charge pump



(c) Ratioed with matched current charge pump

Figure 7.31. Reference spur magnitude comparison. Reference spur magnitude is obtained from a transient analysis at the transistor level simulation. PLL output in locked state is captured, and PSD of the signal is calculated and plotted in this figure. For the PSD calculation, an FFT with length of 2^{19}, and hamming window is used. The spectrum shows that the PLL with ratioed current and ratioed with matched current charge pumps give a lower reference spur magnitude when compared to the conventional charge pump PLL.

Table 7.2. Performance summary of the ratioed with matched current charge pump PLL. Phase noise and reference spurs magnitude are obtained from simulations.

Process technology	180 nm SiGe BiCMOS
Reference clock	71.43 MHz
VCO range	15.86 - 18.38 GHz
RF range	57 - 64 GHz
In-band phase noise @ 1 MHz	-97 dBc/Hz
Phase noise @ 100 MHz	-116 dBc/Hz
Reference spurs	-67.2 dBc

simulated individually at the post layout simulation for an accurate result. Phase noise of each component is retrieved for PLL phase noise estimation. These individual components are connected together to form a PLL system. Reference spur levels for our circuits are then compared to a conventional charge pump PLL, resulting in reduced reference spur levels by about 5 dB in the best case. This is the final chapter of our investigation, and the next chapter thus concludes this thesis.

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Chapter 8

Thesis Summary

THIS thesis addresses a key performance issue in an integer-N PLL, namely, the reduction of reference spurs. This chapter presents a summary of this thesis. Chapters 2 and 3 contain review material that embraces PLL types, architectures, components and noise. Chapters 4 to 7 contain the original contributions, which are divided into three parts: analysis, modelling and design. This chapter summarise the original contributions reported in this thesis.

8.1 Analysis

Reference spur mathematical analysis: Chapter 4

Background: Reference spur analysis helps to estimate its magnitude and determine the major contributing factor to the reference spur. However, little work has been carried out in the literature regarding reference spurs. Non-idealities in the PLL circuit result in ripples in the VCO tuning voltage, hence producing reference spurs at the PLL output. A shortcoming in the literature is that this ripple is approximated as a sinusoidal signal, resulting in inaccurate reference spur analysis. Moreover, the analysis in the literature appears to never have been compared to simulation or actual measurement results for validation. In addition, ripples in the VCO tuning voltage have not been fully modelled. These shortcomings thus provide the open questions that we address in this thesis.

Methodology: A time domain analysis is employed to model the affect of circuit non-idealities in the PLL on the reference spur. Narrow-band frequency modulation theory is used to model the PLL output, with a Fourier series used to represent the periodic ripple in the VCO tuning voltage. This mathematical analysis produces an equation that gives the reference spur magnitude in terms of VCO gain, reference frequency, and ripple magnitude. For verification, reference spur magnitude is estimated using the proposed mathematical analysis is compared to a simulation result.

Result: Two mathematical analyses are compared to a simulation result. The first analysis is for the reference spur magnitude only, where analysis and simulation are within 1% of each other. The second analysis is the ripple magnitude mathematical modelling, where the reference spur magnitude is within 3% of the simulation results.

Future work: For the ripple magnitude mathematical analysis, five major contributing factors to the reference spur magnitude are considered, namely, charge pump current mismatch and PFD delay, switching delay, rise and fall time characteristics of the charge pump current, current leakage and loop filter. The spur magnitude is also affected by other factors such as charge injection and charge sharing. Therefore, the mathematical model for the ripple magnitude may be improved if other factors are considered.

Original contribution: For the first time, a mathematical analysis of ripples in the VCO tuning voltage is presented, and included in the reference spur analysis, resulting in an accurate reference spur magnitude estimation. In addition, the presented reference spur analysis proves that the spur magnitude is 2π lower when compared to the previous analysis in the literature.

8.2 Modelling

Reference spur behavioural modelling: Chapter 5

Background: Simulating PLLs at the transistor level is time consuming, therefore much research has been carried out in behavioural modelling, so that PLL simulation can be carried out at behavioural level, hence saving a large amount of simulation time. Unfortunately, previous work in this area focuses on phase noise modelling and the dynamic behaviour of PLLs. Therefore, PLL behavioural modelling for reference spur simulation is proposed.

Methodology: PLL behavioural modelling is implemented using Simulink within Matlab. Each non-ideality in the PLL circuit that contributes to reference spur is included in the behavioural modelling. These non-idealities include the PFD delay, charge pump current mismatch, charge pump current leakage, rise and fall time characteristics of the charge pump current, and switching delay. Reference spur magnitude from the behavioural level simulation is compared to a transistor level simulation result.

Result: Reference spur magnitude from the proposed behavioural model is within 4% of the transistor level simulation result. The VCO tuning voltage response from the behavioural modelling is similar to the transistor level simulation result. Using the proposed Simulink behavioural model, a large amount of simulation time can be reduced without compromising the performance estimation accuracy.

Original contribution: This is the first time a PLL reference spur behavioural modelling is implemented. The proposed behavioural model helps to simulate reference spur and PLL dynamic behaviour in a very short simulation period (Kamal *et al.* 2010, Kamal *et al.* 2012).

8.3 Design

Spur suppression technique: Chapters 6 and 7

Background: Some previous research has been carried out in spur suppression techniques. One spur suppression approach is a charge pump current matching, to reduce ripple magnitude in the VCO tuning voltage. However, switching delay in the charge pump prevents this method from achieving a minimum ripple magnitude.

Methodology: An optimum charge pump current ratio is determined from the PFD delay and switching delay. The optimum current ratio is implemented by resizing transistors in the charge pump circuit. Then, a PLL containing this ratioed current charge pump is designed and simulated to obtain the reference spur magnitude. The spur magnitude is compared to a conventional charge pump PLL. In addition, the ratioed current charge pump is also combined with the current matching technique, and its reference spur magnitude is compared to the other two PLLs.

Result: Ratioed current and ratioed with matched current charge pump PLLs are designed and simulated. The reference spur magnitudes for these two PLLs are compared to a conventional charge pump PLL. Based on the simulation result, the proposed spur suppression techniques are shown to reduce the reference spur magnitude.

Future work: In this thesis, the optimum current ratio is calculated according to parameters given by simulation results, and transistors in the charge pump are resized to give the optimum current ratio. The implementation may be improved if an automated ratioed current charge pump is designed, where the optimum current is calculated by a circuit and the charge pump current changes according to the optimum current.

Original contribution: For the first time, a determination of an optimum current ratio between I_{dn} and I_{up} is introduced. This optimum current helps to reduce the ripple magnitude in the VCO tuning voltage that is caused by charge pump current mismatch, PFD delay, and switching delay, hence reducing the reference spur magnitude.

Appendix A

Matlab codes

THIS appendix presents Matlab codes used in this thesis, which is a ripple voltage amplitude calculation, charge pump current generation, and third order filter equations. The code for ripple voltage amplitude and charge pump current generation is based on analysis and discussions in Chapter 4. Meanwhile, the third order equations code is for resistors and capacitors value calculation for a loop filter design in Chapter 7.

A.1 Ripple voltage amplitude calculation

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%            Ripple voltage on VCO tuning voltage                     %%%%%
%%%%%                                                                     %%%%%
%%%%%                    Author: Noorfazila Kamal                         %%%%%
%%%%%                    Date  : 25/5/2010                                %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clear;
clc;

%=======Data from transistor level simulation using Cadence Spectre=======%

Fvco =1.94499E+10;      % VCO output frequency
Fref = Fvco/256;        % Reference frequency
Tref = 1/Fref;          % Reference period
fs = 1e6;               % Resolution

Tpfd = 315e-12;         % PFD delay
Tinv = 25e-12;          % Switching delay

%Charge pump current (Icp)
Iup = 490.8e-6;
Idn = 511.5e-6;

%Leakage current
Icp_leak = 5.565e-8;
Itune_leak = 5.800e-8;

%Second order loop filter
C=16e-12;

tauR_up2 = 21e-12;       % Iup: time constant on rising edge
tauF_up2 = 23e-12;       % Iup: time constant on falling edge
tauR_dn2 = 6.2e-12;      % Idn: time constant on rising edge
tauF_dn2 = 17e-12;       % Idn: time constant on falling edge

%Third order loop filter
R3 = 2.785e3;
C3 = 3.85e-12;
C1 = 8.26e-12;
R2 = 2.65e3;
C2 = 109.86e-12;

tauR_up3 = 22.5e-12;    % Iup: time constant on rising edge
tauF_up3 = 24e-12;      % Iup: time constant on falling edge
tauR_dn3 = 8e-12;       % Idn: time constant on rising edge
tauF_dn3 = 27e-12;      % Idn: time constant on falling edge
% time constant for third order filter is larger due to larger impedance

%=========================================================================%
```

```

%Signal difference between UP and DOWN signals due to charge pump
%current mismatch.

if (Iup > Idn)
    Tdiff = Tpfd*(Iup/Idn - 1);
    Tup = Tpfd;
    Tdn = Tdiff + Tpfd;
    Tdel_up = Tinv + Tdiff;
    Tdel_dn = 0;
elseif (Idn > Iup)
    Tdiff = Tpfd*(Idn/Iup - 1);
    Tup = Tdiff + Tpfd;
    Tdn = Tpfd;
    Tdel_up = Tinv;
    Tdel_dn = Tdiff;
end

%Maximum period for HIGH signal
maxT = Tpfd+Tdiff;


%========================Second order loop filter========================%

% Charge pump current
[Iup2,t] = IcpDelay(Iup,tauR_up2,tauF_up2,Tref,Tup,fs,Tdel_up,maxT);
[Idn2,t] = IcpDelay(Idn,tauR_dn2,tauF_dn2,Tref,Tdn,fs,Tdel_dn,maxT);
Icp2 = Iup2 - Idn2;

%Ripple voltage
Vt_fs2 = cumsum(Icp2*(Tref/fs)/C);
V_fs2 = abs(Vt_fs2(round(maxT*fs/Tref)));
V_leak = (Itune_leak*Tref/C)+(Icp_leak*(Tref-maxT)/C);
deltaV_fs2 = V_fs2 + V_leak;
%========================================================================%


%========================Third order loop filter=========================%

% Charge pump current
[Iup3,t] = IcpDelay(Iup,tauR_up3,tauF_up3,Tref,Tup,fs,Tdel_up,maxT);
[Idn3,t] = IcpDelay(Idn,tauR_dn3,tauF_dn3,Tref,Tdn,fs,Tdel_dn,maxT);
Icp3 = Iup3 - Idn3;

%Ripple voltage
Vx = cumsum(Icp*(Tref/fs)/C1);
I3 = Vx/R3;
Vt_fs3 = cumsum(I3*(Tref/fs)/C3);
V_fs3 = max(abs(Vt_fs3));
deltaV_fs3 = 2*V_fs3;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

A.2 Charge pump current generation

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%       IcpDelay function: charge pump current (Iup or Idn)         %%%%%
%%%%%                                                                   %%%%%
%%%%%                   Author: Noorfazila Kamal                        %%%%%
%%%%%                   Date  : 16/5/2010                               %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Parameters declaration:
%tauR = rise time response
%tauF = fall time response
%Tref = reference signal period
%Tfall = UP/DOWN 'HIGH' period
%fs = resolution
%Tdiff = delay caused by switching delay;
%maxT = maximum 'HIGH' period for UP & DOWN signals


function [I,t] = generate_IcDelay(Iup,tauR,tauF,Tref,Tfall,fs,Tdiff,maxT)

smpl = fs;        % number of sample
maxn = 1.15*maxT/(Tref/fs); % set maximum data
I = zeros(1,maxn);

delay = round((Tdiff/Tref)*smpl);
first_period = round((Tfall/Tref)*smpl)+delay;

for n=1:maxn+1;
    if(n<=delay)
        I(n) = 0;
    elseif((n>delay) && (n<=first_period))
        I(n) = Iup*(1-exp(-(n-delay)*Tref/(fs*tauR)));
    else
        I(n) = Iup*(1-exp(-first_period*Tref/(fs*tauR)))...
            *(exp(-(n-first_period)*Tref/(fs*tauF)));
    end
end

t = [0:Tref/fs:maxn*(Tref/fs)];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

A.3 Third order filter equations

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%                           Third order low pass filter                                     %%%%%
%%%%%                                                                                           %%%%%
%%%%%                           Author: Noorfazila Kamal                                        %%%%%
%%%%%                           Date  : 13/1/2009                                               %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
s=zpk('s');

 Fref = 71.43e6;           % Reference frequency
LB_Hz =4e6;                % Loop bandwidth (Hz)
LB = 2*pi*LB_Hz;           % Loop bandwidth (rad/s)
PM_deg = 50;               % Phase margin (degree)
PM = (PM_deg/180)*pi;      % Phase margin (rad)
wn = LB/1.33;              % Natural frequency
 Icp = 500e-6;             % Charge pump current
Kp = Icp/(2*pi);           % PFD gain
Kv = 2*pi*3e9;             % VCO gain
N = 240;                   % Frequency division ratio
ws = 2*pi*Fref;            % Sampling frequency(rad/s)

 atten = 10;                          % Attenuation
n = ((10^(atten/10))-1)^(1/2);  %n is temp
nmax = (ws/wn)*(((cos(PM)-(2-(2*sin(PM)))^(1/2)))/(sin(PM)-1)); % maximum n


% Filter time constants

 tau0 = ((Kp*Kv)/(N*wn^2))*(tan(PM)+sec(PM));
 tau1 = (tan(PM)+sec(PM))/wn;
 tau2 = 1/(wn*(tan(PM)+sec(PM)));
 tau4 = tau1;
 tau6 = n/ws;
 tau5 = ((ws*cos(PM))-(n*wn)*(1+sin(PM)))/(wn*((ws*(1+sin(PM)))-(n*wn*cos(PM))));
 tau3 = tau0*(((1+(wn^2*tau2^2))/((1+(wn^2*tau5^2))*(1+(wn^2*tau6^2))))^(1/2));


% Calculate resistor and capacitor value

C1 = (3/5)*((tau3*tau5)/tau4);
C2 = ((tau3*C1)*(tau5-tau4)*(tau6-tau4))/((C1*tau4^2)-(tau3*tau5*tau6));
C3 = -1*(((tau4*C1)-(tau5*tau3))*((C1*tau4)-(tau3*tau6)))/((C1*tau4^2)-(tau3*tau5*tau6));
R2 = (tau4*((C1*tau4^2)-(tau3*tau5*tau6)))/(tau3*C1*((tau4^2+(tau5*tau6))-(tau4*(tau5+tau6))));
R3 = (-1*tau3*tau5*tau6*((C1*tau4^2)-(tau3*tau5*tau6)))/(tau4*C1*(((tau4*C1)-(tau3*tau5)) ...
      *((tau4*C1)-(tau3*tau6))));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

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Appendix B

Test chips

THIS appendix contains GLIMMR test chip layout and die photos. Since 2006, three GLIMMR test chips (GTC) have been fabricated in 180 nm SiGe BiCMOS technology by Jazz Semiconductor. The circuits are designed and simulated using Cadence Design Systems.

B.1 GLIMMR Test Chips

Figures B.1 and B.2 show the first two GLIMMR test chips. Unfortunately, image of full GTC3 is not avalilable. Only the PLL test circuit in the GTC3 is available, as shown in Figure B.3. Size of each GTC is 5 mm $\times$ 5 mm die area.

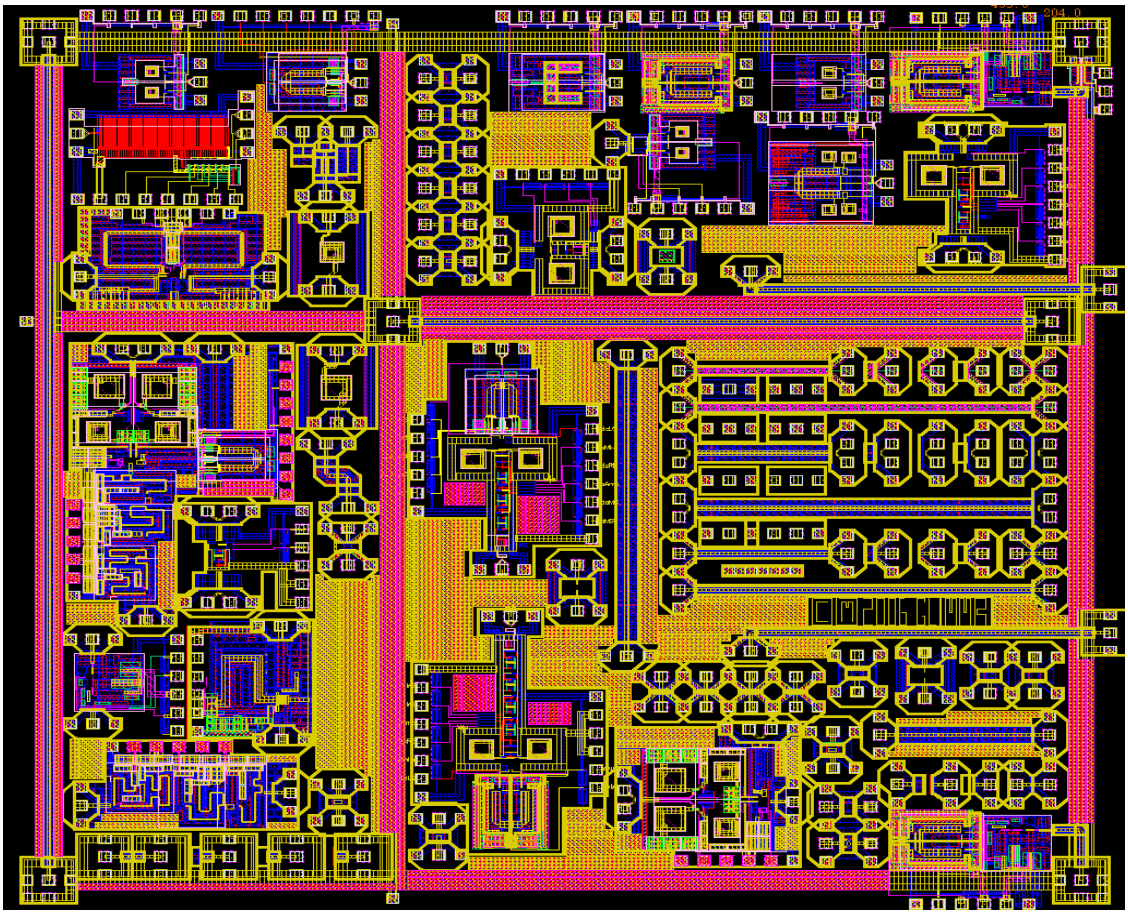

Figure B.1. GLIMMR test chip 1 (GTC1). The GTC1 was fabricated in January 2006. The circuit includes individual RF and analog components for design validation. Test circuits that fabricated on the GTC1 are analog-to-digital converter (ADC), mixer, power amplifier, low noise amplifier (LNA), voltage-controlled oscillator (VCO), frequency divider, and transmission lines.

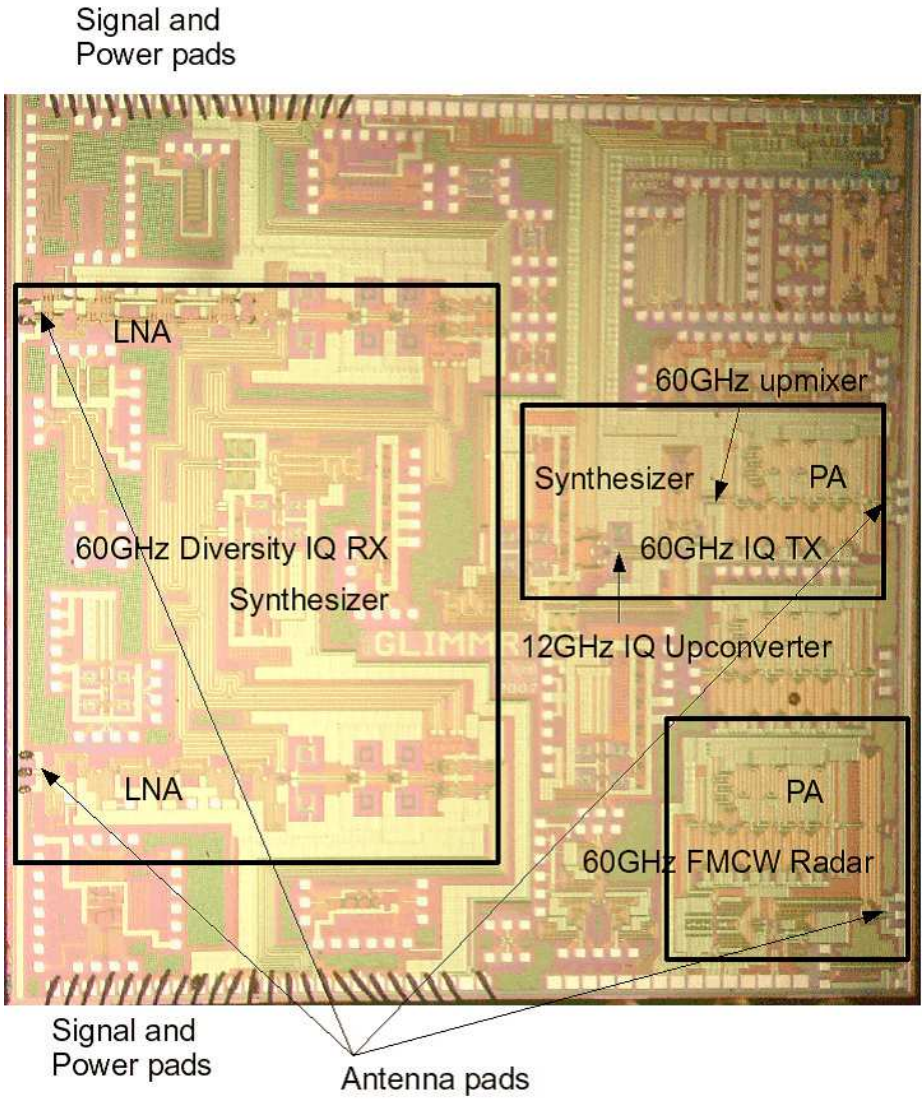

Figure B.2. GLIMMR test chip 2 (GTC2). The GTC2 was fabricated in January 2007. This test chip contains of a few sub-systems and test circuits such as 40 GHz synthesizer, 60 GHz transmitter and receiver, bond wire antenna, 1 GHz 5 bits ADC, 1 GHz 5 bits DAC, and transmission lines.

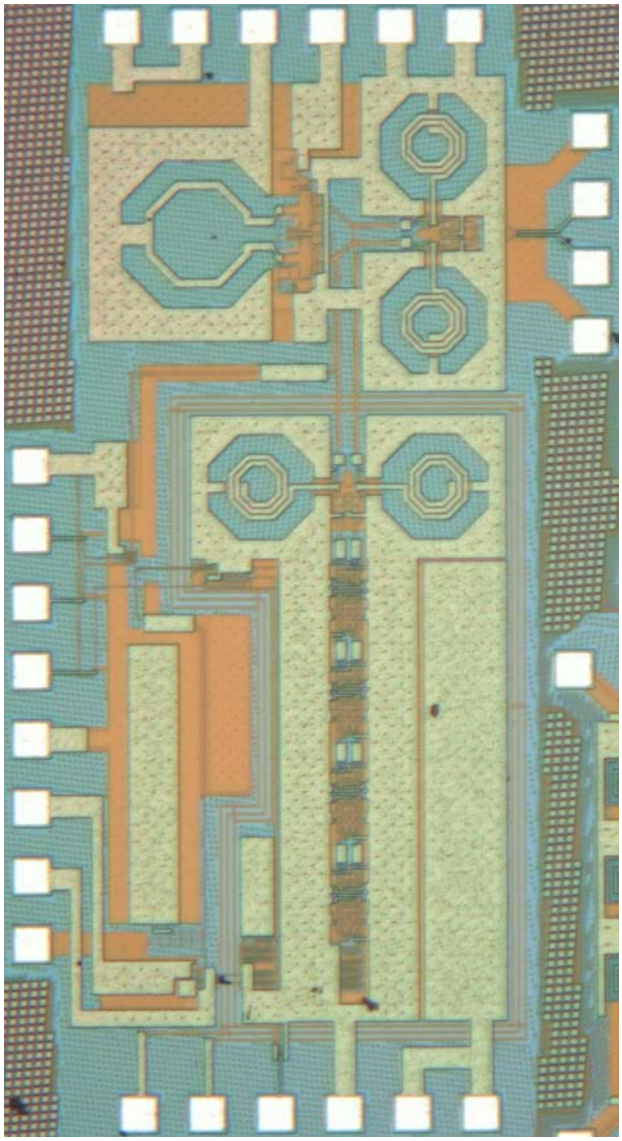

Figure B.3. PLL in the GLIMMR test chip 3 (GTC3). This is micrograph of the PLL test circuit in the GTC3. Unfortunately, layout and micrograph of the GTC3 are not available. Besides the PLL test circuit, GTC3 also contains a complete 60 GHz transmitter and receiver.

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List of Acronyms

ADPLL	All-digital phase-locked loop
CCO	Current-Controlled Oscillator
CML	Common Mode Logic
DCO	Digitally Controlled Oscillator
ECL	Emitter Coupled Logic
GLIMMR	Gigabit Low-cost Integrated Millimeter-wave Radio
HDL	Hardware Description Language
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
LPF	Low pass filter
MAC	Medium Access Control
MSB	Most Significant Bit
P2D	Phase-to-digital
PBRS	Pseudo-Random-Bit-String
PD	Phase detector
PFD	Phase/Frequency Detector
PLL	Phase-Locked Loop
PSD	Power Spectral Density
RF	Radio Frequency
rms	root-mean-square

SCL	Source Coupled Logic
SSPD	Sub-Sampling Phase Detector
TDC	Time-to-digital converter
TSPC	True Single-Phase Clocked
VCCS	Voltage Controlled Current Source
VCO	Voltage-Controlled Oscillator
VIC	Variable impedance converter
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

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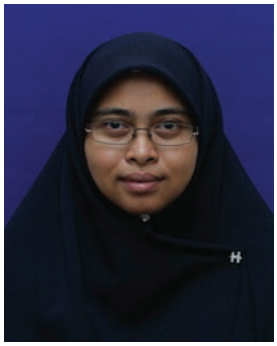
Biography



Noorfazila Kamal was born in Perak, Malaysia in 1979. From 1997 to 2000, she was educated at Universiti Teknologi Malaysia (UTM), in Johor Bharu, Malaysia, where she obtained a Bachelor's Degree in Computer Engineering with honours. Her undergradute project title is Speech Recognition for Arabic Alphabet, under supervision of Prof. Abdul Rahman Al-Attas. In 2001 she worked as a tutor at Faculty of Electrical Engineering, Universiti Teknologi Malaysia. In October 2002, she joined The Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia.

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