Neuromorphic VLSI Designs for Spike Timing and Rate-based Synaptic Plasticity with Application in Pattern Classification

by

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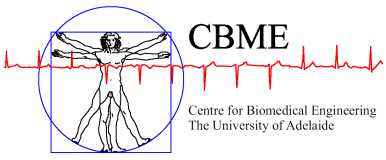

THE UNIVERSITY *of* ADELAIDE

To my dearest wife, Maryam
and to my Mum and Dad,
with all my love.

Contents

Abstract

This thesis presents a versatile study on the design and Very Large Scale Integration (VLSI) implementation of various synaptic plasticity rules ranging from phenomenological rules, to biophysically realistic ones. In particular, the thesis aims at developing novel spike timing-based learning circuits that advance the current neuromorphic systems, in terms of power consumption, compactness and synaptic modification (learning) abilities. Furthermore, the thesis investigates the usefulness of the developed designs and algorithms in specific engineering tasks such as pattern classification. To follow the mentioned goals, this thesis makes several original contributions to the field of neuromorphic engineering, which are briefed in the following.

First, a programmable multi-neuron neuromorphic chip is utilised to implement a number of desired rate- and timing-based synaptic plasticity rules. Specific software programs are developed to set up and program the neuromorphic chip, in a way to show the required neuronal behaviour for implementing various synaptic plasticity rules. The classical version of Spike Timing Dependent Plasticity (STDP), as well as the triplet-based STDP and the rate-based Bienenstock-Cooper-Munro (BCM) rules are implemented and successfully tested on this neuromorphic device. In addition, the implemented triplet STDP learning mechanism is utilised to train a feedforward spiking neural network to classify complex rate-based patterns, with a high classification performance.

In the next stage, VLSI designs and implementations of a variety of synaptic plasticity rules are studied and weaknesses and strengths of these implementations are highlighted. In addition, the applications of these VLSI learning networks, which build upon various synaptic plasticity rules are discussed. Furthermore, challenges in the way of implementing these rules are investigated and effective ways to address those challenges are proposed and reviewed. This review provides us with deep insight into the design and application of synaptic plasticity rules in VLSI.

Next, the first VLSI designs for the triplet STDP learning rule are developed, which significantly outperform all their pair-based STDP counterparts, in terms of learning capabilities. It is shown that a rate-based learning feature is also an emergent property

of the new proposed designs. These primary designs are further developed to generate two different VLSI circuits with various design goals. One of these circuits that has been fabricated in VLSI as a proof of principle chip, aimed at maximising the learning performance—but this results in high power consumption and silicon real estate. The second design, however, slightly sacrifices the learning performance, while remarkably improves the silicon area, as well as the power consumption of the design, in comparison to all previous triplet STDP circuits, as well as many pair-based STDP circuits. Besides, it significantly outperforms other neuromorphic learning circuits with various biophysical as well as phenomenological plasticity rules, not only in learning but also in area and power consumption. Hence, the proposed designs in this thesis can play significant roles in future VLSI implementations of both spike timing and rate based neuromorphic learning systems with increased learning abilities. These systems offer promising solutions for a wide set of tasks, ranging from autonomous robotics to brain machine interfaces.

Statement of Originality

I certify that this work contains no material, which has been accepted for the award of any other degree or diploma in my name, in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text. In addition, I certify that no part of this work will, in the future, be used in a submission in my name, for any other degree or diploma in any university or other tertiary institution without the prior approval of the University of Adelaide and where applicable, any partner institution responsible for the joint-award of this degree.

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S. Mostafa Rahimi Azghadi,
March 2014,
Adelaide

Thesis Conventions

The following conventions have been adopted in this Thesis:

Typesetting

This document was compiled using LaTeX2e. Texmaker and TeXstudio were used as text editor interfaced to LaTeX2e. Inkscape and Xcircuit were used to produce schematic diagrams and other drawings.

Referencing

The Harvard style has been adopted for referencing.

System of units

The units comply with the international system of units recommended in an Australian Standard: AS ISO 1000–1998 (Standards Australia Committee ME/71, Quantities, Units and Conversions 1998).

Spelling

Australian English spelling conventions have been used, as defined in the Macquarie English Dictionary (A. Delbridge (Ed.), Macquarie Library, North Ryde, NSW, Australia, 2001).

Awards and Scholarships

2013

- Simon Rockliff Scholarship, DSTO
- Doreen McCarthy Research Bursary, AFUW-SA
- IEEE South Australia Section Student Travel Award, IEEE SA

2012

- Brain Corporation Fellowships for Spiking Neural Networks, IEEE WCCI2012
- The IEEE Computational Intelligence Society travel grant, IEEE WCCI2012
- Research Abroad Scholarship, The University of Adelaide
- D. R. Stranks fellowship, The University of Adelaide

2011

- Japanese Neural Network Society Travel Award, Okinawa Institute of Science and Technology

2010

- International Postgraduate Research Scholarships, The Australian Government
- Adelaide University Scholarships, The University of Adelaide

Publications

Journal Articles

Azghadi-M. R., Al-Sarawi-S., Iannella-N., Indiveri-G., Abbott-D. (2014b). Spike-based synaptic plasticity in silicon: Design, implementation, application, and challenges, *Proceedings of the IEEE*, **102**(5), pp. 717–737. *

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Note: Articles with an asterisk (*) are directly relevant to this thesis.

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